

PDTD113/123/143/114EQA series

50 V, 500 mA NPN resistor-equipped transistors

Rev. 1 — 4 February 2016

Product data sheet

1. Product profile

1.1 General description

NPN Resistor-Equipped Transistor (RET) family in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

Table 1. Product overview

Type number	R1	R2	Package NXP	PNP complement
PDTD113EQA	1 k Ω	1 k Ω	DFN1010D-3 (SOT1215)	PDTB113EQA
PDTD123EQA	2.2 k Ω	2.2 k Ω		PDTB123EQA
PDTD143EQA	4.7 k Ω	4.7 k Ω		PDTB143EQA
PDTD114EQA	10 k Ω	10 k Ω		PDTB114EQA

1.2 Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- $\pm 10\%$ resistor ratio tolerance
- Simplifies circuit design
- Reduces component count
- Reduced pick and place costs
- Low package height of 0.37 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint
- AEC-Q101 qualified

1.3 Applications

- Digital applications
- Cost saving alternative for BC807/BC817 series in digital applications
- Controlling IC inputs
- Switching loads

1.4 Quick reference data

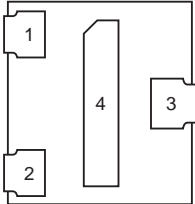
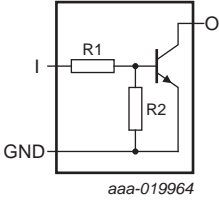
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	500	mA



2. Pinning information

Table 3. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p>Transparent top view</p>	 <p>aaa-019964</p>
2	GND	GND (emitter)		
3	O	output (collector)		
4	O	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTD113EQA	DFN1010D-3	plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 × 1.0 × 0.37 mm	SOT1215
PDTD123EQA			
PDTD143EQA			
PDTD114EQA			

4. Marking

Table 5. Marking codes

Type number	Marking code
PDTD113EQA	01 00 11
PDTD123EQA	01 01 10
PDTD143EQA	01 10 01
PDTD114EQA	01 11 01

4.1 Binary marking code description

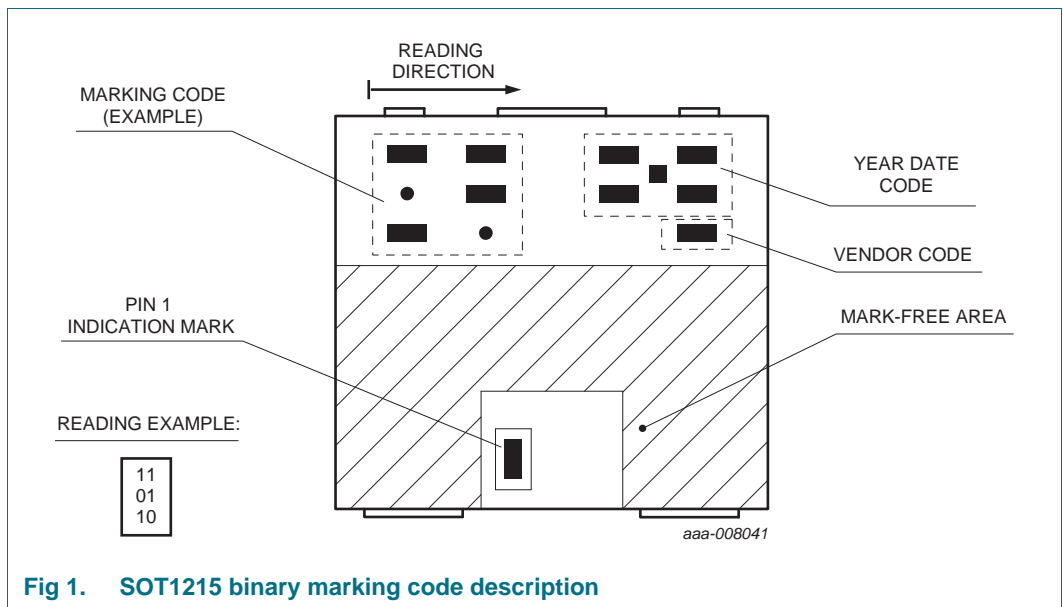


Fig 1. SOT1215 binary marking code description

5. Limiting values

Table 6. Limiting values

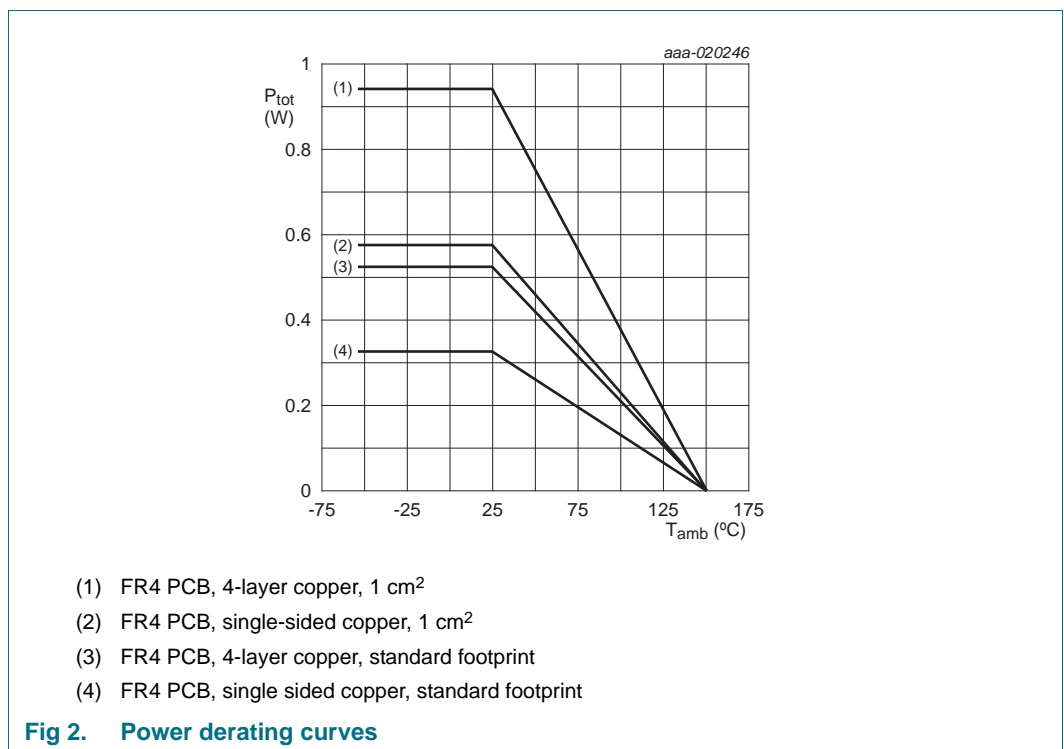
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	10	V

Table 6. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _I	input voltage					
	PDTD113EQA		-10	+10	V	
	PDTD123EQA		-10	+12	V	
	PDTD143EQA		-10	+30	V	
	PDTD114EQA		-10	+50	V	
I _O	output current		-	500	mA	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	325	mW
			[2]	-	575	mW
			[3]	-	525	mW
			[4]	-	940	mW
T _j	junction temperature		-	150	°C	
T _{amb}	ambient temperature		-55	+150	°C	
T _{stg}	storage temperature		-65	+150	°C	

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated; mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm².

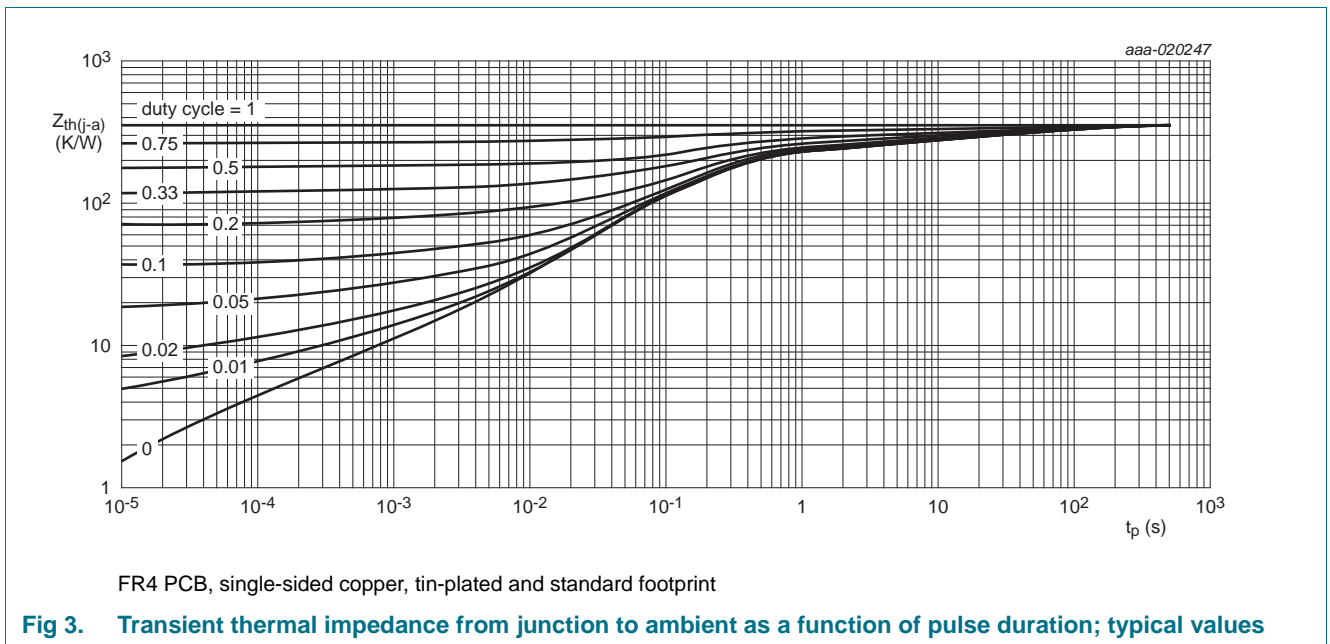


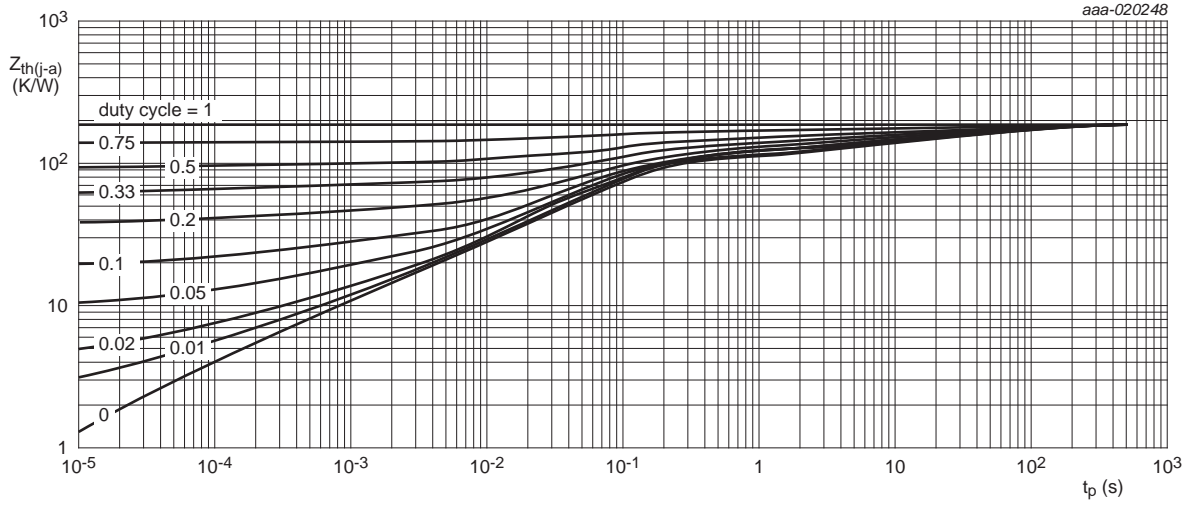
6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
			[2]	-	-	218	K/W
			[3]	-	-	239	K/W
			[4]	-	-	133	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W	

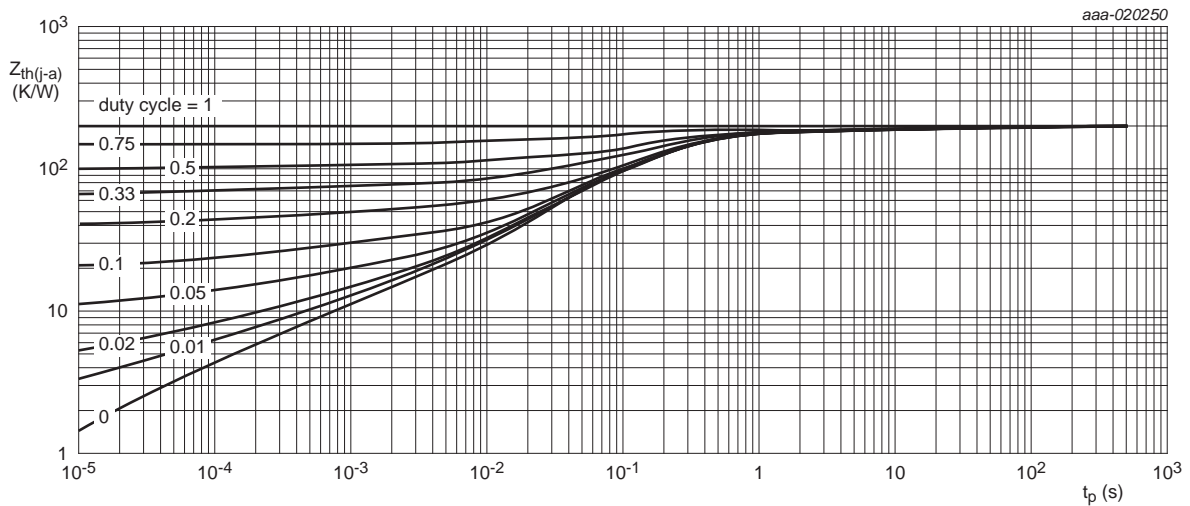
- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated; mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm².





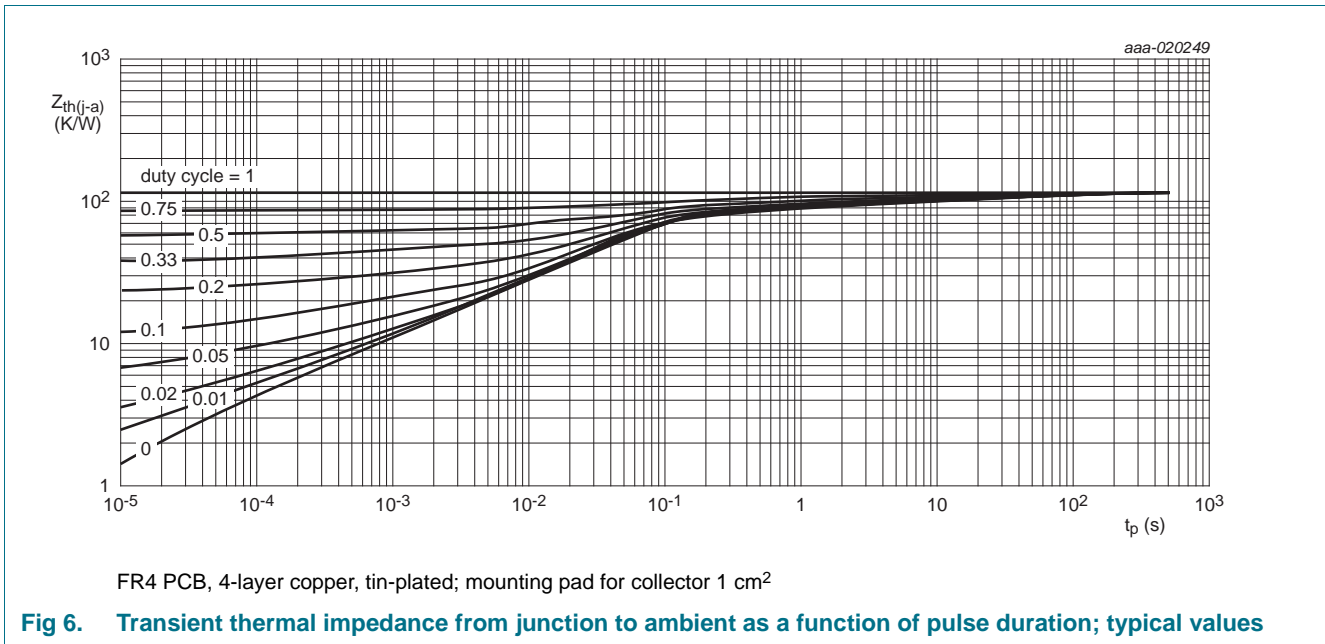
FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm²

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated and standard footprint

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



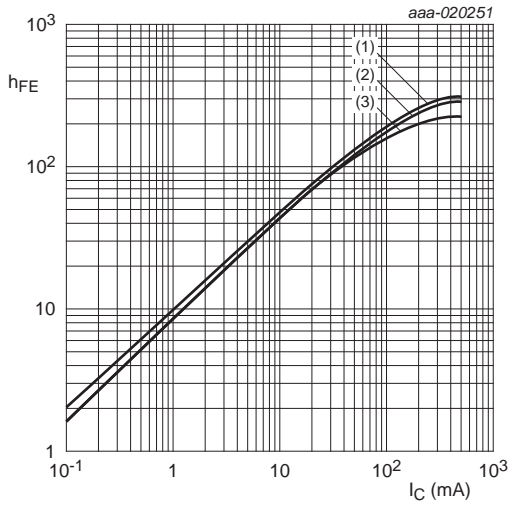
7. Characteristics

Table 8. Characteristics
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 50 V; I _B = 0 A	-	-	0.5	μA
I _{EBO}	emitter-base cut-off current					
	PDTD113EQA	V _{EB} = 5 V; I _C = 0 A	-	-	4	mA
	PDTD123EQA		-	-	2	mA
	PDTD143EQA		-	-	0.9	mA
PDTD114EQA				0.4	mA	
h _{FE}	DC current gain					
	PDTD113EQA	V _{CE} = 5 V; I _C = 50 mA	33	-	-	
	PDTD123EQA		40	-	-	
	PDTD143EQA		60	-	-	
PDTD114EQA	70		-	-		
V _{CEsat}	collector-emitter saturation voltage	I _C = 50 mA; I _B = 2.5 mA	-	-	100	mV
V _{I(off)}	off-state input voltage					
	PDTD113EQA	V _{CE} = 5 V; I _C = 100 μA	0.6	1.05	1.5	V
	PDTD123EQA		0.6	1.05	1.8	V
	PDTD143EQA		0.6	1.05	1.5	V
PDTD114EQA	0.6		1.05	1.5	V	
V _{I(on)}	on-state input voltage					
	PDTD113EQA	V _{CE} = 0.3 V; I _C = 20 mA	1	1.45	1.8	V
	PDTD123EQA		1	1.5	2	V
	PDTD143EQA		1	1.7	2.2	V
PDTD114EQA	1		2.2	3	V	
R1	bias resistor 1 (input)		[1]			
	PDTD113EQA		0.7	1	1.3	kΩ
	PDTD123EQA		1.54	2.2	2.86	kΩ
	PDTD143EQA		3.3	4.7	6.1	kΩ
	PDTD114EQA		7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.9	1	1.1
C _c	collector capacitance	V _{CB} = 10 V; I _E = i _e = 0 A; f = 1 MHz	-	5	-	pF
f _T	transition frequency	V _{CE} = 5 V; I _C = 50 mA; f = 100 MHz	[2]	-	210	-

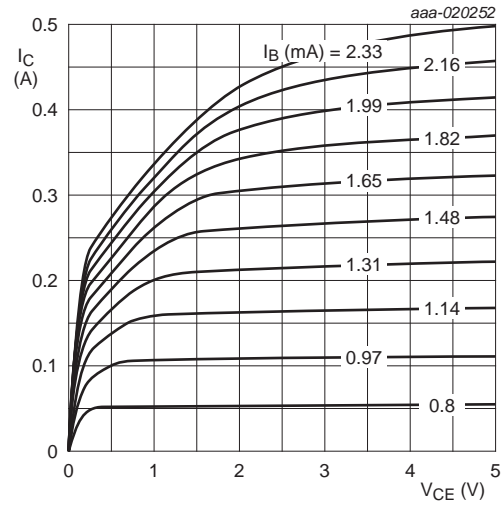
[1] See section test information for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.



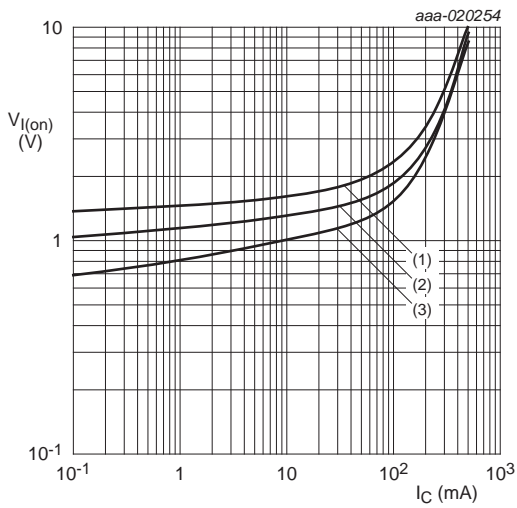
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 7. PDTD113EQA: DC current gain as a function of collector current; typical values



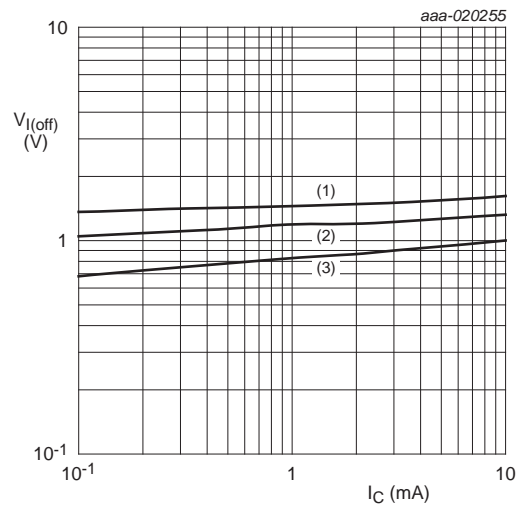
$T_{amb} = 25\text{ °C}$

Fig 8. PDTD113EQA: Collector current as a function of collector-emitter voltage; typical values



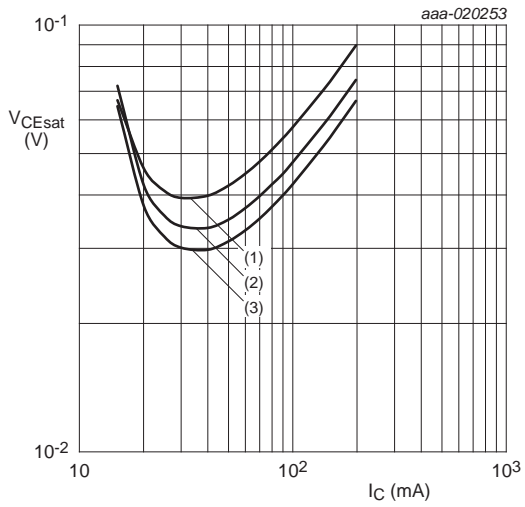
$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 9. PDTD113EQA: On-state input voltage as a function of collector current; typical values



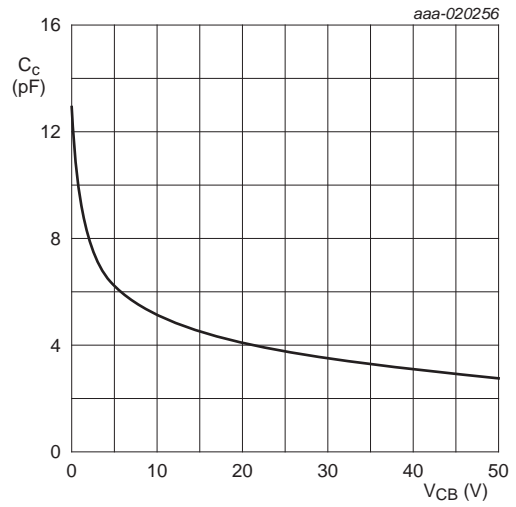
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 10. PDTD113EQA: Off-state input voltage as a function of collector current; typical values



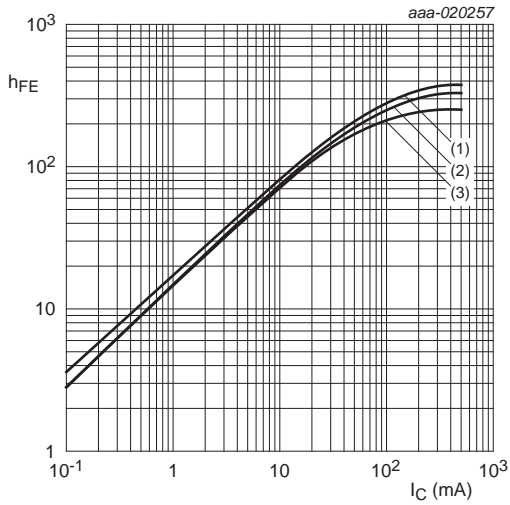
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 11. PDTD113EQA: Collector-emitter saturation voltage as a function of collector current; typical values



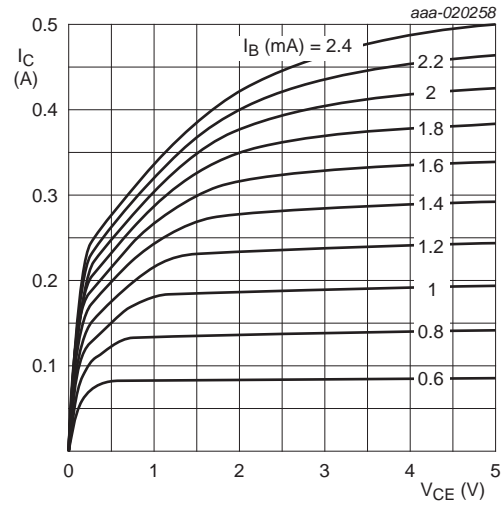
$f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$

Fig 12. PDTD113EQA: Collector capacitance as a function of collector-base voltage; typical values



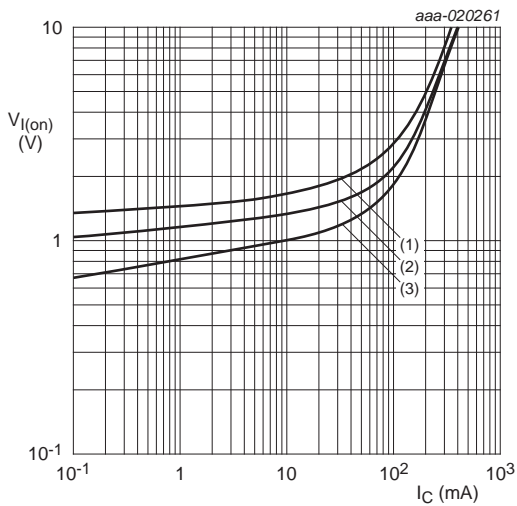
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 13. PDTD123EQA: DC current gain as a function of collector current; typical values



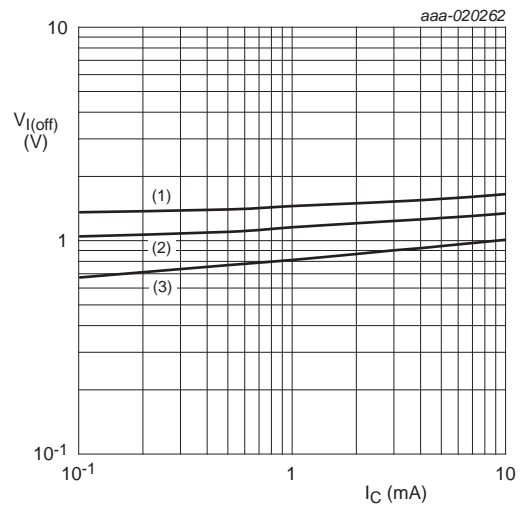
$T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 14. PDTD123EQA: Collector current as a function of collector-emitter voltage; typical values



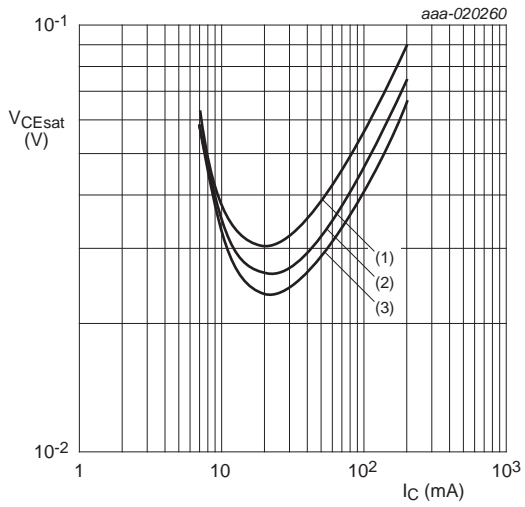
$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 15. PDTD123EQA: On-state input voltage as a function of collector current; typical values



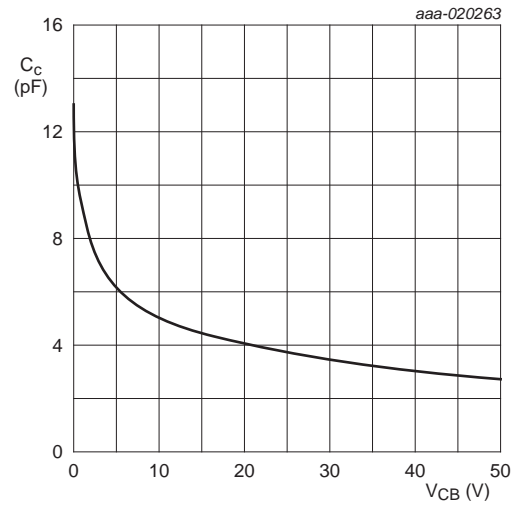
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 16. PDTD123EQA: Off-state input voltage as a function of collector current; typical values



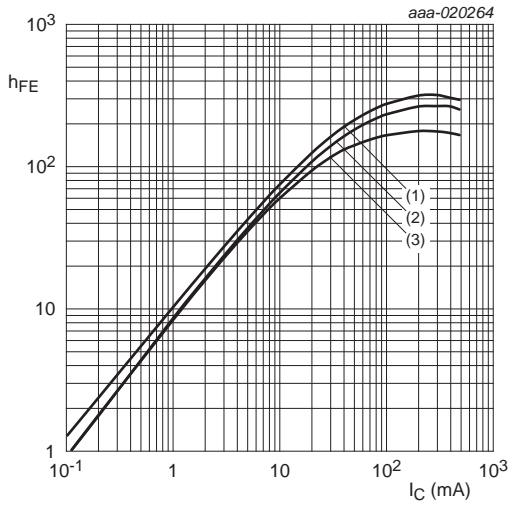
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 17. PDTD123EQA: Collector-emitter saturation voltage as a function of collector current; typical values



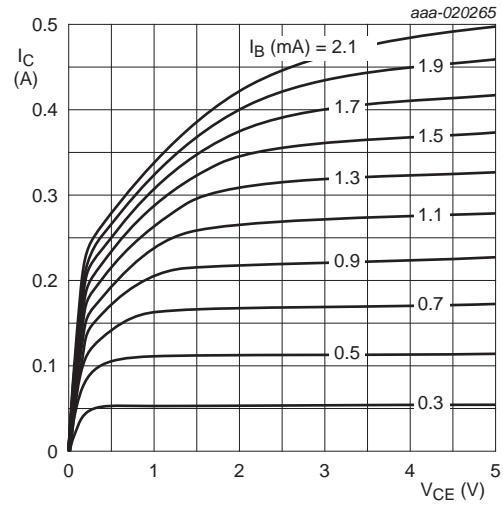
$f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$

Fig 18. PDTD123EQA: Collector capacitance as a function of collector-base voltage; typical values



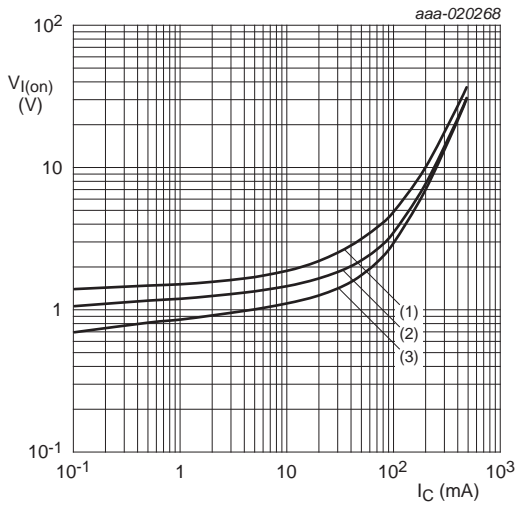
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 19. PDTD143EQA: DC current gain as a function of collector current; typical values



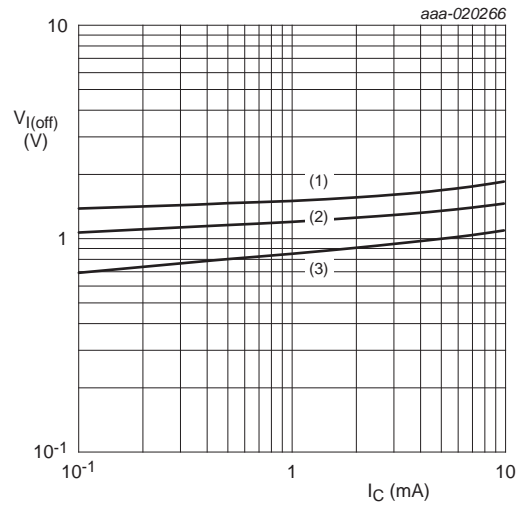
$T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 20. PDTD143EQA: Collector current as a function of collector-emitter voltage; typical values



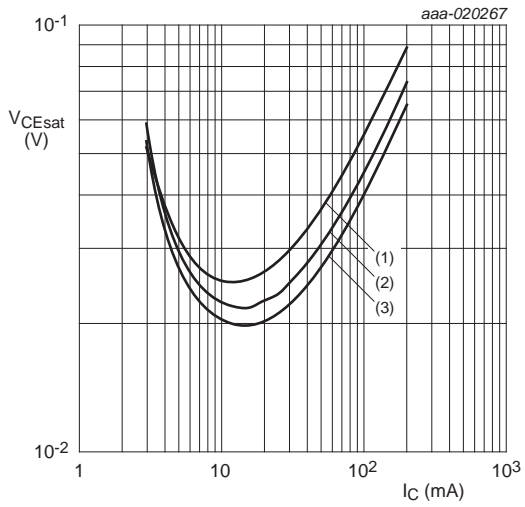
$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 21. PDTD143EQA: On-state input voltage as a function of collector current; typical values



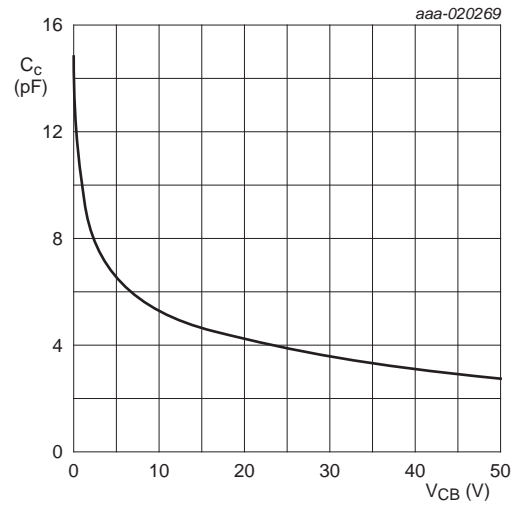
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 22. PDTD143EQA: Off-state input voltage as a function of collector current; typical values



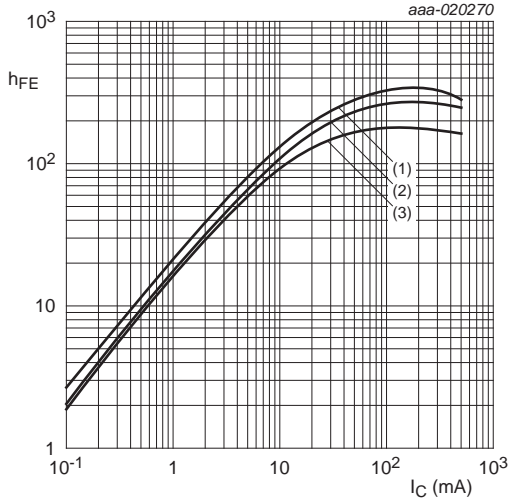
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 - (3) $T_{amb} = -40\text{ }^\circ\text{C}$

Fig 23. PDTD143EQA: Collector-emitter saturation voltage as a function of collector current; typical values



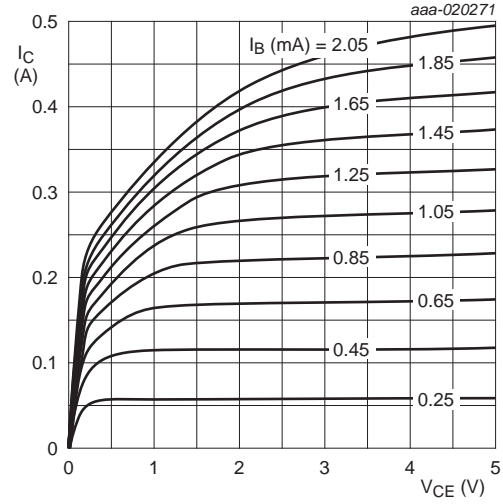
$f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$

Fig 24. PDTD143EQA: Collector capacitance as a function of collector-base voltage; typical values



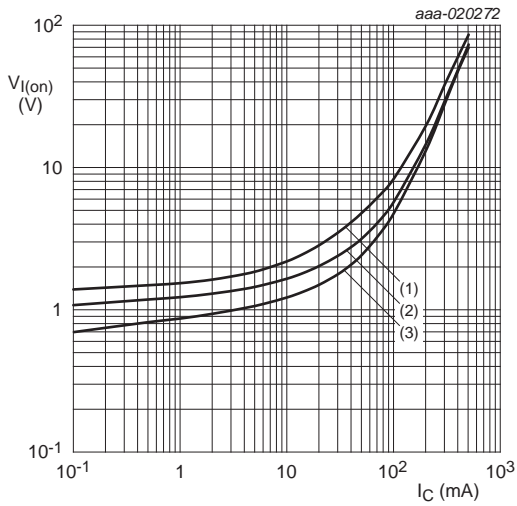
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 25. PDTD114EQA: DC current gain as a function of collector current; typical values



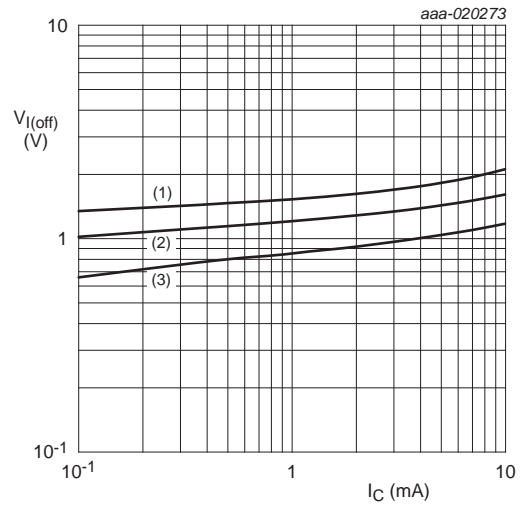
$T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 26. PDTD114EQA: Collector current as a function of collector-emitter voltage; typical values



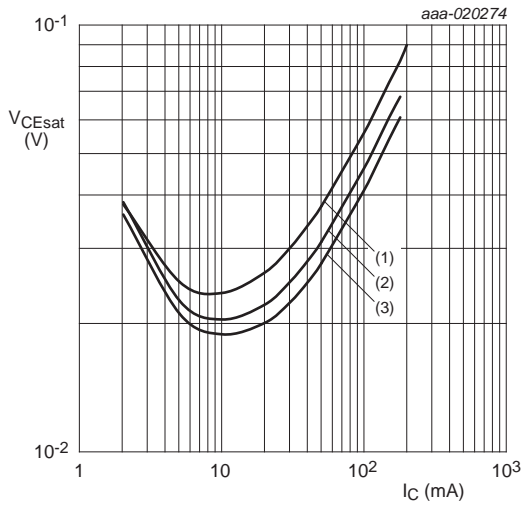
$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 27. PDTD114EQA: On-state input voltage as a function of collector current; typical values



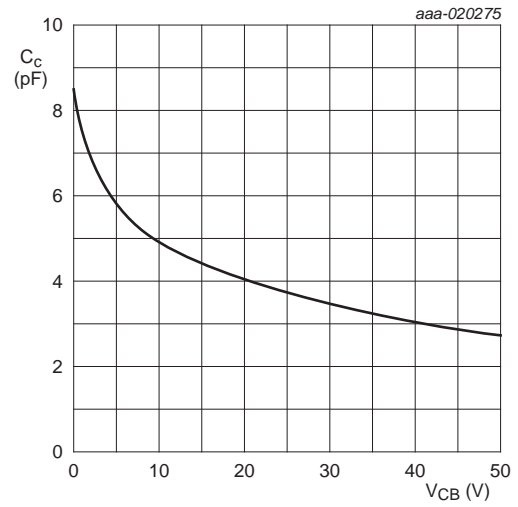
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 28. PDTD114EQA: Off-state input voltage as a function of collector current; typical values



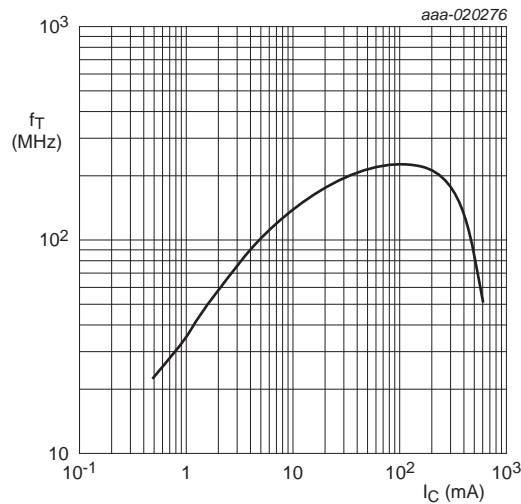
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 29. PDTD114EQA: Collector-emitter saturation voltage as a function of collector current; typical values



$f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$

Fig 30. PDTD114EQA: Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5\text{ V}; f = 100\text{ MHz}; T_{amb} = 25\text{ °C}$

Fig 31. Transition frequency as a function of collector current; typical values of built-in transistor

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

8.2 Resistor calculation

- Calculation of bias resistor 1 (R1):

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation method A of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_{I3})}{R1 \cdot I_{I3}} - 1$$

- Calculation method B of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

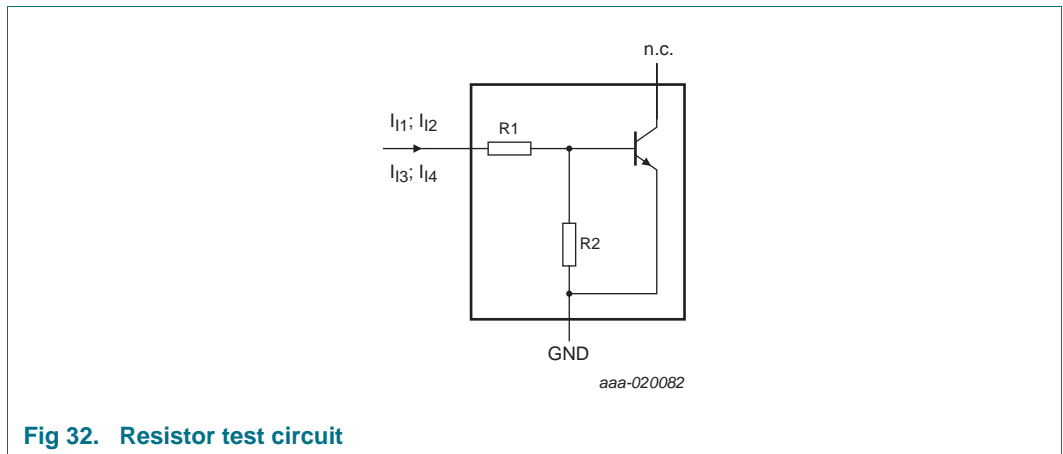


Fig 32. Resistor test circuit

8.3 Resistor test conditions

Table 9. Resistor test conditions

Type number	R1 kΩ	R2 kΩ	Test conditions			
			I _{I1}	I _{I2}	I _{I3}	I _{I4}
PDTD113EQA [1]	1	1	1.5 mA	1.9 mA	-2.2 mA	-
PDTD123EQA [1]	2.2	2.2	0.7 mA	0.8 mA	-0.75 mA	-
PDTD143EQA [2]	4.7	4.7	1.3 mA	1.5 mA	-1.05 mA	-1.25 mA
PDTD114EQA [2]	10	10	0.7 mA	0.8 mA	-0.45 mA	-0.55 mA

[1] Uses calculation method A of bias resistor ratio R2/R1

[2] Uses calculation method B of bias resistor ratio R2/R1

9. Package outline

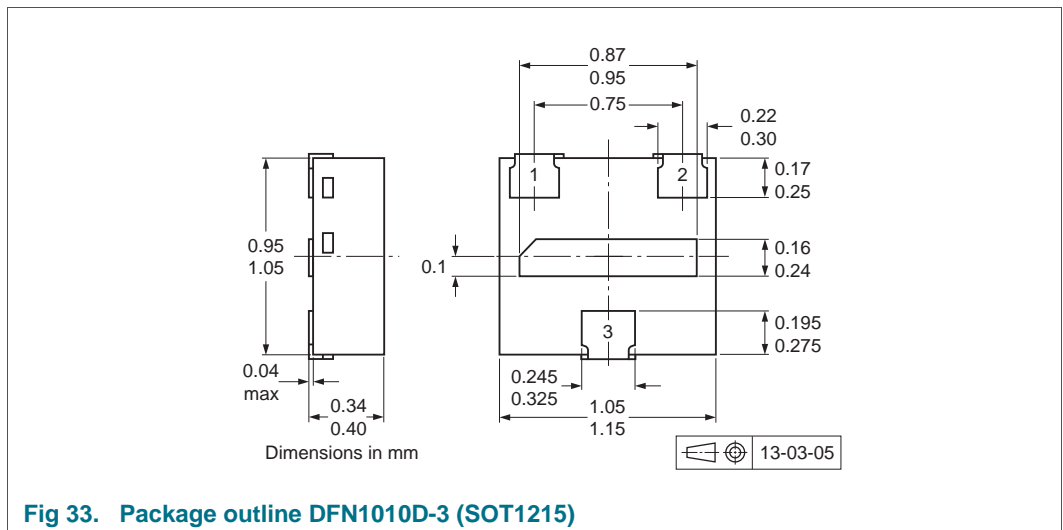


Fig 33. Package outline DFN1010D-3 (SOT1215)

10. Soldering

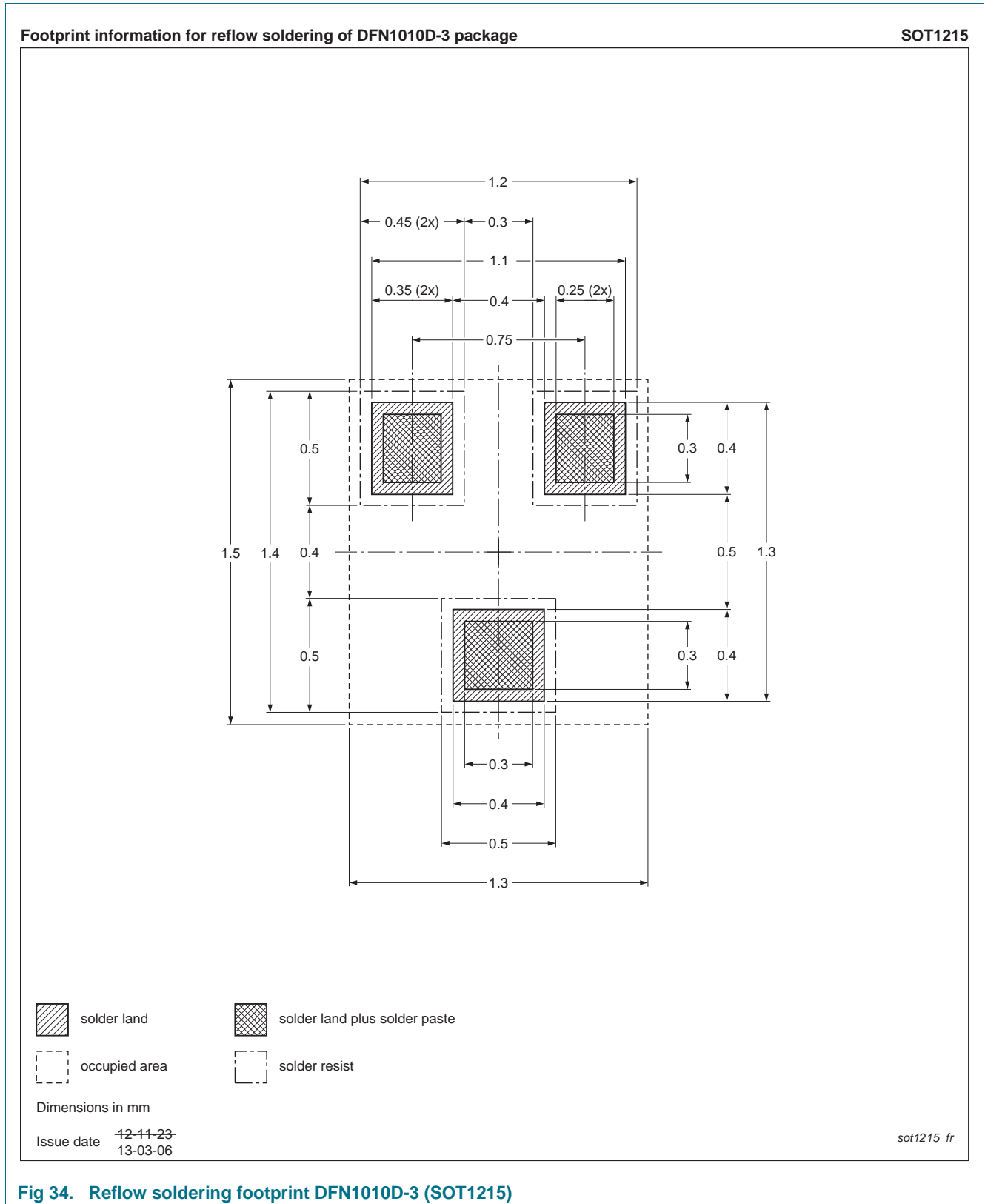


Fig 34. Reflow soldering footprint DFN1010D-3 (SOT1215)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTD113_123_143_114EQA_SER v.1	20160104	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1 Product profile 1

1.1 General description 1

1.2 Features and benefits 1

1.3 Applications 1

1.4 Quick reference data 1

2 Pinning information 2

3 Ordering information 2

4 Marking 3

4.1 Binary marking code description 3

5 Limiting values 3

6 Thermal characteristics 5

7 Characteristics 8

8 Test information 15

8.1 Quality information 15

8.2 Resistor calculation 15

8.3 Resistor test conditions 15

9 Package outline 16

10 Soldering 17

11 Revision history 18

12 Legal information 19

12.1 Data sheet status 19

12.2 Definitions 19

12.3 Disclaimers 19

12.4 Trademarks 20

13 Contact information 20

14 Contents 21

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016. All rights reserved.

For more information, please visit: <http://www.nxp.com>
 For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 February 2016
 Document identifier: PDTD113_123_143_114EQA_SER