PE12016G / PE12024G

Incremental Encoder

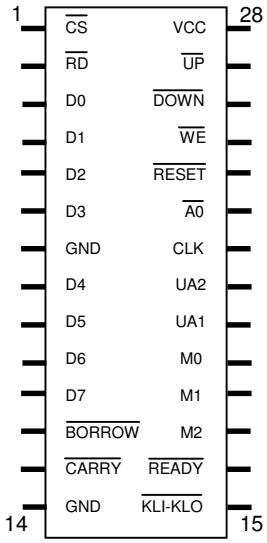
Productivity Engineering
Gesellschaft für Prozessintegration mbH

December 15, 2005 Version 1.7

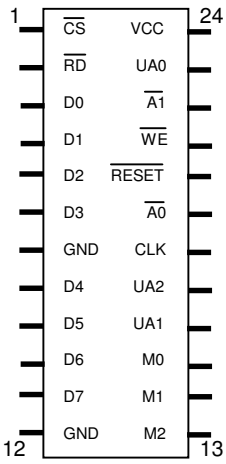
Features:

- Functional and pincompatible with obsolete TI CF32007NW/NT / THCT12016 / THCT 12024 / LS2000
- 5 V and 3.3 V Operation
- 0.6u CMOS Process
- Direction discriminator
- Pulse width measurement
- Frequency measurement
- Cascadable (PE12016G only)
- TTL compatible
- 8 Bit parallel tristateable Bus
- Simple read & write procedure
- High speed 20 MHz clock operation
- PE12016G ONLY: 1:1 Replacement for LS2000AN
- PE12024G ONLY: 24-Bit resolution, separate UA0 counter reset
- WEEE & RoHS Compliant according DIRECTIVE 2002/95/EC (Green Package Material)

PE12016G
PDIP28-600 Mil



PE12024G
PDIP24-300 Mil



Description:

The PE12016G/12024G INCREMENTAL ENCODER INTERFACE can independently determine the direction or displacement of a mechanical device or axis based on two input signals from transducers in quadrature. Alternatively, it can measure a pulse width using a known clock rate, or a frequency, by counting input pulses over a known time interval. It includes one 16-bit or 24-bit counter which may also be used separately (PE12016G only). The PE12016G may be cascaded to provide accuracy greater than 16-bits. Both devices are designed for use in many microprocessor-based systems.

Availability:

The PE12016G/24G is available as replacement IC or Netlist IP Core, fully compatible with the obsolete TI CF32007NW/NT functionality. The replacement IC is packaged within the popular PDIP28-600 Mil (PE12016G) and the PDIP24-300 Mil package (PE12024G).

The IP Core can be targeted to any desired FPGA/CPLD or ASIC Technology and is delivered within the according netlist format. The database has been proven in a co-emulation together with the reference part by stimulating both devices with the same inputs and observing the identical results on the outputs.

Ressource Usage IP Core:

Gate count for ASIC Technologies is 1700 Gates.

For CPLDs 128 Macrocells are needed, resulting in a Xilinx XC95144 CPLD

Differences:

The PE12016G/24G has some minor enhancements. UA1 and UA2 are synchronized with the clock, eliminating the need to place a discrete ACT74 type Flipflop in front of these signals. Due to this feature a latency of one clock cycle is introduced, resulting worst case in a +/-1 counter difference.

The output driver capability is slightly decreased. Pullups are on the following pins: /A1, /UP, /DOWN and /KLI-KLO. UA0 has a Pulldown. The value is approximately 75 kOhm. For further details refer to the application notes at the end of this datasheet.

Applications:

The PE12016G/12024G enables mechanical devices to be interlaced with micro-processors. It may be used in many diverse applications, including robotics, printers/plotters, tracker balls (or mouse), lathes and machine tools, automobiles, conveyor belts and transport mechanisms.

Architecture:

The four main elements of the PE12016G are shown in Fig 2:

1. The measurement and mode control logic generates up or down count pulses, internal signals (I1 and I2) from the quadrature signals Ua1 and Ua2, the clock input and from Mode Controls (M0, M1, M2).
2. The control logic provides common microprocessor interface signals.
3. The output multiplexer allows the processor to select data from either the upper (MS-byte) or the lower (LS-byte)
4. The 3-state buffers place this data on the bus

The PE12024G-architecture, shown in ***Figure: 3***, is very similar to that of the PE12016G, except for the up/down counter which has 24-bits and can be independently reset by Ua0. The cascading feature has also been removed.

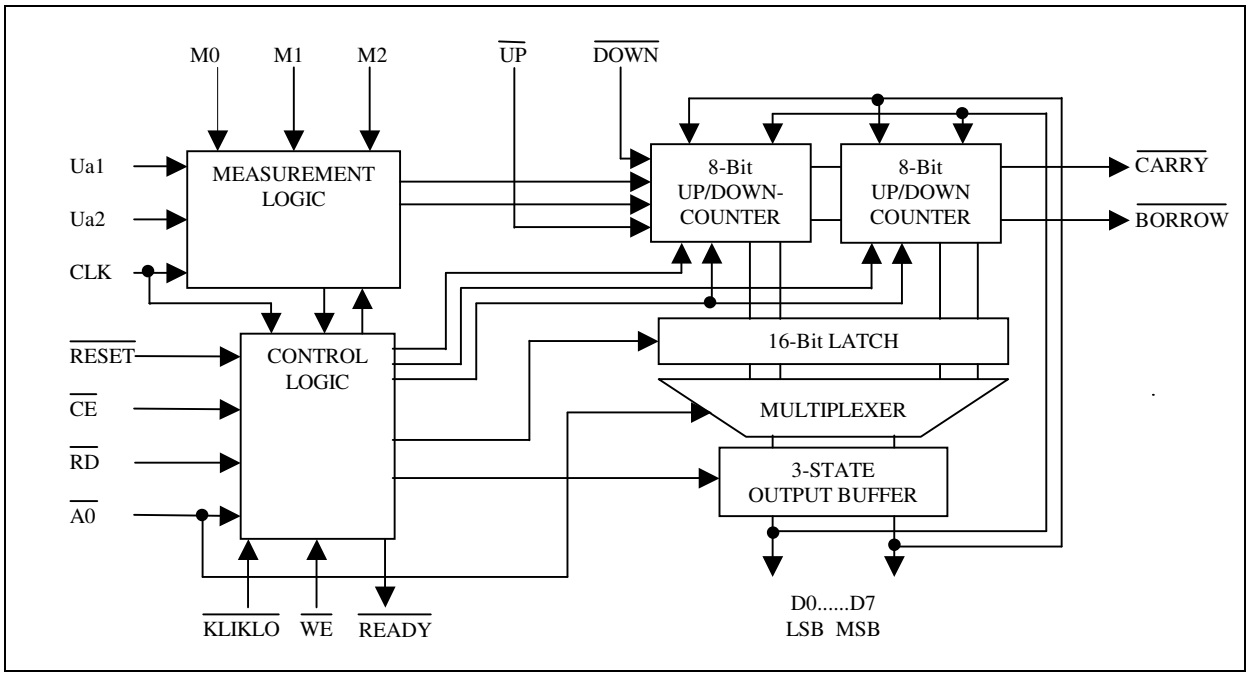


Fig. 1: PE 12016G Block Diagram

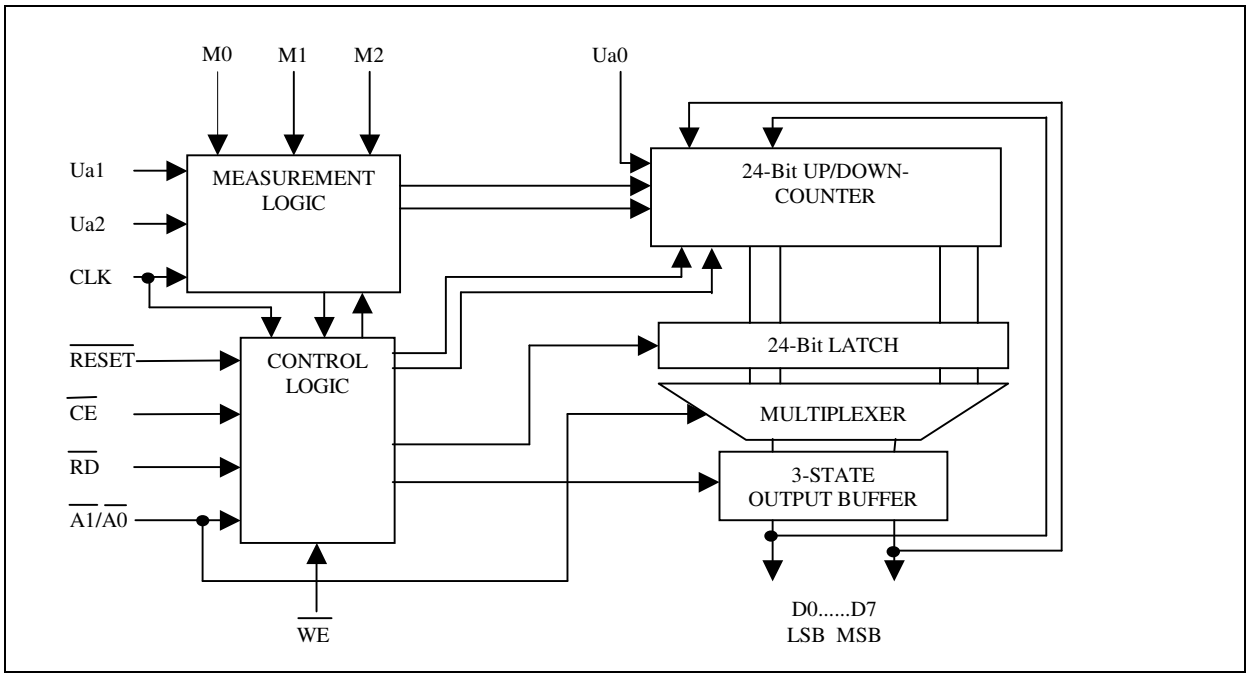


Fig. 2: PE12024G Block Diagram

Operation:

The eight modes of operation of the PE12016G/12024G are summarized in ***Table 1***.

Mode	M2	M1	M0	Mode Description
0	0	0	0	**COUNTER** 16-bit (PE12016G only) up/down counter (inhibits direction discriminator)
1	0	0	1	**DIRECTION DISCRIMINATOR** Single count pulse synchronous with Ua1 rising in forward direction and Ua1 falling in backward direction.
2	0	1	0	Single count pulse synchronous with Ua2 rising in forward direction and Ua2 falling in backward direction.
3	0	1	1	Double count pulse synchronous with Ua1 rising and falling.
4	1	0	0	Double count pulse synchronous with Ua2 rising and falling.
5	1	0	1	Quadruple count pulse synchronous with all edges.
6	1	1	0	**PULSE WIDTH MEASUREMENT** Ua1 is the gate signal Ua2 is high for up counting and low for down counting. Count is synchronous with rising clock.
7	1	1	1	**FREQUENCY MEASUREMENT** Ua1 is frequency signal to be measured Ua2 is the gate signal of known time interval. Count is synchronous with rising edge of Ua1.

Table 1: PE12016G/12024G Operation Modes

Detailed Information about the different Modes:

Mode 0: 16-Bit Up/Down Counter Mode

In this mode the PE12016G may be used as a fast 16-bit up/down counter with cascade capability. This is operated using the /UP and /DOWN inputs.

The states of the counter outputs are transferred to a 16-bit latch. The contents of this 16-bit latch are multiplexed on a 8-bit parallel data bus (D0…D7) and enabled using /RD and /CS.

/A0 is the control input for the byte multiplexer. A high level at this input transfers the least significant byte to the data outputs; and a low level transfers the most significant byte.

The up/down counters are loaded in individual 8-bit bytes by the /WR and /CS signals, with the byte selected by the /A0 input. The counter may be cleared using the /RESET signals (which clears both counter and control logic), or individually, using Ua0 signal (PE12024G) only.

Cascading to n-bits is possible using inputs /UP and /DOWN, outputs /BORROW, /CARRY and the input-outputs /KLI-KLO (PE12016G only).

NOTE: The PE12024G cannot be used in Mode 0 since /UP and /DOWN inputs are not available.

To read or load the 24-bit (PE12024G only) in all modes, /CS, /RD or /WR, /A0 and /A1 are used to perform the Read or Write operation. The operation should always start with the LSB (/A0=/A1=HIGH), followed by the LSB+1 (/A0=LOW, /A1=HIGH) and then the MSB (/A0=HIGH, /A1=LOW).

/A0	/A1	BYTE	REMARKS ON D0-D7
H L	H H	LSB LSB+1	PE12016G only
H L	L L	MSB ALL X	PE12024G extensions

Table 2: PE12024G Address Select

Mode 1-5 : Direction Discriminator Modes

The quadrature signals Ua1 and Ua2 identify forward or backward directions. If Ua1 leads Ua2, the forward direction is indicated and the counter will count up; if Ua1 lags Ua2, the reverse direction is indicated and the counter will count down.

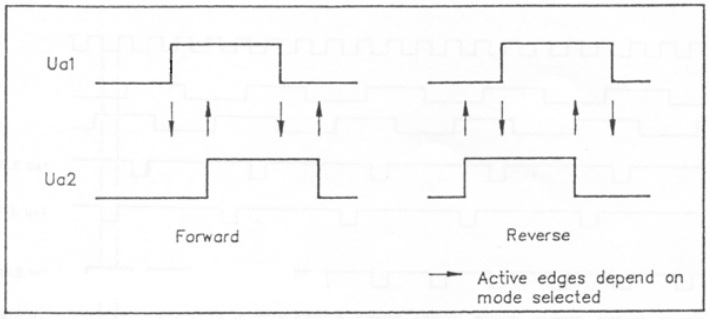


Fig. 3: Direction Discriminator Modes

Both Ua1 and Ua2 are stored on the clock falling edge in the first of a pair of consecutive D-type flip-flops, and are transferred to the next on the clock rising edge. By comparing the states of the four flip-flops and checking the mode inputs, the up or down count pulses are generated; see ***Figures 4*** and ***5***.

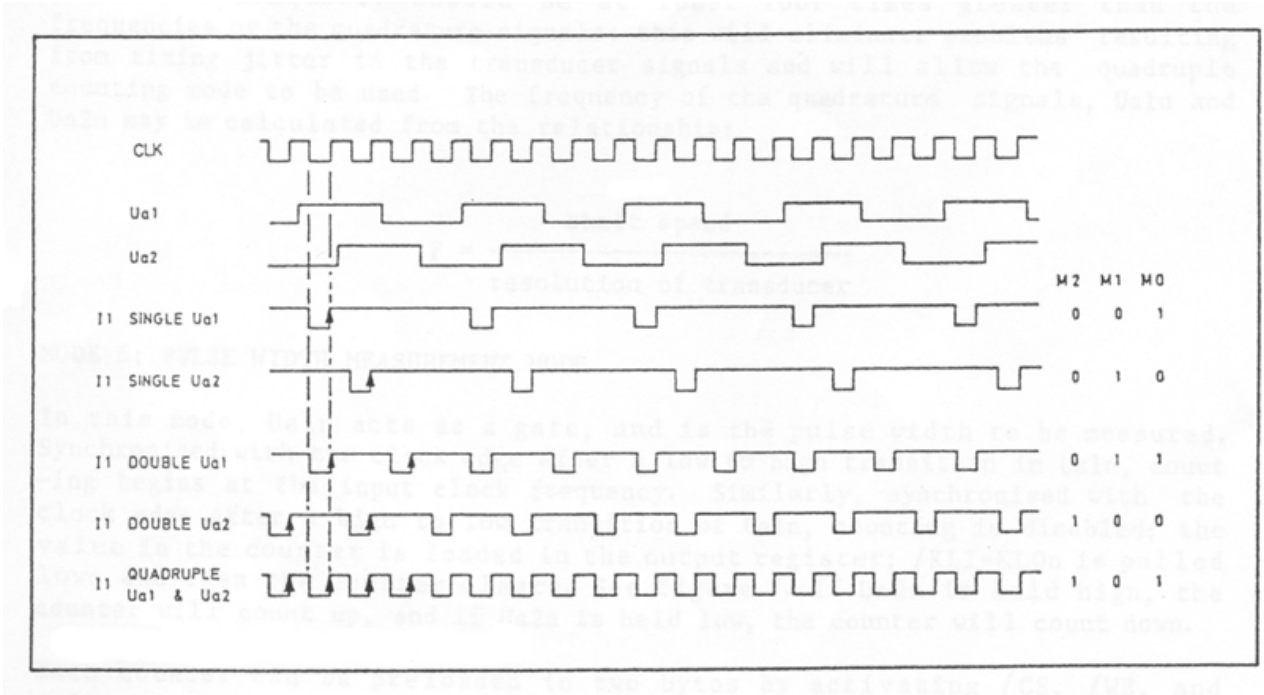


Fig. 4: Direction Discriminator Up Clock

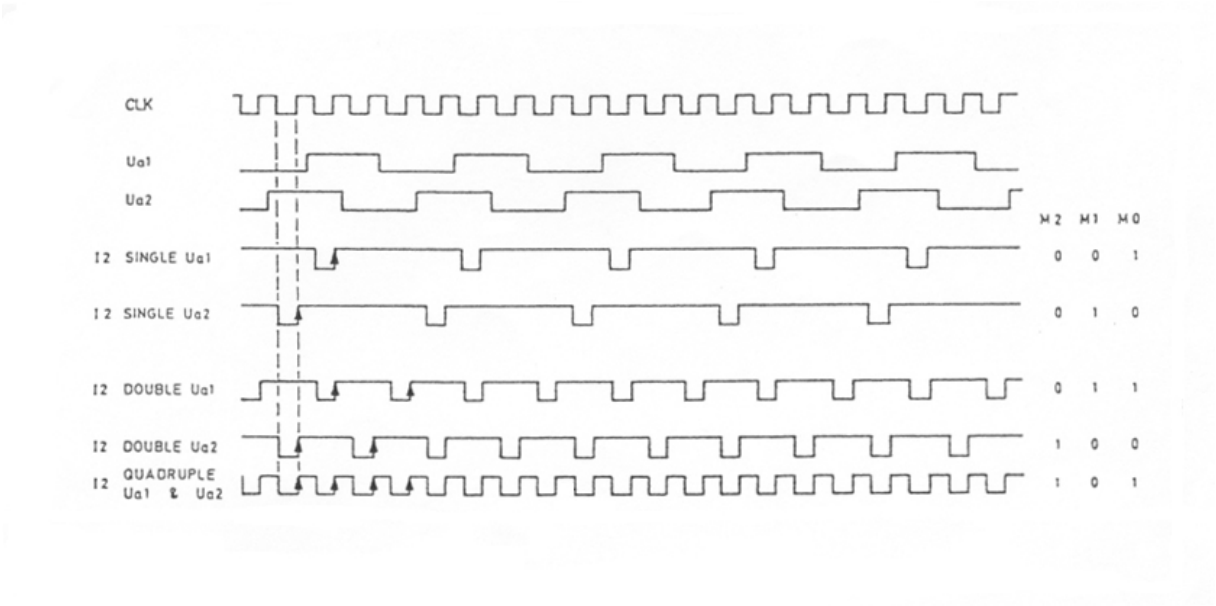


Fig. 5: Direction Discriminator Down Clock

MODES 1 to 5 define which edge of the quadrature signals will be counted in accordance with ***Table 1***.

The clock frequency should be at least four times greater than the frequencies of the quadrature signals: this will eliminate problems resulting from timing jitter in the transducer signals and will allow the quadruple counting mode to be used. The frequency of the quadrature signals, Ua1 and Ua2 may be calculated from the relationship:

$$F = \frac{shaft\_speed}{resolution\_of\_transducer}$$

MODE 6: Pulse Width Measurement Mode

In this mode, Ua1 acts as a gate, and is the pulse width to be measured. Synchronised with the clock edge after a low to high transition in Ua1, counting begins at the input clock frequency. Similarly, synchronised with the clock edge after a high to low transition of Ua1, counting is disabled. The value in the counter is loaded in the output register, /KLI-KLO (PE12016G only) is pulled low and then the counter clears. See ***Figure 7***. If Ua2 is held high, the counter will count up, and if Ua2 is held low, the counter will count down.

Each counter can be preloaded in two or three bytes (PE12024G only) by activating /CS, and /WE, and selecting the individual bytes with /A0, and/or /A1 after Ua1 has fallen and before the next preload takes place.
The KLI-KLO signal (PE12016G only) may be used as an interrupt to indicate to the processor when the output register has been loaded. In the pulse width mode, the output register will not be loaded via /CS and /RD, but by the falling edge of Ua1.

In pulse width mode, the minimum time that can be measured is:
Tmin = 2 (To) (Accuracy is +/- To)

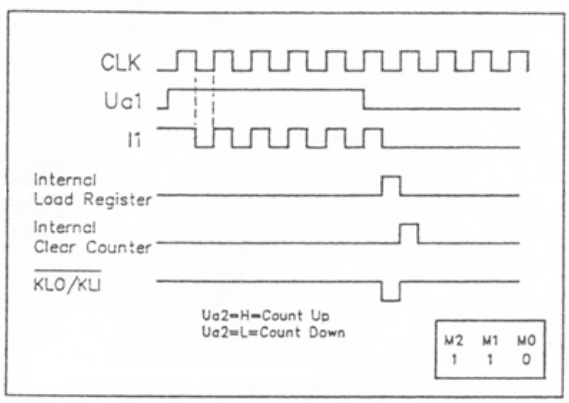


Fig. 6: Pulse Width Measurement

MODE 7: Frequency Measurement Mode

In Mode 7, Ua1 is the signal of unknown frequency to be measured; Ua2 is a gate signal of known width. A low to high transition of Ua2 enables counting at the frequency of Ua1. When the gate (Ua2) goes low, counting is disabled. The value of the counter is loaded into the output register, /KLI-KLO is pulled low (PE12016G only), and the counter is then cleared. See ***Figure 8***.

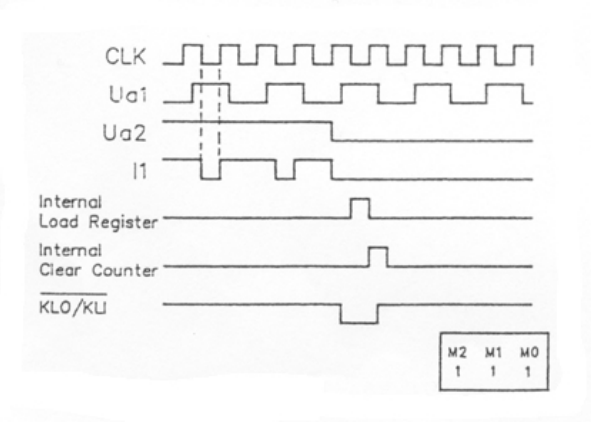


Fig. 7: Frequency Measurement

Reset Operation:

A total reset is initiated by pulling the /RESET pin low. This will clear the counters to zero, reset the D flip-flops at the inputs of the quadrature signals (Ua1 and Ua2), clear the latches that inhibit the load register pulse, and load zero into the register.

To avoid a spurious count error (+/- 1) after a reset, the Ua1 and Ua2 inputs should be held to the values indicated in ***Table 3*** during and just after the reset pulse.

MODE	Ua1	Ua2
0	X	X
1-5	H	H
6-7	L	L

Table 3: Ua1 and Ua2 levels during reset operations

NOTE:
If a /RESET=LOW appears during a read or write cycle of the PE12016G, the /READY output will stay LOW as long /RESET is active.

Cascading Devices (PE12016G only)

The /KLI-KLO pins of all cascaded PE12016G's should be tied together, so that all of the devices load their output registers at the same time. When the 'Master' generates a pulse for the other PE12016Gs, /KLI-KLO on the 'Master' works as an output, and /KLI-KLO on the 'Slaves' work as inputs. The /CARRY output of one device should be tied to the /UP input of the next device in the cascade. Similarly, /BORROW should be connected to /DOWN.

Write Operation

A number may be preloaded into the counter by pulling /CS and /WE low while using /A0 /A1* (/A1* PE12024G only) to direct the value on the data bus to the selected byte of the counter. This will cause /READY (PE12016G only) to go low on the next falling clock edge, and remain low until /CS or /WE goes high. See ***Figure 10***.

Read Operation

When in Modes 0 to 5 the contents of the counter can be read at any time by pulling /CS and /RD low. The most significant byte may be selected by setting /A0 low, and the least significant byte may be read by setting /A0 high (PE12016G only, for PE12024G – see ***Table 2***). This will cause a 'load output register' pulse to be generated and /KLI-KLOn will go low during the next low clock pulse. /READY (PE12016G only) will also go low as the clock goes low, and will stay low until /CS and/or /RD go high. The load output register pulse stores the current value of the counter in a 16-bit or 24-bit latch register: /A0 and /A1 (PE12024G only) direct the selected byte through a multiplexer to the outputs : /CS and /RD also enable the 3-stat outputs – see ***Figure 9***.

The output register will be loaded immediately if /KLI-KLO (PE12016G only) is pulled low externally; this signal normally comes from a cascaded device.

For Modes 6 & 7 see the earlier description of these modes.

Configuration

Special consideration should be paid to the automatic configuration features of the PE12016G/12024G. The purpose of these features is to allow for the different order of byte reads (high then low or low then high) of different processors when doing a word read across a byte wide bus and also to automatically configure when devices are cascaded.

Byte Order Configuration

After a system reset has occurred, the first read operation will store the value of /A0 /A1 into a latch within the device. From that time until the next system reset the load output register pulse will only be generated during a read operation if /A0 /A1 is at this stored value.

This means that the internal load output register pulse is correctly generated for word operations regardless of the byte order of the particular processor. Special care should be taken when reading individual bytes to ensure that these operations are always done in a consistent order.

Cascaded configuration (PE12016G only)

After a system reset the first device and channel to receive a read operation (/RD and /CS = LOW) configures itself into 'Master' mode and outputs a pulse on /KLI-KLO. In cascaded operation the /KLI-KLO pins of the cascaded channels are connected together and the input pulse on /KLI-KLO of the cascaded channels configures these to 'Slave' mode. On all subsequent read operations the load output register pulse is only generated by the 'Master' channel (for the appropriate polarity of /A0 and /A1 (PE12024G only), as noted above) and this is fed to the 'Slave' devices via the /KLI-KLO connection.

Special care must be taken when cascading devices or channels to always read in the same channel order, as well as the byte order already mentioned - **see also Systems Application.**

Pin Description

Pin Name	Pin Number			I/O	Description
	PDIP28 PE12016G	PDIP24 PE12024G			
/CS	1	1		Input	Chip Select. A low enables the device.
/RD	2	2		Input	Read. When this and /CS are active (low), the data from the output register will be present on the data bus.
D0 D1 D2 D3 D4 D5 D6 D7	3 4 5 6 8 9 10 11	3 4 5 6 8 9 10 11		Input/ Output (3-state)	LSB Data Bus Buffer: 8-Bit bidirectional Buffer with 3-state outputs connected to the microprocessor system. MSB
/BORROW	12	-		Output (PP)	Push-pull output of the Counter underflow signal (PE12016G only).
/CARRY	13	-		Output (PP)	Counter overflow signal (PE12016G only)
/KLI-KLO	15	-		Input/ Output (OD with Pull-up)	Cascade load input / cascade load output. Open drain (OD) output with internal 75KΩ (nom) pull-up. (PE12016G only)
/READY	16	-		Output (PP)	When active low, the signal indicates to the MPU that read or write may be completed. /READY falling edge is synchronous with CLK. The push pull output requires no external pull-up resistor (PE12016G only).
M2 M1 M0	17 18 19	13 14 15		Input Input Input	Mode Select Inputs (see ***Table 1***)
Ua1 Ua2	20 21	16 17		Input Input	Measuring input signals

Pin Description - continued

Pin Name	Pin Number			I/O	Description
	PDIP28 PE12016G	PDIP24 PE12024G			
Ua0	-	23		Input	Reset input for the 24-bit counter (PE12024G only)
CLK	22	18		Input	Clock. Used for internal synchronisation and control timing.
/A0	23	19		Input	Byte select. A high level selects the least significant byte. /A1=1 with PE12024G A low level selects the most significant byte (/A1=High with the PE12024G) – see ***Table 2***.
/A1	-	22		Input	Byte select. A low level with /A0=High selects the MS-byte (Bits 16-23) on the PE12024G
/RESET	24	20		Input	Device Reset. When active (low), the control logic is reset to a known state and the counter is cleared.
/WE	25	21		Input	Write enable. When /WE and /CS are active (low), the data that is on the bus is loaded into the counter.
/DOWN	26	-		Input	Cascade Input for counting down. (PE12016G only)
/UP	27	-		Input	Cascade Input for counting up. (PE12016G only)
Vcc	28	24			Power Supply voltage
GND	7, 14	7, 12			Ground

Operating Conditions

Absolute Maximum Ratings over operating free air temperature:

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	-0.3 to + 7.0	V
V_{IN}	DC Input Voltage	-0.3 to V_{CC} + 0.3	V
I_{IN}	DC Input Current	+/- 10	mA
Storage Temperature (Plastic Package)		-40 to +125	℃

DC Characteristics (referred to GND):

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{OH} All except, /READY and /KLI-KLO	Output High Level	I_{OH} = -20 uA	V_{CC}-0.1			V
V_{OH} D0-D7		I_{OH} = -12 mA, V_{CC} = 5.0V	2.4			V
V_{OH} All except D0-D7, /READY and /KLI-KLO		I_{OH} = -6 mA, V_{CC} = 3.3V	2.4			V
V_{OL}	Output Low Level	I_{OH} = 20 uA			0.1	V
V_{IH}	Input High Level	TTL Schmitt Trigger	2.0 2.4			V
V_{IL}	Input Low Level				0.5	V
I_{CC}	Supply current	20 MHz V_{CC}=Max		10		mA
VT+	Schmitt Trigger positive going threshold	V_{CC} = Min to Max			2.4	V
VT-	Schmitt Trigger negative going threshold	V_{CC} = Min to Max			0.5	V
V_{HYS}	Schmitt Trigger Hysteresis	V_{CC} = Min to Max	0.2			V
I_{OZ}	Tristate Output Leakage Current	V_{CC} = Max or GND	-10		+10	uA
I_{IH}	Input High current	V_{IN} = V_{CC}	-10		+10	uA
	Input with pullup		-200		-10	uA
I_{IL}	Input Low current	V_{IN} = GND	-10		+10	uA

Recommended Operating Conditions:

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	4.5 to 5.5	V
V_{CC}	DC Supply Voltage (Low Power Application)	3.0 to 3.6	V
T_{AC}	Temperature Range	0 to +70	℃

Timing Requirements over Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Units
Tc1	CLK Cycle Time, duty cycle 50%	50			ns
Tc2	Pulse width low CLK Tr, Tf<5ns	25			ns
Twrs	Pulse width, /RESET input low	50			ns
fmud	Maximum frequency, /UP or /DOWN, Input duty cycle 50% (PE12016G only)	20	25		MHz
Twud	Pulse width, /UP or /DOWN input low (PE12016G only)	25			ns
Twk	Pulse width, /KLI-KLO input low (PE12016G only)	20			ns
Twrd1	Pulse width, /RD input low (Mode = 6 & 7)				ns
Twrd2	Pulse width, /RD input low (Mode = 0 to 5)		Tc1		ns
Tdrd	Time between two or three* Read cycles (LSB or LSB+1* and MSB)	0			ns
Twwr	Pulse width, /WE input low	25			ns
Tdwr	Time between two or three* Write cycles (LSB or LSB+1* and MSB)	0			ns
Tsd	Set up time, DATA prior to ↑/WE	15			ns
Twua0	Pulse width, Ua0 input high*	25			
Tsus	Set up time, /CS and /RD low before CLK falling edge	15			ns
Tsa	Set up time, /A0, /A1* prior to /WE and /CS low	10			ns
Tsud	Set up time, /UP or /DOWN rising edge before CLK falling edge (PE12016G only)	20			ns
Tsab	Set up time, Ua1 or Ua2 prior to CLK falling edge.	15			ns
Tsda	Set up time, DATA prior to ↑/WE	Tsd			ns
Tsbb	Set up time, Ua2 stable before CLK falling edge	15			ns
Tsac	Set up time, Ua1 or Ua2 rising edge before CLK falling edge.	15			ns
Tsar	Set up time, /A0, /A1* stable before /CS and /RD low after reset	10			ns
Tsbc	Set up time, Ua1 or Ua2 falling edge	15			ns
Tsr	Set up time, /RESET high prior to CLK falling edge.	0			ns
Tsuc	Set up time, /UP or /DOWN rising edge prior to /KLI-KLO (input) falling edge (PE12016G only).	20			ns

Timing Requirements over Recommended Operating Conditions - continued

Symbol	Parameter	MIN	TYP	MAX	Units
Thdw	Hold time DATA after ↑/WE	10			ns
Twgp	Pulse width, Ua1 input high (Mode = 6)	Min 2 x Tc1			ns
Twgp	Pulse width, Ua2 input high (Mode = 7)	Min 2 x Tc1			ns
Tdgp	Pulse width, Ua1 input low (Mode = 6)	Min 2 x Tc1			ns
Tdgf	Pulse width, Ua2 input low (Mode = 7)	Min 2 x Tc1			ns
Tha	Address hold time after /WE or /CS high	12			ns
Thab	Ua1 or Ua2 hold time after CLK falling edge	12			ns
Thda	D0-D7 hold time after /A0 or /A1* change	10			ns
Thac	Ua1 high hold time after CLK falling edge	12			ns
Thbc	Ua2 hold time after CLK falling edge	12			ns
Twrh	Pulse width, Ua0 input high	5			ns

* PE12024G only

Switching Characteristics, (Vcc=Min, Temperature +70 Degrees)

Symbol	Parameter	Test Conditions See appendix A (test pattern)	MIN	TYP	MAX	Units
Tdd1	Access time, /RD and CLK to data output valid (Mode = 0 to 5)				65	ns
Tdd2	Access time, /RD to data output valid Mode = 0 to 5 2nd byte or 3rd byte* Mode = 6 to 7 both bytes, or all three bytes (PE12024G only)				45	ns
Thr	Propagation delay /RD, /WE or /CS inactive to /READY (PE12016G only)	From CS ↑			20	ns
Tdr	Propagation delay CLK ↓ to /READY low (PE12016G only)				30	ns
Tduc	Propagation delay /UP or /DOWN rising edge to /CARRY or /BORROW rising edge (PE12016G only)	From /UP ↑ to /CARRY ↑			35	ns
Tdcc	Propagation delay from CLK to /CARRY or /BORROW rising edge (PE12016G only)	From /CLK ↑ to /CARRY ↑ or from /CLK ↑ to /BORROW ↑			25	ns
Tdco	Propagation delay CLK falling edge to /KLI-KLO falling edge (PE12016G only)				55	ns
Tdcb	Propagation delay CLK rising edge to /CARRY or /BORROW rising edge (PE12016G only)	From /CLK ↑ to /CARRY ↑ or /BORROW ↑			25	ns
Ted	Enable Time /RD and /CS low to D0-D7				65	ns
Twco	/KLI-KLO low output pulse width (PE12016G only)			Tc2		ns
Twcb	/CARRY or /BORROW low output pulse width (PE12016G only)			Twud		ns
Twcc	/CARRY or /BORROW low output pulse width (PE12016G only)			Tc2		ns
Thdr	Release time, DATA after /RD, /CS	From /CS ↑ DATA $>01_{16}$ → ZZ_{16}	0		45	ns

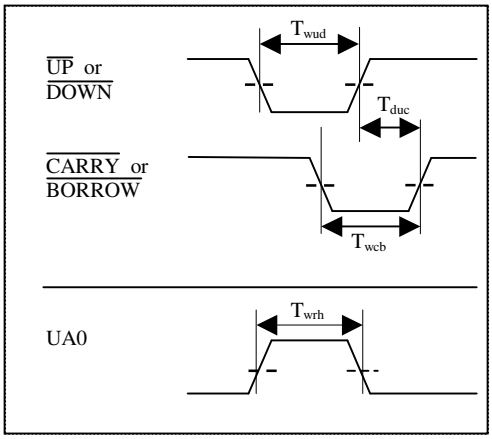


Fig. 8: Timing – Mode 0

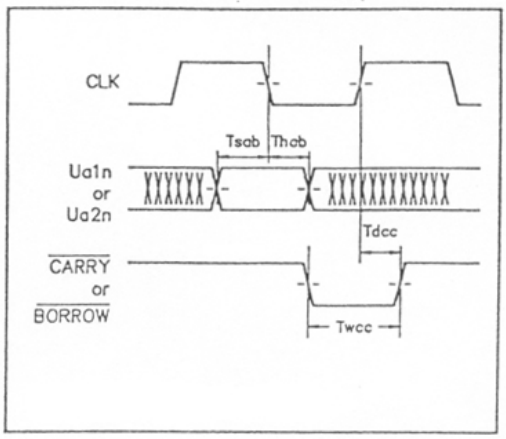


Fig. 9: Timing – Mode 1 - 5

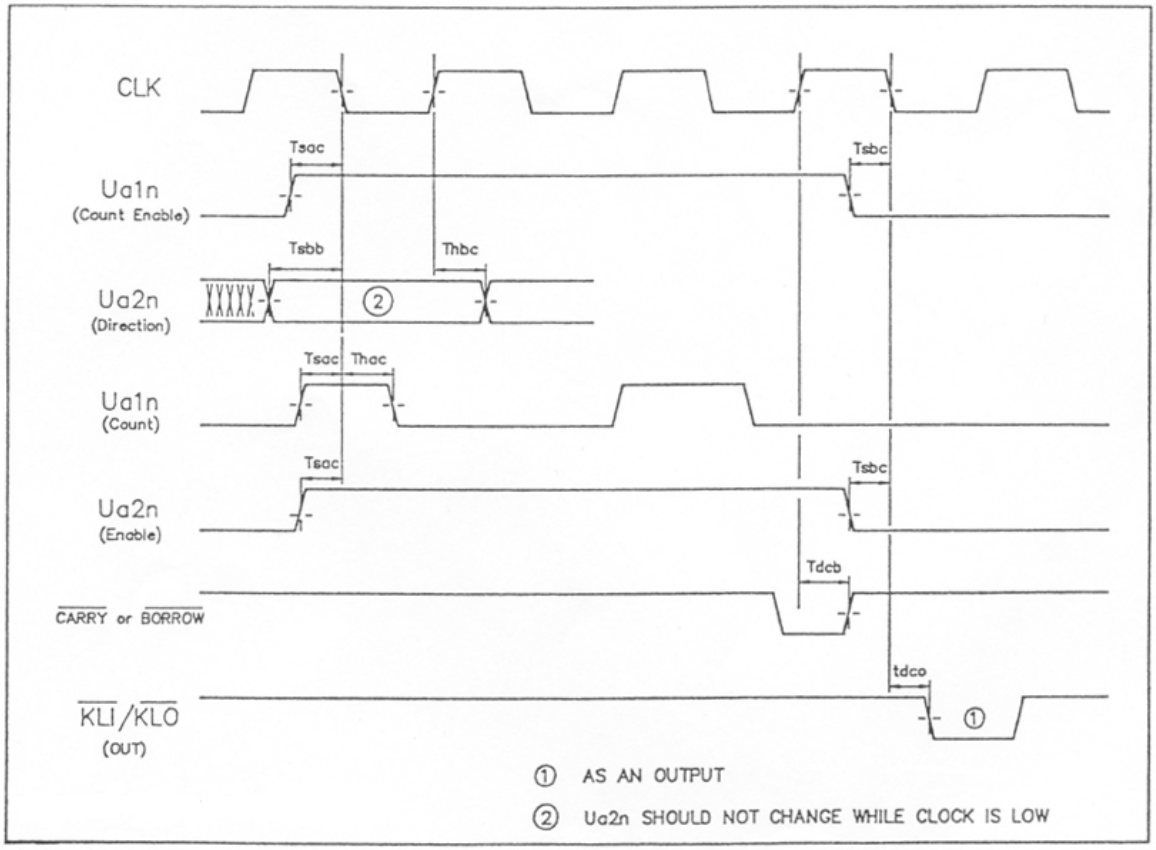


Fig. 10: Timing – Mode 6-7

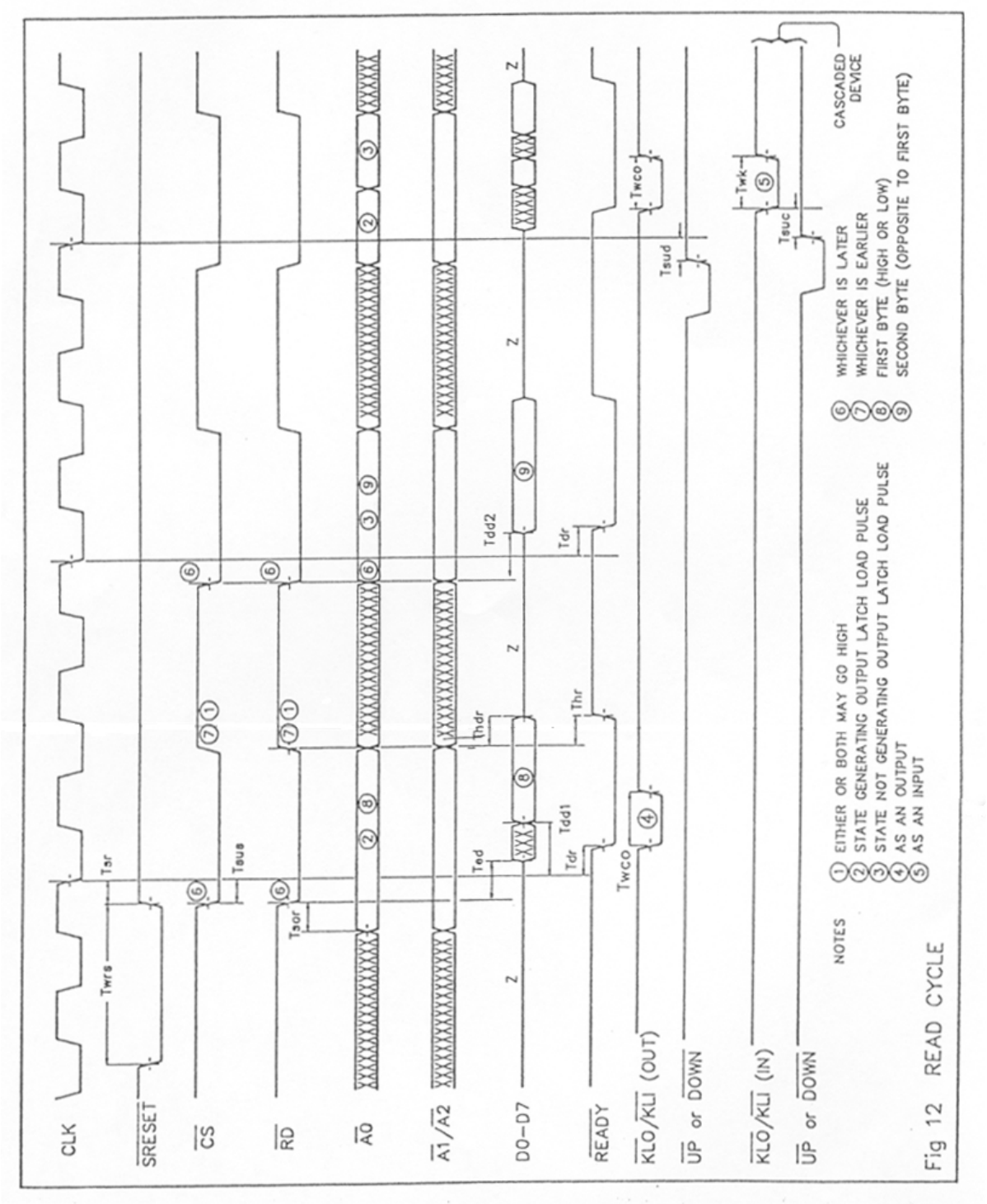


Fig. 11: Read Cycle

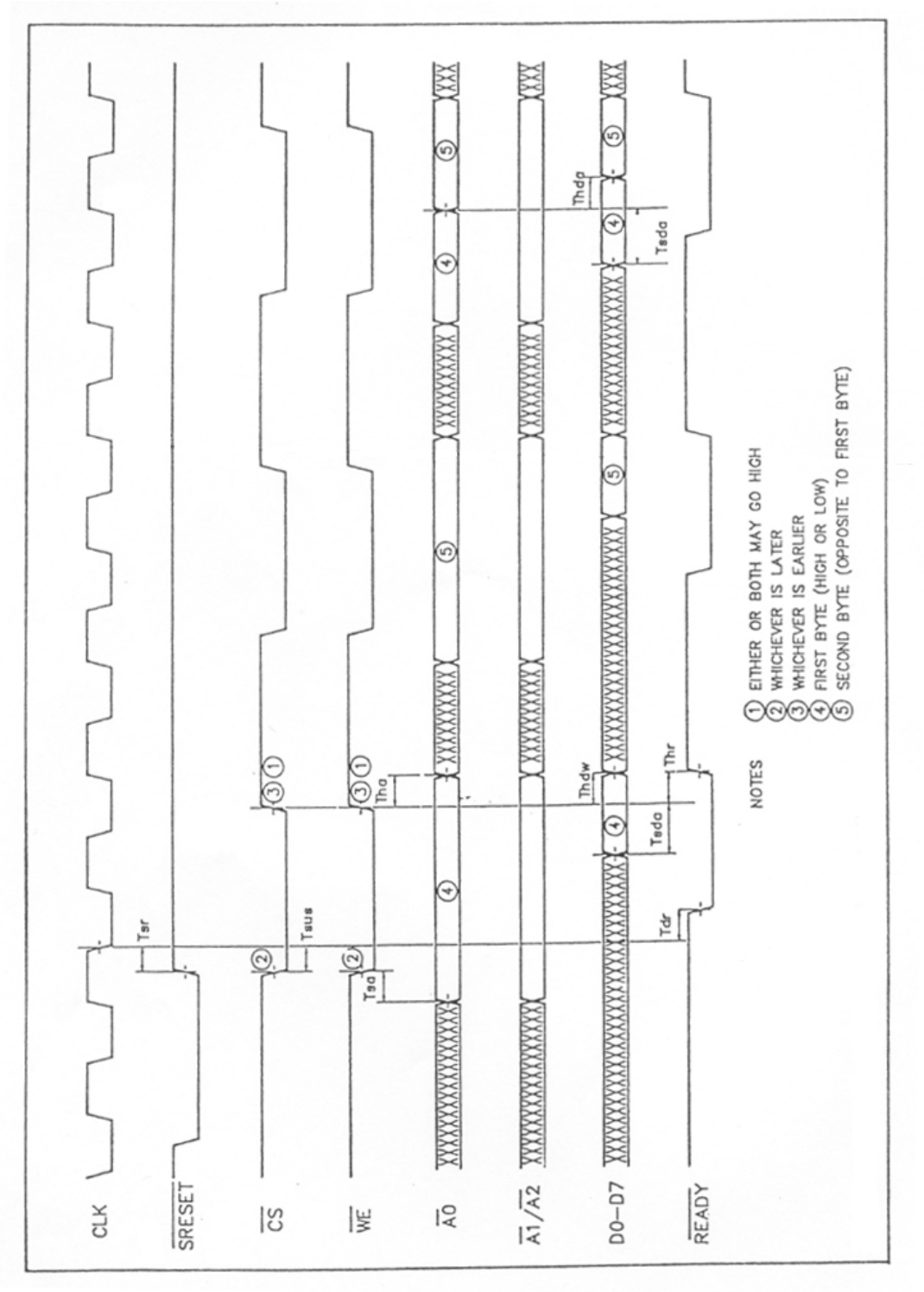


Fig. 12: Write Cycle

System Application

The implementation of a three axis control system with the PE12016G, 12024G is shown in ***Figure 14***. The microprocessor accesses each channel,
memory mapped I/O or I/O addresses with normal read or write cycles. CLK frequencies up to 20MHz can be sourced directly from the microcontroller. For an external freeze, all /KLI-KLOs can be connected together and driven by the external 'freeze-logic'. This logic must be designed such that all PE12016G/12024Gs are programmed into the slave mode before the first read or write cycle appears and must be synchronised with CLK.

If the /READ output (PE12016G only), is used, it must be externally wire-OR'ed (not shown in ***Figure 14***) and fed to the microcontroller /READY input. An external zero pulse from the resolver can drive the PE12024G Ua0 input.

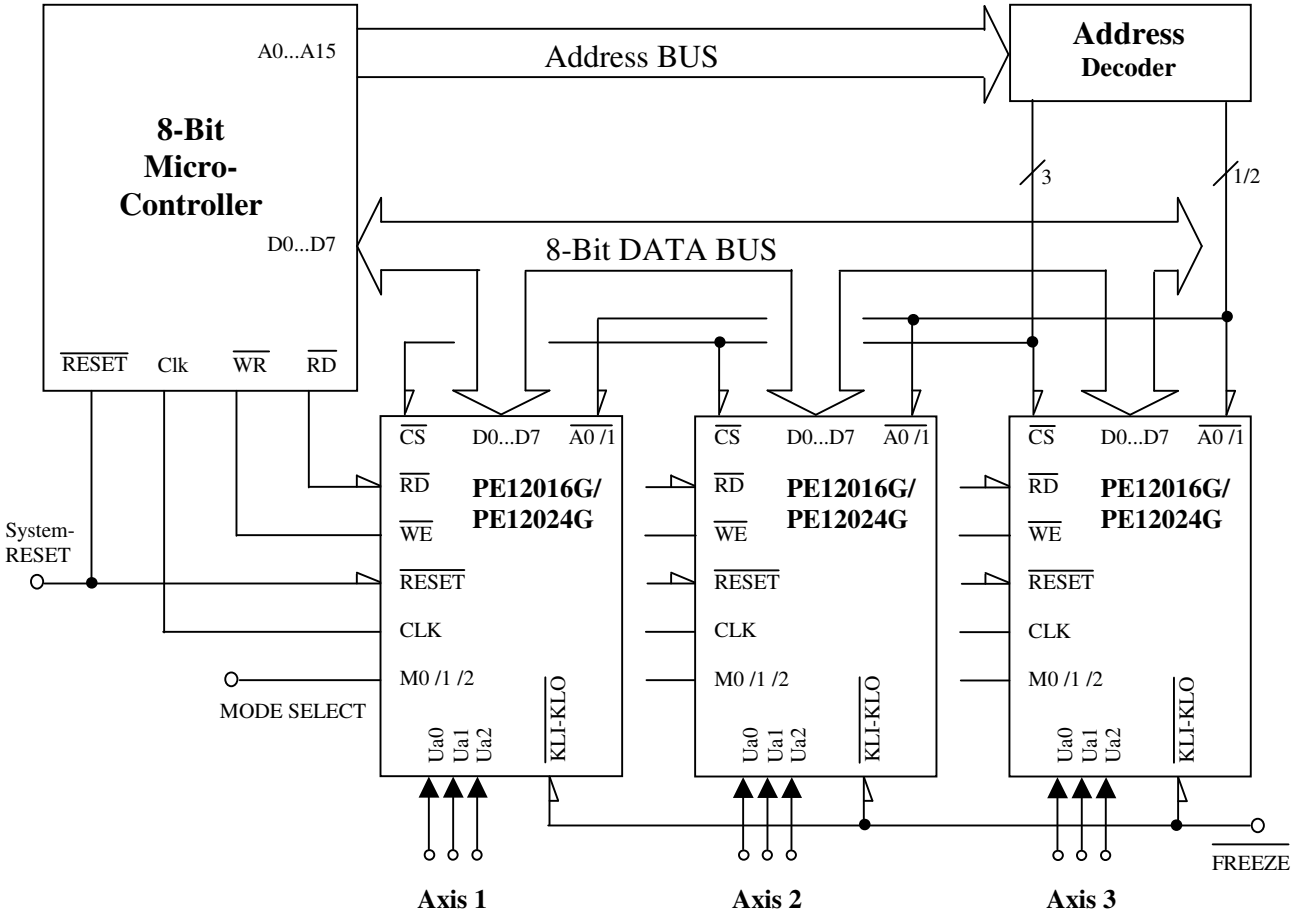


Fig. 13: Block Diagram for a three-axis Control System

Cascading the PE12016G

Figure 15 shows the cascading of two PE12016Gs for 32-bit resolution. The master (LS-word) needs to be programmed to mode 5 and the slave (MS-word) to mode 0 (count only). The /KLI-KLO inputs of both devices are connected together. An external pull-up is not required since it is on-chip. Optional /KLI-KLO signal could be used as an external freeze input. In this case, both devices operate in slave mode (see ***Figure 15*** – cascaded configuration) by generating a /FREEZE low pulse, synchronous with CLK before the first read or write cycle appears after /RESET.
In normal applications, the PE12016G receiving the first read/write cycle after initialisation via a /RESET, is programmed into master mode.

/CARRY an /BORROW of the master PE12016G are connected to the /UP and /DOWN inputs of the slave. If /READY is used to slow down the microprocessor read/write cycle, both /READY outputs must be OR'ed to generate a common READY signal.

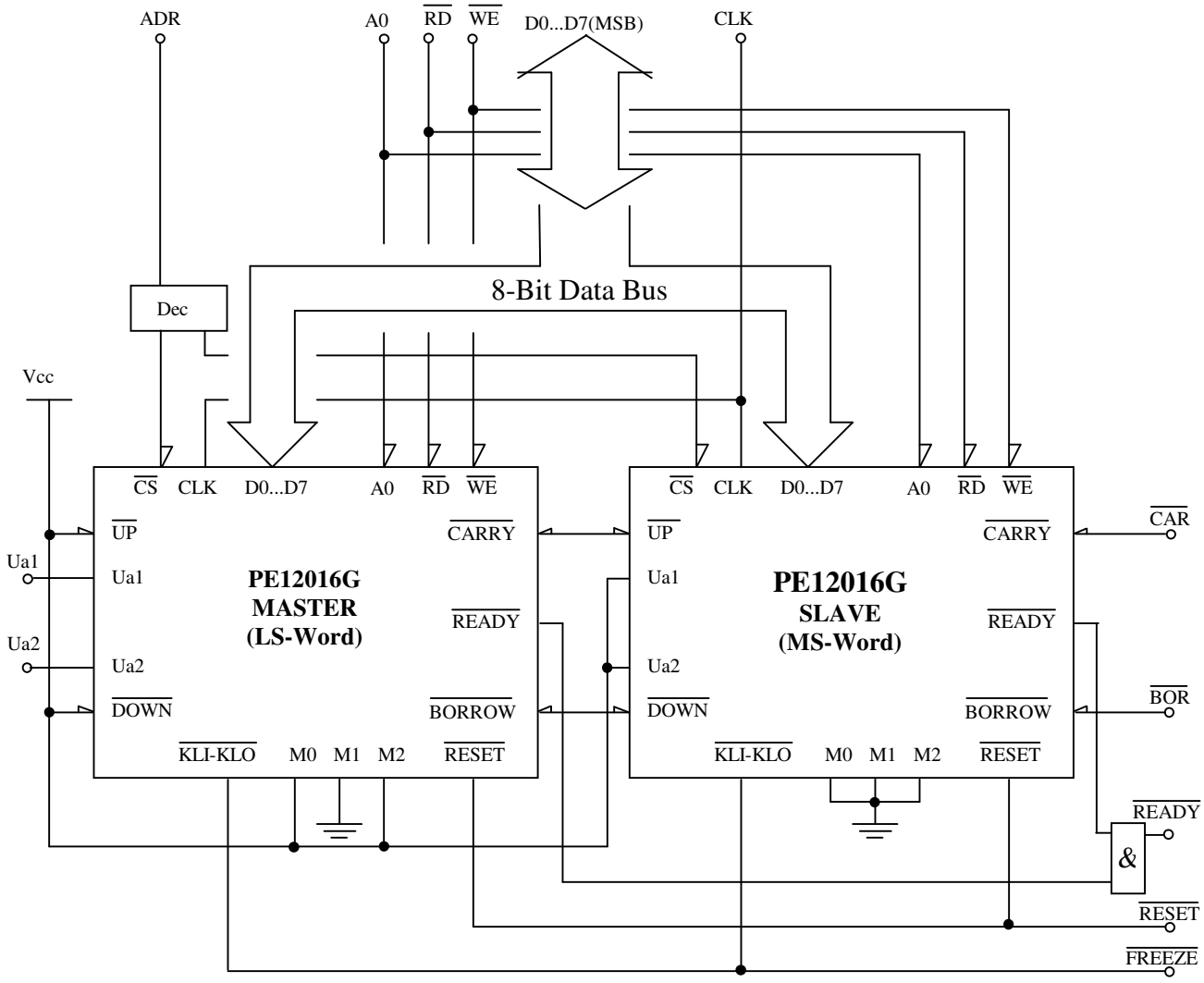
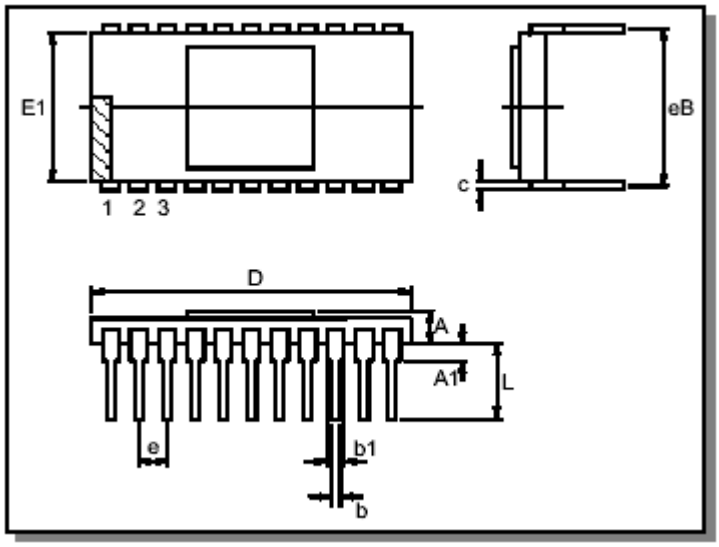


Fig. 14: Cascading of two PE12016G for 32-bit Resolution

PDIP24/28 Package Dimensions

Package Drawing:



Plastic Dual Inline Packages PDIP24 300 mil, PDIP28 600 mil												
Package type		**D**	**E 1**	**eB**	**A**	**A 1**	**b 1**	**e**	**b**	**c**	**L**	**Package Code**
PDIP24 300 mil	min	29.97	7.12	7.62	2.16	0.64	1.14	2.54	0.38	0.23	3.18	
	max	31.00	7.87		5.08	1.78	1.65		0.56	0.38	5.08	
PDIP28 600 mil	min	35.05	14.73	15.24	2.16	0.64	0.14	2.54	0.38	0.23	3.18	
	max	36.07	15.49		5.08	1.78	1.65		0.56	0.38	5.08	
Dimension: mm, original dimension: inch												

Fig. 15: PDIP24/28 Package Dimensions

Package availability chart and ordering code:

	PDIP24-300 mil	**PDIP28-600 mil**	
PE12016G	no	PE12016G-PDIP28	
PE12024G	PE12024G-PDIP24	no	

Application Notes:

Read Cycle:

The read cycle is intended and designed synchronous to the clock. Special care has to be taken for the parameter T_{sus} (the setup time of the falling edge of /RD before the falling CLK edge). If T_{sus} is not within spec, there is the possibility that the output register is not updated and the same value will be read twice.
Therefore the microprocessor system collecting the data and PE12016G/12024G should either have the same clock or the /RD on the PE12016G/12024G has to be synchronized into the PE12016G/12024G clock domain via an ACT74 Type Flipflop.

Cascading:

Cascaded channels which use the /UP, /DOWN Inputs for counting have to be configured to Mode 0. The /UP, /DOWN inputs will have no effect in other Modes. This behaviour is different to CF32007 but not considered serious.

Mode 0:

Mode 0 (PE12016G) is only recommended for cascading. Other applications have to take care of the parameter T_{suc}. PE12016G might give out an invalid value, if this specification is not met. To avoid this, the microprocessor should take care, that data will only be read, when /UP or /DOWN are logically high. Typically this can be achieved by gating these inputs via microprocessor ports by discrete AND/OR gates.

Electrical Design Recommendations:

It is recommended that the PE12016G/12024G is used without a socket and with at least 1 decoupling capcitors (100 nF) connected to VCC and GND close to the package.

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