Product Specification

PE3341

2700 MHz Integer-N PLL with Field-Programmable EEPROM

Features

- Field-programmable EEPROM for self-starting applications
- Standard 2700 MHz operation, 3000 MHz speed-grade option
- ÷10/11 dual modulus prescaler
- Internal charge pump
- Serial programmable
- Low power — 20 mA at 3 V
- Ultra-low phase noise
- Available in 24-lead TSSOP or 20-lead 4x4 mm QFN package

Product Description

The PE3341 is a high performance integer-N PLL with embedded EEPROM capable of frequency synthesis up to 2700 MHz with a speed-grade option to 3000 MHz. The EEPROM allows designers to permanently store control bits, allowing easy configuration of self-starting synthesizers. The superior phase noise performance of the PE3341 is ideal for applications such as sonet, wireless base stations, fixed wireless, and RF instrumentation systems.

The PE3341 features a ÷10/11 dual modulus prescaler, counters, a phase comparator, and a charge pump as shown in Figure 1. Counter values are programmable through a three-wire serial interface.

The PE3341 UltraCMOS™ Phase Locked-Loop is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering excellent RF performance with the economy and integration of conventional CMOS.

Figure 1. Block Diagram

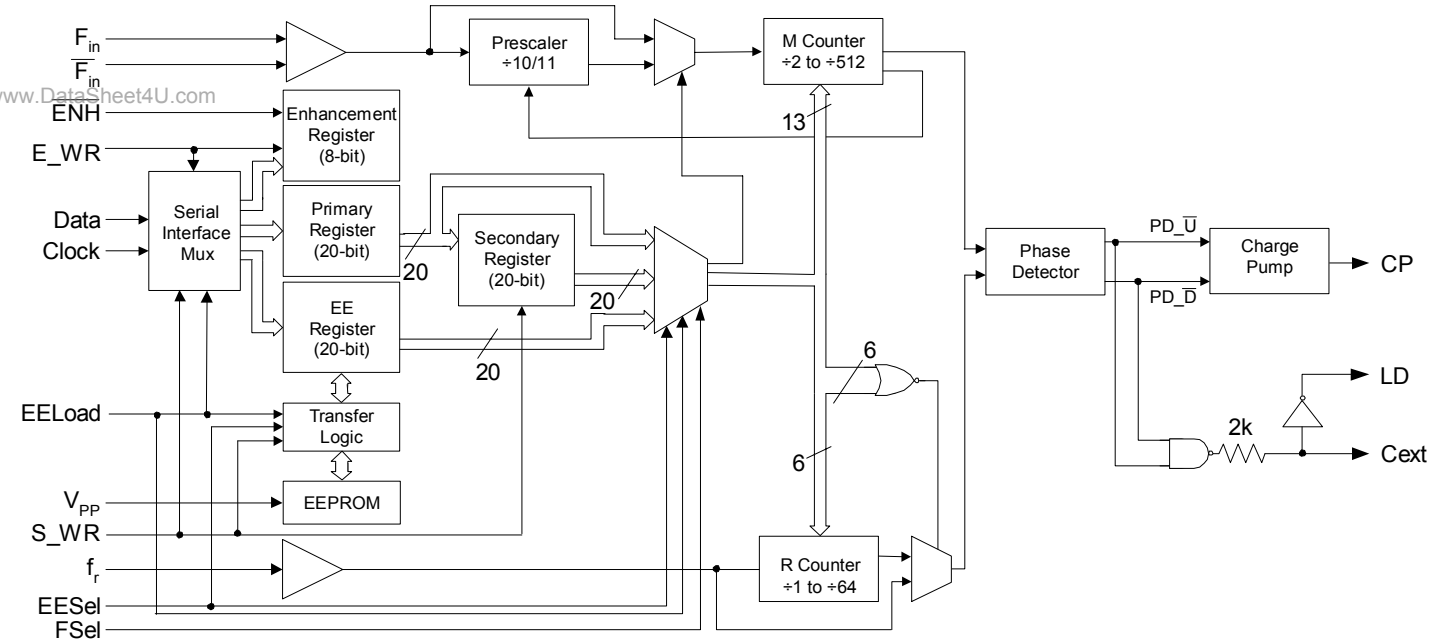


Figure 2. Pin Configurations (Top View)

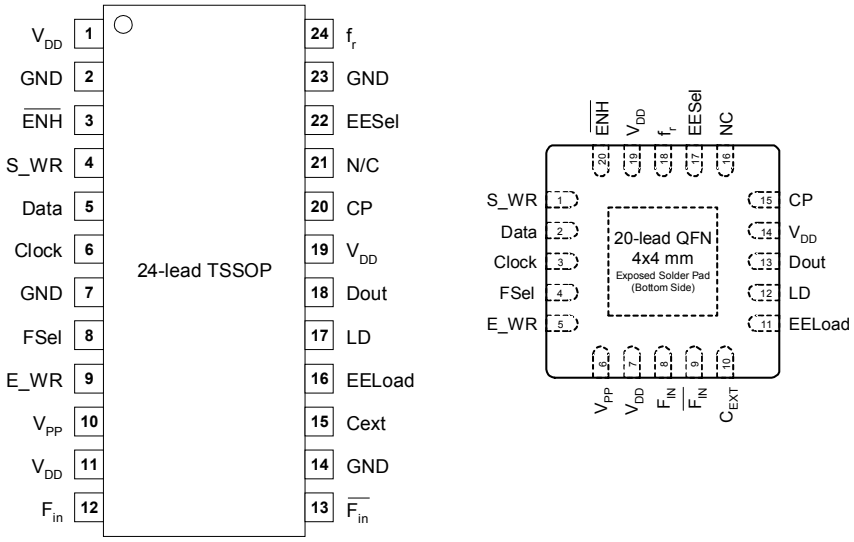


Figure 3. Package Types

24-lead TSSOP, 20-lead QFN

Table 2. Pin Descriptions

Pin No. TSSOP	Pin No. QFN	Pin Name	Type	Description
1	19	V_{DD}	(Note 1)	Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing required.
2		GND	(Note 2)	Ground.
3	20	$\overline{ENH}$	Input	Enhancement mode control line. When asserted LOW, enhancement register bits are functional. Internal 70 kΩ pull-up resistor.
4	1	S_WR	Input	Secondary Register WRITE input. Primary Register contents are copied to the Secondary Register on S_WR rising edge. Also used to control Serial Port operation and EEPROM programming.
5	2	Data	Input	Binary serial data input. Input data entered LSB (B_0) first.
6	3	Clock	Input	Serial clock input. Data is clocked serially into the 20-bit Primary Register, the 20-bit EE Register, or the 8-bit Enhancement Register on the rising edge of Clock. Also used to clock EE Register data out Dout port.
7		GND	(Note 2)	Ground.
8	4	FSel	Input	Frequency Register selection control line. Internal 70 kΩ pull-down resistor.
9	5	E_WR	Input	Enhancement Register write enable. Also functions as a Serial Port control line. Internal 70 kΩ pull-down resistor.
10	6	V_{PP}	Input	EEPROM erase/write programming voltage supply pin. Requires a 100pF bypass capacitor connected to GND.
11	7	V_{DD}	(Note 1)	Same as pin 1.
12	8	F_{in}	Input	Prescaler input from the VCO.
13	9	$\overline{F_{in}}$	Input	Prescaler complementary input. A series 50 Ω resistor and DC blocking capacitor should be placed as close as possible to this pin and connected to the ground plane.
14		GND	(Note 2)	Ground.
15	10	C_{EXT}	Output	Logical "NAND" of PD_U and PD_D terminated through an on-chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
16	11	EELoad	Input	Control line for Serial Data Port, Frequency Register selection, EE Register parallel loading, and EEPROM programming. Internal 70 kΩ pull-down resistor.
17	12	LD	Output, OD	Lock detect output, an open-drain logical inversion of C_{EXT}. When the loop is in lock, LD is high impedance; otherwise, LD is a logic LOW.

Pin No. TSSOP	Pin No. QFN	Pin Name	Type	Description
18	13	Dout	Output	Data out function. Dout is defined with the Enhancement Register and enabled with $\overline{ENH}$.
19	14	V_{DD}	(Note 1)	Same as pin 1.
20	15	CP	Output	Charge pump output. Sources current is when f_c leads f_p and sinks current when f_c lags f_p.
21	16	N/C		No connection.
22	17	EESel	Input	Control line for Frequency Register selection, EE Register parallel loading, and EEPROM programming. Internal 70 kΩ pull-up resistor.
23		GND	(Note 2)	Ground.
24	18	f_r	Input	Reference frequency input.

Notes 1: V_{DD} pins 1, 11, and 19 (TSSOP) or pins 6, 14 and 19 (QFN), are connected by diodes and must be supplied with the same positive voltage level.

2: Ground connections are made through the exposed solder pad. The solder pad must be soldered to the ground plane for proper operation.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	–0.3	+4.0	V
V_I	Voltage on any digital input	–0.3	V_{DD}+0.3	V
T_{Stg}	Storage temperature range	–65	+85	°C

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC and AC Characteristics table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3. DC Electrical Specifications

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.15	V
T_A	Operating ambient temperature range	-40	85	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{ESD}	ESD voltage human body model (Note 1)		1000	V
V_{ESD} (V_{PP})	ESD voltage human body model (Note 1)		200	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. DC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current; Prescaler enabled	V_{DD} = 2.85 to 3.15 V		20	30	mA
Digital Inputs: S_WR, Data, Clock						
V_{IH}	High-level input voltage	V_{DD} = 2.85 to 3.15 V	0.7 x V_{DD}			V
V_{IL}	Low-level input voltage	V_{DD} = 2.85 to 3.15 V			0.3 x V_{DD}	V
I_{IH}	High-level input current	V_{IH} = V_{DD} = 3.15 V			+1	µA
I_{IL}	Low-level input current	V_{IL} = 0, V_{DD} = 3.15 V	-1			µA
Digital inputs: $\overline{ENH}$, EESel (contains a 70 kΩ pull-up resistor)						
V_{IH}	High-level input voltage	V_{DD} = 2.85 to 3.15 V	0.7 x V_{DD}			V
V_{IL}	Low-level input voltage	V_{DD} = 2.85 to 3.15 V			0.3 x V_{DD}	V
I_{IH}	High-level input current	V_{IH} = V_{DD} = 3.15 V			+1	µA
I_{IL}	Low-level input current	V_{IL} = 0, V_{DD} = 3.15 V	-100			µA
Digital inputs: FSel, EELoad, E_WR (contains a 70 kΩ pull-down resistor)						
V_{IH}	High-level input voltage	V_{DD} = 2.85 to 3.15 V	0.7 x V_{DD}			V
V_{IL}	Low-level input voltage	V_{DD} = 2.85 to 3.15 V			0.3 x V_{DD}	V
I_{IH}	High-level input current	V_{IH} = V_{DD} = 3.15 V			+100	µA
I_{IL}	Low-level input current	V_{IL} = 0, V_{DD} = 3.15 V	-1			µA
EE Memory Programming Voltage and Current: V_{PP}, I_{PP}						
V_{PP}_WRITE	EEPROM write voltage			12.5		V
V_{PP}_ERASE	EEPROM erase voltage			-8.5		V
I_{PP}_WRITE	EEPROM write cycle current				30	mA
I_{PP}_ERASE	EEPROM erase cycle current		-10			mA
Reference Divider input: f_r						
I_{IHR}	High-level input current	V_{IH} = V_{DD} = 3.15 V			+100	µA
I_{ILR}	Low-level input current	V_{IL} = 0, V_{DD} = 3.15 V	-100			µA
Counter output: Dout						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = -3 mA	V_{DD} - 0.4			V
Lock detect outputs: (C_{EXT}, LD)						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{out} = 0.1 mA			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{out} = -0.1 mA	V_{DD} - 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 1 mA			0.4	V
Charge Pump output: CP						
I_{CP} – Source	Drive current	V_{CP} = V_{DD} / 2	-2.6	-2	-1.4	mA
I_{CP} – Sink	Drive current	V_{CP} = V_{DD} / 2	1.4	2	2.6	mA
I_{CPL}	Leakage current	1.0 V < V_{CP} < V_{DD} – 1.0 V	-1		1	µA
I_{CP} - Source vs. I_{CP} – Sink	Sink vs. source mismatch	V_{CP} = V_{DD} / 2, T_A = 25° C			15	%
I_{CP} vs. V_{CP}	Output current magnitude variation vs. voltage	1.0 V < V_{CP} < V_{DD} – 1.0 V T_A = 25° C			15	%

Table 6. AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
Control Interface and Registers (see Figure 4)					
f_{Clk}	Serial data clock frequency	(Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time		30		ns
t_{ClkL}	Serial clock LOW time		30		ns
t_{DSU}	Data set-up time to Clock rising edge		10		ns
t_{DHLD}	Data hold time after Clock rising edge		10		ns
t_{PW}	S_WR pulse width		30		ns
t_{CWR}	Clock rising edge to S_WR rising edge		30		ns
t_{CE}	Clock falling edge to E_WR transition		30		ns
t_{WRC}	S_WR falling edge to Clock rising edge		30		ns
t_{EC}	E_WR transition to Clock rising edge		30		ns
EEPROM Erase/Write Programming (see Figures 5 & 6)					
t_{EESU}	EELoad rising edge to V_{PP} rising edge		500		ns
t_{EEPW}	V_{PP} pulse width		25	30	ms
t_{VPP}	V_{PP} pulse rise and fall times	(Note 2)	1		µs
Main Divider (Including Prescaler)					
F_{In}	Operating frequency		300	2700	MHz
F_{In}	Operating frequency	Speed-grade option (Note 3)	300	3000	MHz
P_{FIn}	Input level range	External AC coupling	-5	5	dBm
Main Divider (Prescaler Bypassed)					
F_{In}	Operating frequency	(Note 4)	50	270	MHz
P_{FIn}	Input level range	External AC coupling (Note 4)	-5	5	dBm
Reference Divider					
f_r	Operating frequency	(Note 5)		100	MHz
P_{fr}	Reference input power (Note 4)	Single ended input	-2		dBm
Phase Detector					
f_c	Comparison frequency	(Note 6)		20	MHz
SSB Phase Noise (F_{in} = 1.3 GHz, f_r = 10 MHz, f_c = 1.25 MHz, LBW = 70 kHz, V_{DD} = 3.0 V, Temp = -40° C)					
	100 Hz Offset			-75	dBc/Hz
	1 kHz Offset			-85	dBc/Hz

Note 1: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{Clk} specification.

Note 2: Rise and fall times of the V_{PP} programming voltage pulse must be greater than 1 µs.

Note 3: The maximum frequency of operation can be extended to 3.0 GHz by ordering a special speed-grade option. Please refer to Table 14, Ordering Information, for ordering details.

Note 4: CMOS logic levels can be used to drive F_{In} input if DC coupled and used in Prescaler Bypass mode. Voltage input needs to be a minimum of 0.5 Vp-p. For optimum phase noise performance, the reference input falling edge rate should be faster than 80 mV/ns. No minimum frequency limit exists when operated in this mode.

Note 5: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5 Vp-p. For optimum phase noise performance, the reference input falling edge rate should be faster than 80 mV/ns.

Note 6: Parameter is guaranteed through characterization only and is not tested.

Functional Description

The PE3341 consists of a dual modulus prescaler, three programmable counters, a phase detector with charge pump and control logic with EEPROM memory (see Figure 1).

The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the state of the internal modulus select logic. The R and M counters divide the reference and prescaler outputs by integer values stored in one of three selectable registers. The modulus select logic uses the 4-bit A counter.

The phase-frequency detector generates up and down frequency control signals that direct the charge pump operation, and are also used to enable a lock detect circuit.

Frequency control data is loaded into the device via the Serial Data Port, and can be placed in three separate frequency registers. One of these registers (EE register) is used to load from and write to the non-volatile 20-bit EEPROM.

Various operational and test modes are available through the enhancement register, which is only accessible through the Serial Data Port (it cannot be loaded from the EEPROM).

Main Counter Chain

The main counter chain divides the RF input frequency, F_{in}, by an integer derived from the user-defined values in the M and A counters. It operates in two modes:

High Frequency Mode

Setting PB (prescaler bypass) LOW enables the ÷10/11 prescaler, providing operation to 2.7 GHz. In this mode, the output from the main counter chain, f_p, is related to the VCO frequency, F_{in}, by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \quad (1)$$
$$\text{where } 0 \le A \le 15 \text{ and } A \le M + 1; 1 \le M \le 511$$

When the loop is locked, F_{in} is related to the reference frequency, f_r, by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \quad (2)$$
$$\text{where } 0 \le A \le 15 \text{ and } A \le M + 1; 1 \le M \le 511$$

A consequence of the upper limit on A is that F_{in} must be greater than or equal to 90 x (f_r / (R+1)) to obtain contiguous channels. Programming the M counter with the minimum value of 1 will result in a minimum M counter divide ratio of 2.

Programming the M and A counters with their maximum values provides a divide ratio of 5135.

Prescaler Bypass Mode

Setting the PB bit of a frequency register HIGH allows F_{in} to bypass the ÷10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{in} to the reference frequency f_r:

$$F_{in} = (M + 1) \times (f_r / (R+1)) \quad (3)$$
$$\text{where } 1 \le M \le 511$$

Reference Counter

The reference counter chain divides the reference frequency, f_r, down to the phase detector comparison frequency, f_c.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (4)$$
$$\text{where } 0 \le R \le 63$$

Note that programming R with 0 will pass the reference frequency, f_r, directly to the phase detector.

Phase Detector and Charge Pump

The phase detector is triggered by rising edges from the main counter (f_p) and the reference counter (f_c). It has two outputs, PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses LOW. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_U pulses LOW. The width of either pulse is directly proportional to the phase offset between the f_p and f_c signals.

The signals from the phase detector are also routed to an internal charge pump. PD_U controls a current source at pin CP, and PD_D controls a current sink at pin CP. When using a positive Kv VCO, PD_U pulses (current source) will increase the VCO frequency, and PD_D pulses (current sink) will decrease VCO frequency.

Lock Detect Output

A lock detect signal is provided at pin LD, via the pin C_{EXT} (see Figure 1). C_{EXT} is the logical "NAND" of PD_U and PD_D waveforms, driven through a series 2k ohm resistor. When the loop is locked, this output will be HIGH with narrow pulses LOW. Connecting C_{EXT} to an external shunt capacitor provides integration of this signal.

The C_{EXT} signal is sent to the LD pin through an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_U and PD_D.

Serial Data Port

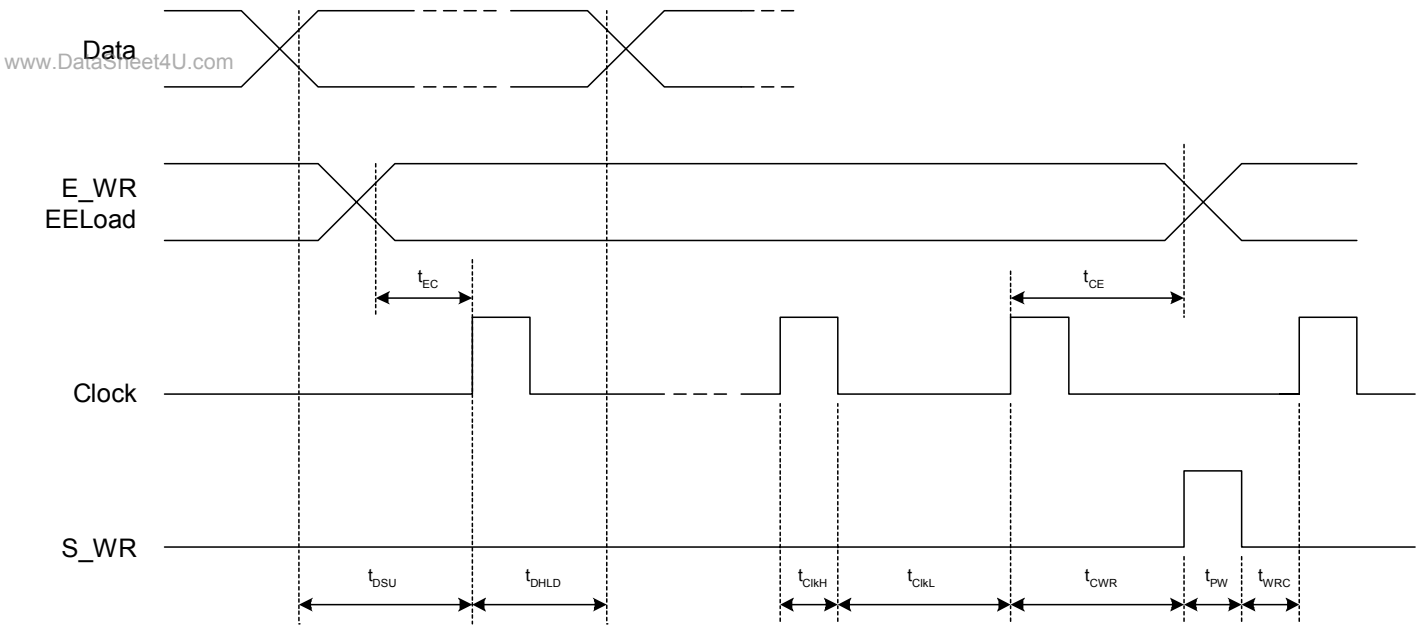
The Serial Data Port allows control data to be entered into the device. This data can be directed into one of three registers: the Enhancement register, the Primary register, and the EE register. Table 7 defines the control line settings required to select one of these destinations.

Input data presented on pin 5 (Data) is clocked serially into the designated register on the rising edge of Clock. Data is always loaded LSB (B_0) first into the receiving register. Figure 4 defines the timing requirements for this process.

Table 7. Serial Interface

S_WR	E_WR	EELoad	Register Loaded
0	0	0	Primary Register
0	1	0	Enhancement Register
0	X	1	EE Register

Figure 4. Serial Interface Timing Diagram



Frequency Registers

There are three independent frequency registers, any one of which can be selected to control the operation of the device. Each register is 20 bits in length, and provides data to the three counters and the prescaler bypass control. Table 8 defines these bit assignments.

Primary Register

The Primary Register is a serial shift register, loaded through the Serial Data Port. It can be selected to control the PLL as shown in Table 9. It is not buffered, thus when this register is selected to control the PLL, its data is continuously presented to the counters during a load operation.

This register is also used to perform a parallel load of data into the Secondary Register.

Secondary Register

The Secondary Register is a parallel-load register. Data is copied into this register from the Primary Register on the rising edge of S_WR, according to the timing diagrams shown in Figure 3. It can be selected to control the PLL as shown in Table 9.

EE Register

The EE Register is a serial/parallel-in, serial/ parallel-out register, and provides the interface to the EEPROM. It is loaded from the Serial Data Port to provide the parallel data source when writing to the EEPROM. It also accepts stored data from the EEPROM for controlling the PLL.

Serial loading of the EE Register is done as shown in Table 7 and Figure 4. Parallel loading of the register from EEPROM is accomplished as shown in Table 10.

The EE register can be selected to control the PLL as shown in Table 9. Note that it cannot be selected to control the PLL using data that has been loaded serially. This is because it must first go through one of the two conditions in Table 10 that causes the EEPROM data to be copied into the EE Register. The effect of this is that only EEPROM data is used when the EE Register is selected.

The contents of the EE register can also be shifted out serially through the Dout pin. This mode is enabled by appropriately programming the Enhancement Register. In this mode, data exits the register on the rising edge of Clock, LSB (B_0) first, and is replaced with the data present on the Data input pin. Tables 7 and 12 define the settings required to enable this mode.

Table 8. Primary / Secondary / EE Register Bit Assignments

R_5	R_4	M_8	M_7	PB	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}

Table 9. Frequency Register Selection

EESel	FSel	EELoad	Register Selected
0	1	0	Primary Register
0	0	0	Secondary Register
1	X	0	EE Register

Table 10. EE Register Load from EEPROM

EESel	EELoad	Function
_/‾	0	EEPROM → EE Register
1	‾_	EEPROM → EE Register

Enhancement Register

The Enhancement Register is a buffered serial shift register, loaded from the Serial Data Port. It activates special test and operating modes in the PLL. The bit assignments for these modes are shown in Table 11.

The functions of these Enhancement Register bits are shown in Table 12. A function becomes active when its corresponding bit is set HIGH. Note that bits 1, 2, 5, and 6 direct various data to the Dout pin, and for valid operation no more than one should be set HIGH simultaneously.

The Enhancement Register is buffered to prevent inadvertent control changes during serial loading. Data that has been loaded into the register is captured in the buffer and made available to the PLL on the falling edge of E_WR.

A separate control line is provided to enable and disable the Enhancement mode. Functions are enabled by taking the $\overline{ENH}$ control line LOW. Note: The enhancement register bit values are unknown during power up. To avoid enabling the enhancement mode during power up, set the Enh pin high ("1") until the enhancement register bit values are programmed to a known state.

Table 11. Enhancement Register Bit Assignments

Reserved	EE Register Output	f_p output	Power down	Counter load	MSEL output	f_c output	Reserved
B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

Table 12. Enhancement Register Functions

Bit Function		Description
Bit 0	Reserved	Program to 0
Bit 1	EE Register Output	Allows the contents of the EE Register to be serially shifted out Dout, LSB (B_0) first. Data is shifted on rising edge of Clock.
Bit 2	f_p output	Provides the M counter output at Dout.
Bit 3	Power down	Powers down all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Provides the internal dual modulus prescaler modulus select (MSEL) at Dout.
Bit 6	f_c output	Provides the R counter output at Dout.
Bit 7	Reserved	Program to 0

EEPROM Programming

Frequency control data that is present in the EE Register can be written to the non-volatile EEPROM. All 20 bits are written simultaneously in a parallel operation. The EEPROM is guaranteed for at least 100 erase/write cycles.

Erase Cycle

The EEPROM should be taken through an erase cycle before writing data, since the write operation performs a logical AND of the EEPROM's current contents with the data in the EE Register. Erasing the EEPROM is accomplished by holding the S_WR, EESel, and EELoad inputs HIGH, then applying one ERASE programming voltage pulse to the V_{PP} input (see Table 13). The voltage source for this operation must be capable of supplying the EEPROM erase cycle current (I_{PP}_ERASE, Table 5). The timing diagram is shown in Figure 5.

Write Cycle

Using the Serial Data Port, the EE Register is first loaded with the desired data. The EEPROM is then programmed with this data by taking the S_WR input HIGH and EESel input LOW, then applying one WRITE programming voltage pulse to the V_{PP} input. The voltage source for this operation must be capable of supplying the EEPROM write cycle current (I_{PP}_WRITE, Table 5). The timing diagram of this operation is shown in Figure 6. Programming is completed by taking the EELoad input LOW.

Note that it is possible to erroneously overwrite the EE Register with the EEPROM contents before the write cycle begins by unneeded manipulation of the EELoad bit (see Table 10).

Table 13. EEPROM Programming

S_WR	EESel	EELoad	V_{PP}	Function
1	1	1	25ms @ −8.5V	Erase cycle
1	0	1	25ms @ +12.5V	Write cycle

Figure 5. EEPROM Erase Timing Diagram

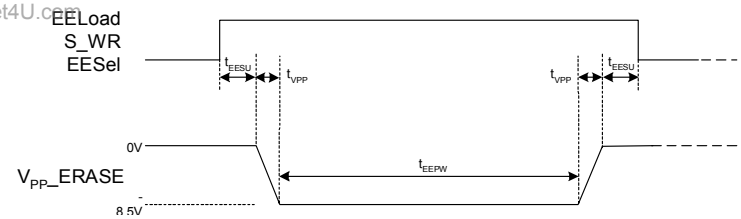
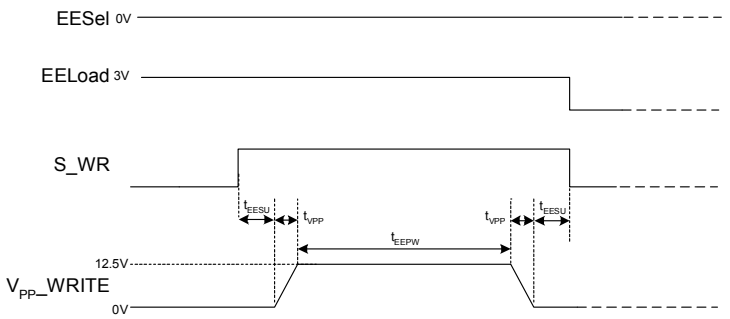


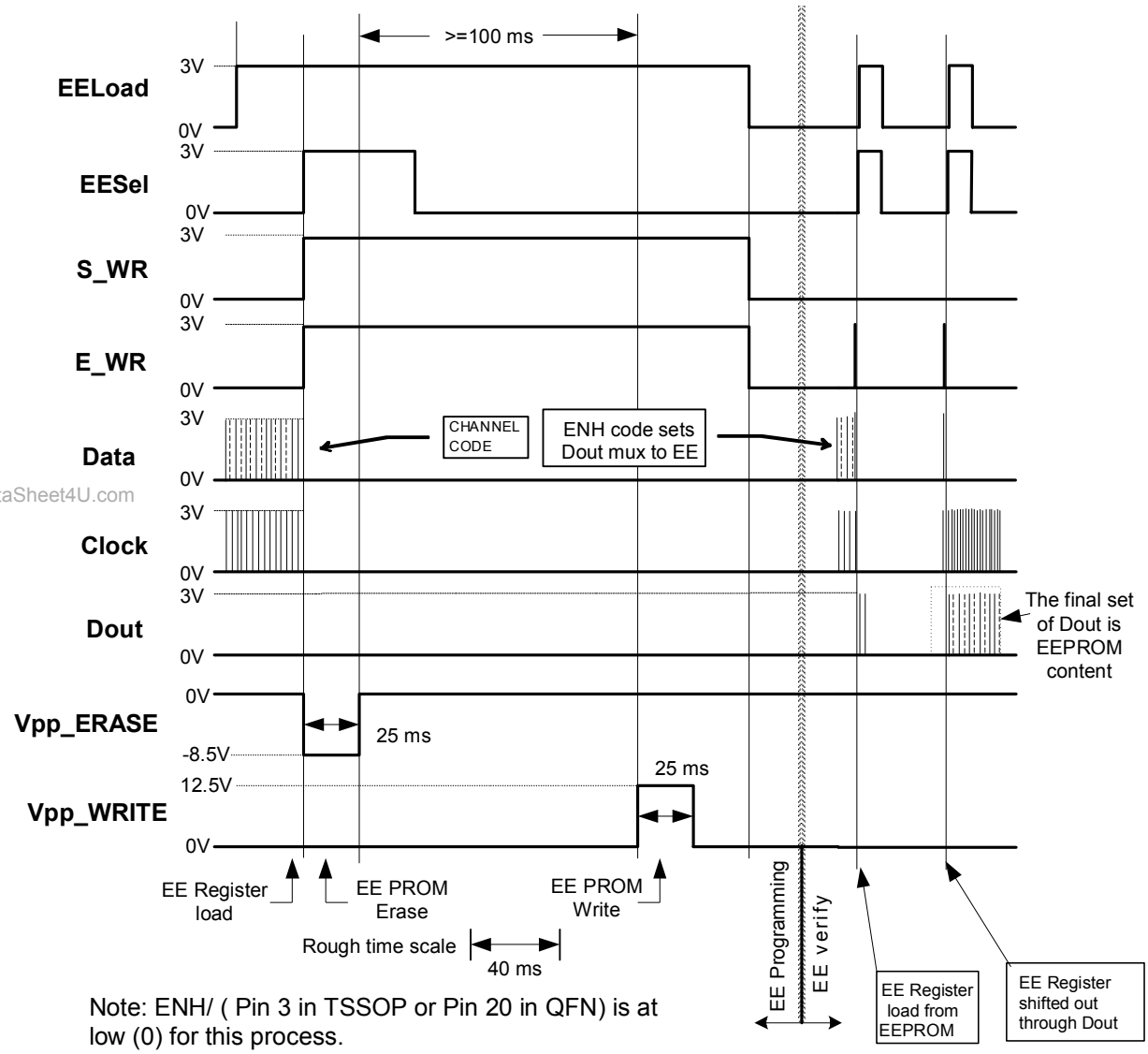
Figure 6. EEPROM Write Timing Diagram



Gross EEPROM Programming Timing Grid

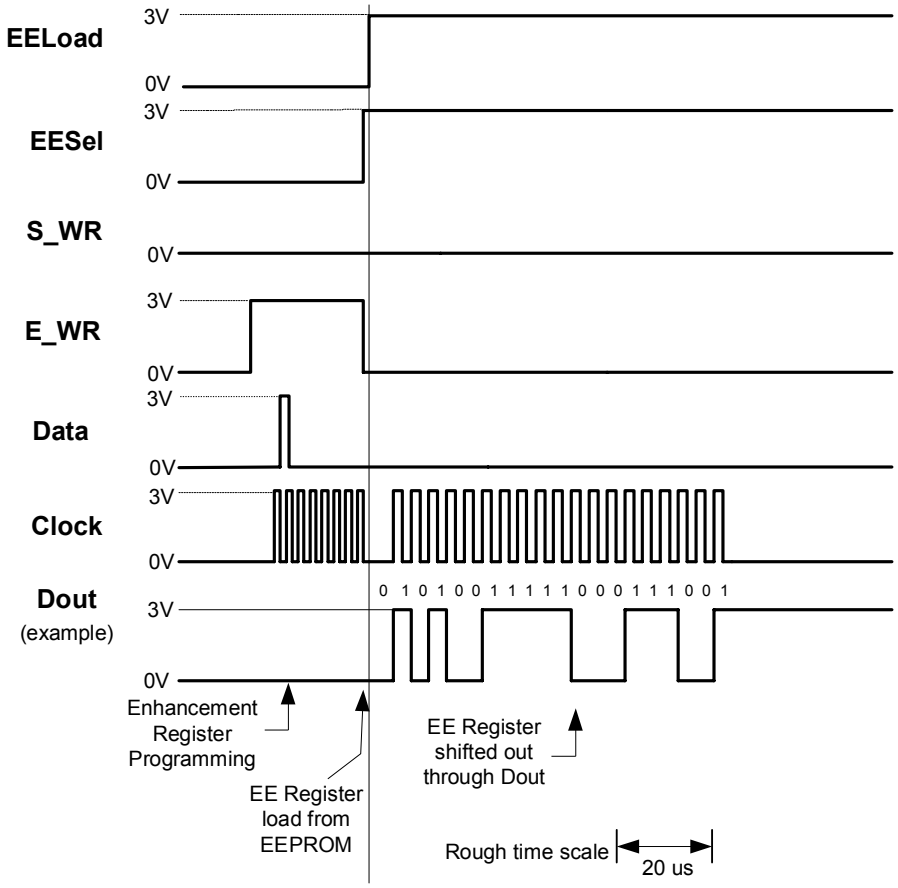
Figure 7 shows a gross PE3341 EEPROM programming timing grid although each individual step has been described thoroughly in previous sections. It starts with EE Register load, and then together with other parameters a Vpp_ERASE negative pulse is applied to Vpp pin to erase the EEPROM contents and followed by a Vpp_WRITE pulse for EEPROM write cycle. The separation between the Vpp_ERASE and Vpp_WRITE pulse has to be at least 100 ms if mechanical relays are used to avoid both being on at the same time. After EE programming, the contents of the EEPROM cells can be verified by setting Enhancement Register Bit 1. A procedure shown in Figure 8 is applied twice. The first time is to load the EE Register from EEPROM and the second time is to shift out the EE Register contents through Dout pin.

Figure 7. Gross PE3341 EEPROM Programming Timing Grid



Note: ENH/ (Pin 3 in TSSOP or Pin 20 in QFN) is at low (0) for this process.

Figure 8. Details of EE register contents loaded from EEPROM and then shifted out Serially through Dout pin - The procedure is performed twice.



Note: ENH/ (Pin 3 in TSSOP or Pin 20 in QFN) is at low (0) for this process.

In Figure 8, the first step is to program Enhancement Register to set Bit 1 high (“1”) to access EE Register Output Bit Function. Subsequent action, which includes pulses, allows the existing EE Register contents to be shifted out the Dout pin and the EEPROM contents are loaded to the EE Register. Since the initial data existing in the EE Register could be anything, the data must be flushed out before clocking the contents of the EEPROM register out. After the same procedures are duplicated, the Dout output is the EEPROM content. Note that only 19 Clock pulses are enough for the 20-bit EE Register because the first bit data is already present at Dout pin. Also ENH/ (Pin 3 in TSSOP or Pin 20 in QFN) is set to low (“0”) to access the Enhancement mode.

Application Information

The PE3341 has been designed to allow a self-starting PLL synthesizer to be built, removing the need to have a micro-controller or other programming source load data into the device on power-up. It can be used as a remotely controllable PLL as well, since the EEPROM circuitry has been added to a complete PLL core (PE3339).

The PE3341's EEPROM can be programmed in-circuit, or prior to assembly using a socketed fixture.

It can be reprogrammed a minimum of 100 times, but is not designed to support constant reprogramming of the EEPROM by an application.

Self-Starting Mode

In self-starting applications, the EE Register is used to control the device and must be selected per Table 9. Additionally, the contents of the EEPROM must be copied to the EE Register per Table 10, and device power must be stable for this transfer to be reliably accomplished. These requirements can be met by connecting a capacitor of 50pF-10uF (evaluation design uses 3.3uF) from the EESel pin to ground. The delay of the rising edge on EESel, created by the RC time constant of its 70k ohm internal pull-up resistor and the external capacitor, will allow device power to stabilize first, ensuring proper data transfer. This edge is adaptable by capacitor value selection. The Vcc applied to the IC must be settled first.

Evaluation and Programming Kit Support

To provide easy evaluation of the PE3341 and to also enable programming of small evaluation quantities, Peregrine has developed complete evaluation kits and programming kits for the PE3341 EEPROM PLLs.

Evaluation Kits

The evaluation kits consist of an evaluation board and support software enabling the user to evaluate the full functionality of the part. The EEPROM can be loaded with user specified values and then placed in a self start-up mode. Please refer to Table 14, Ordering Information, for the specific order codes.

Programming Kits

The programming kits consist of a programming board and support software that enables the user to program small quantities of devices for prototype evaluation and for small pre-production runs. Please refer to Table 14, Ordering Information, for the specific order codes

Large production quantities can be special programmed at Peregrine for an additional charge. Please contact Peregrine Sales for pricing and leadtime at sales@psemi.com.

Figure 9. Package Drawing

24-lead TSSOP

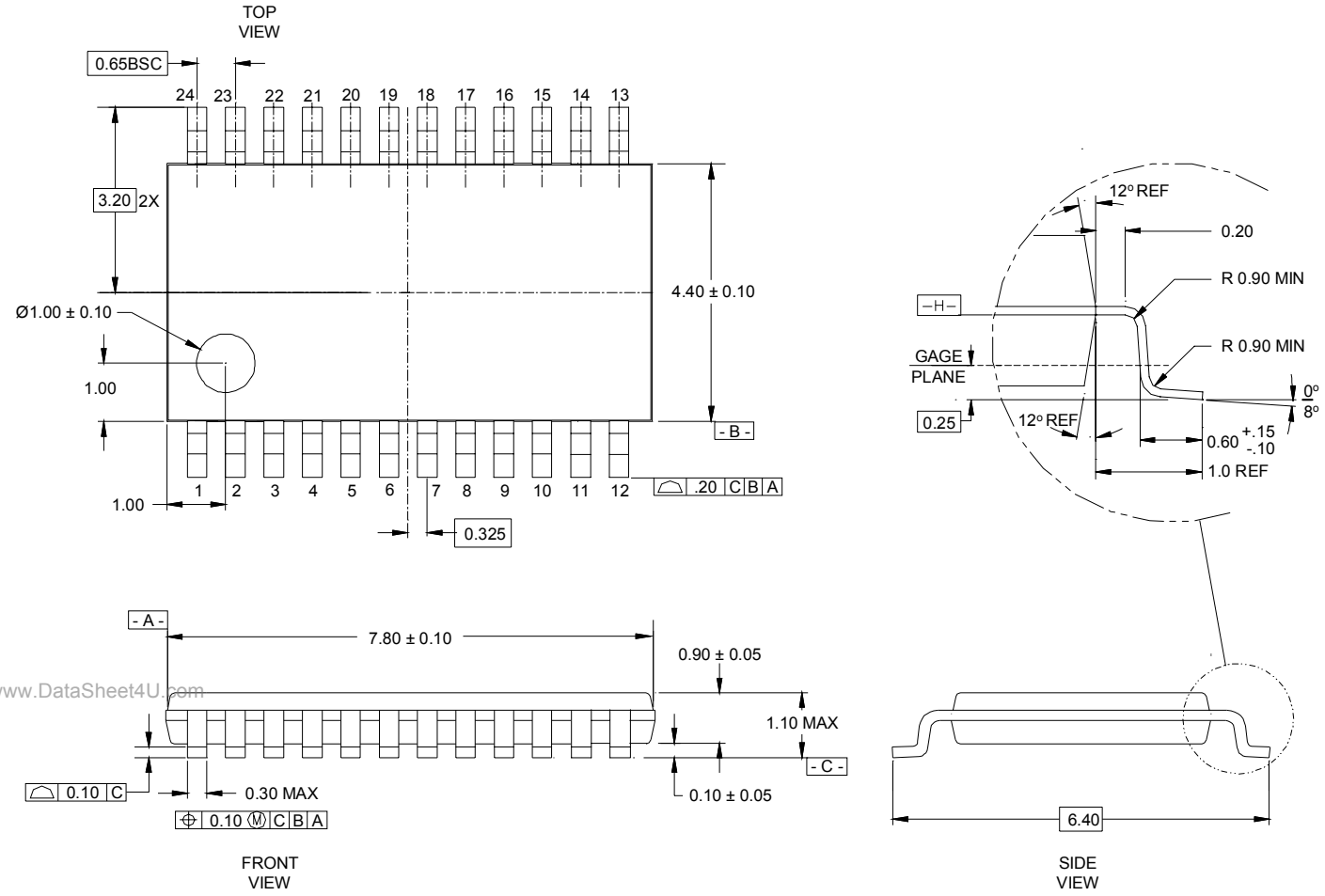
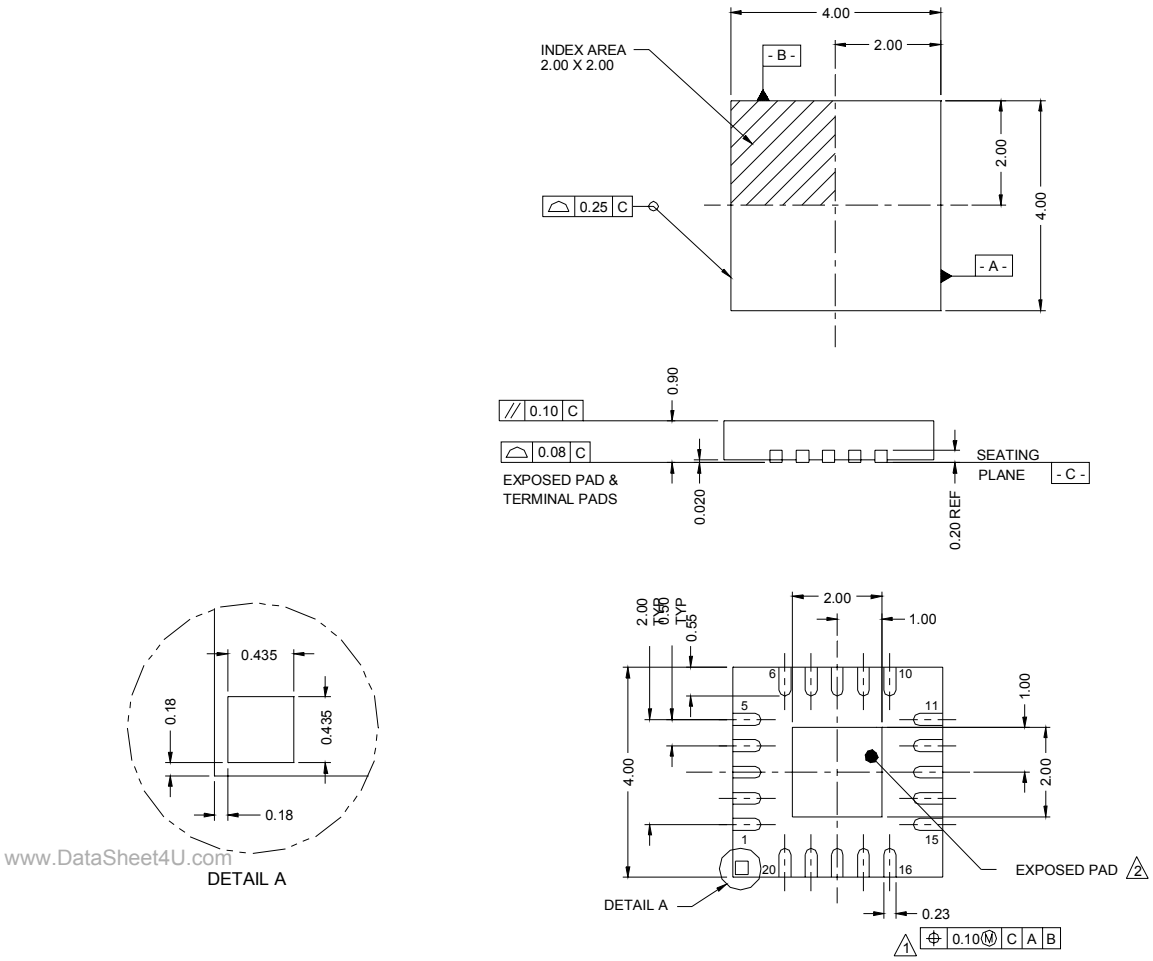


Figure 10. Package Drawing

20-lead QFN



1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 FROM TERMINAL TIP.

2. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Table 14. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
3341-01	PE3341	PE3341-24TSSOP-62A	24-lead TSSOP	62 units / Tube
3341-02	PE3341	PE3341-24TSSOP-2000C	24-lead TSSOP	2000 units / T&R
3341-03	PE3341	PE3341-20QFN4x4-92A	20-lead QFN	92 units / Tube
3341-04	PE3341	PE3341-20QFN4x4-3000C	20-lead QFN	3000 units / T&R
3341-53	PE3341	PE3341G-20QFN4x4-92A	Green 20-lead QFN	92 units / Tube
3341-54	PE3341	PE3341G-20QFN4x4-3000C	Green 20-lead QFN	3000 units / T&R
3341-31	PE3341	PE3341-24TSSOP-62A (3GHz grade)	24-lead TSSOP	62 units / Tube
3341-32	PE3341	PE3341-24TSSOP-2000C (3GHz grade)	24-lead TSSOP	2000 units / T&R
3341-33	PE3341	PE3341-20QFN4x4-92A (3GHz grade)	20-lead QFN	92 units / Tube
3341-34	PE3341	PE3341-20QFN4x4-3000C (3GHz grade)	20-lead QFN	3000 units / T&R
3341-00	PE3341-EK	PE3341-24TSSOP-EK (TSSOP)	Evaluation Kit	1 / Box
3341-05	PE3341-EK	PE3341-20QFN4x4-EK (QFN)	Evaluation Kit	1 / Box
3341-06	PE3341-PK	PE3341-24TSSOP-PK (TSSOP)	Programming Kit	1 / Box
3341-07	PE3341-PK	PE3341-20MLP4x4-PK (QFN)	Programming Kit	1 / Box

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