



深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co., Ltd.



PE4013S

N-Channel Enhancement Mode Power MOSFET

Description

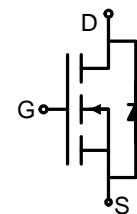
The PE4013S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

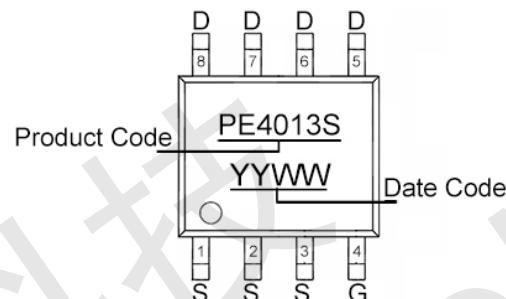
- $V_{DS} > 40V, I_D = 8A$
- $R_{DS(ON)} < 12m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} < 15m\Omega @ V_{GS}=4.5V$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current

Application

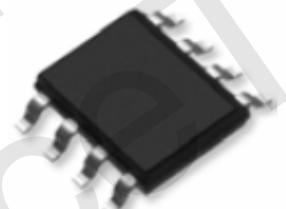
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A=25^\circ C$	I_D	8	A
	$T_A=100^\circ C$		5.5	
Pulsed Drain Current (Note 1)		I_{DM}	32	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	2.5	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	80	$^\circ C/W$



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=40\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$\text{V}_{\text{GS}(\text{th})}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS}(\text{ON})}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=7\text{A}$	-	8.5	12	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_D=6\text{A}$	-	11	15	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=8\text{A}$		75	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=20\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{F}=1.0\text{MHz}$	-	1800	-	PF
Output Capacitance	C_{oss}		-	280	-	PF
Reverse Transfer Capacitance	C_{rss}		-	190	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$\text{V}_{\text{DD}}=20\text{V}, \text{R}_L=2\Omega$ $\text{V}_{\text{GS}}=10\text{V}, \text{R}_G=3\Omega$	-	6.4	-	nS
Turn-on Rise Time	t_r		-	17.2	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	29.6	-	nS
Turn-Off Fall Time	t_f		-	16.8	-	nS
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=20\text{V}, \text{I}_D=7\text{A}, \text{V}_{\text{GS}}=10\text{V}$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	4.5	-	nC
Gate-Drain Charge	Q_{gd}		-	6.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_s=1\text{A}$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$\text{TJ} = 25^\circ\text{C}, \text{IF} = 10\text{A}$ $d\text{i}/dt = 100\text{A}/\mu\text{s}$ (Note 3)	-	29	-	nS
Reverse Recovery Charge	Q_{rr}		-	26	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



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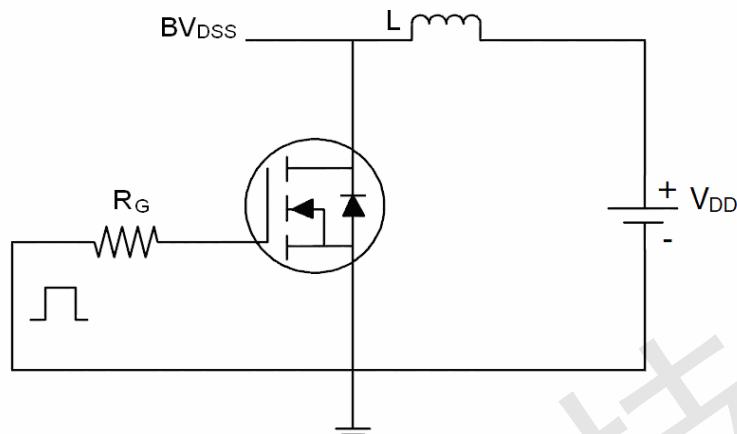
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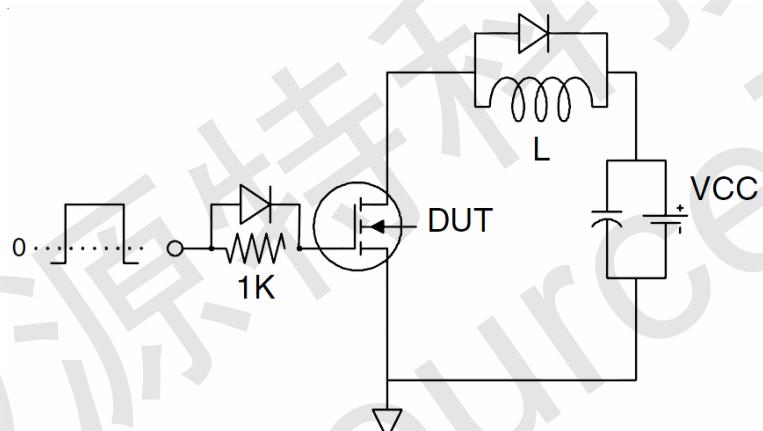
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Test Circuit

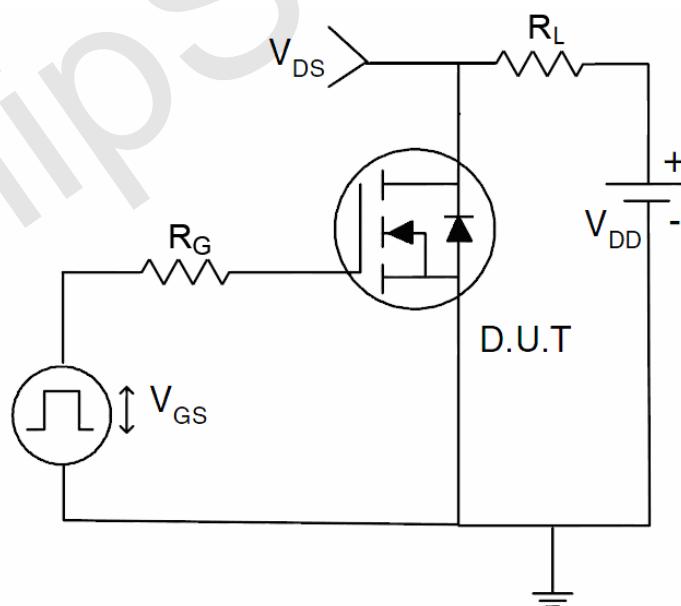
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:





Typical Electrical and Thermal Characteristics (Curves)

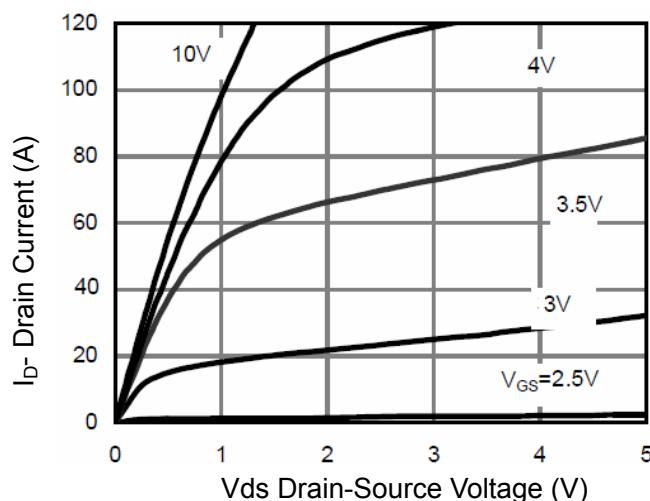


Figure 1 Output Characteristics

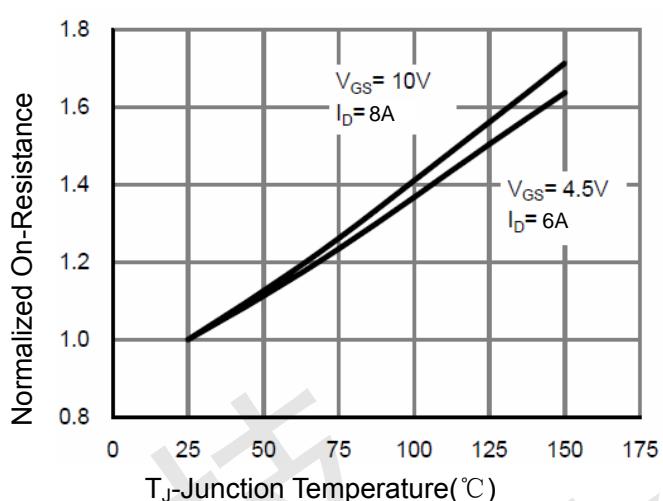


Figure 4 Rdson-JunctionTemperature

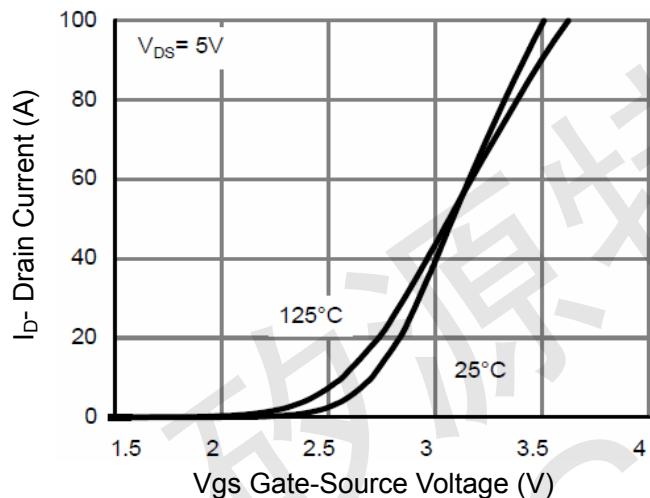


Figure 2 Transfer Characteristics

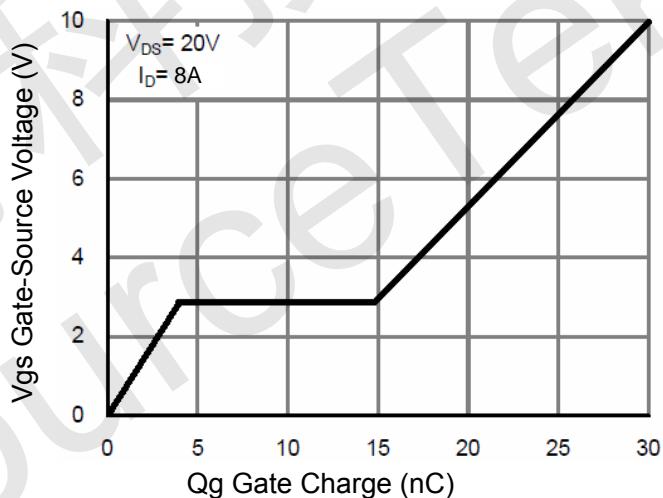


Figure 5 Gate Charge

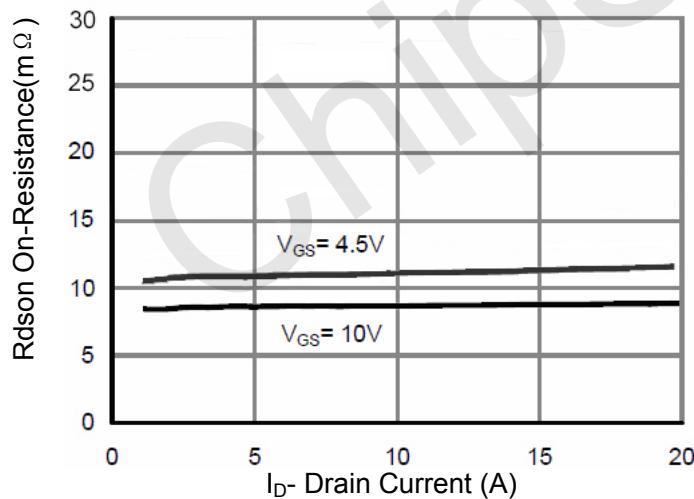


Figure 3 Rdson- Drain Current

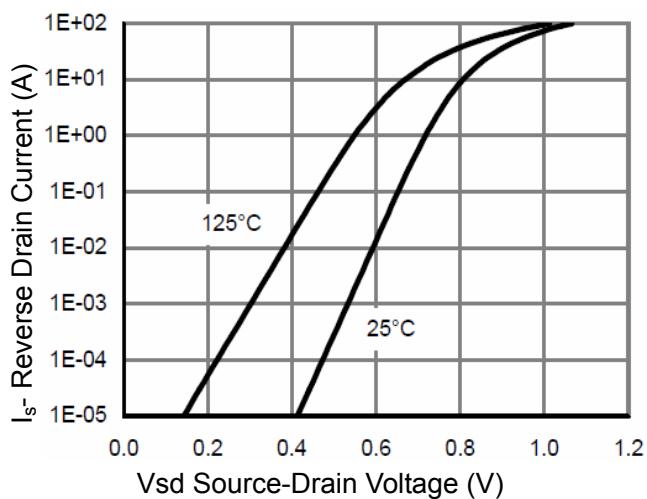


Figure 6 Source- Drain Diode Forward



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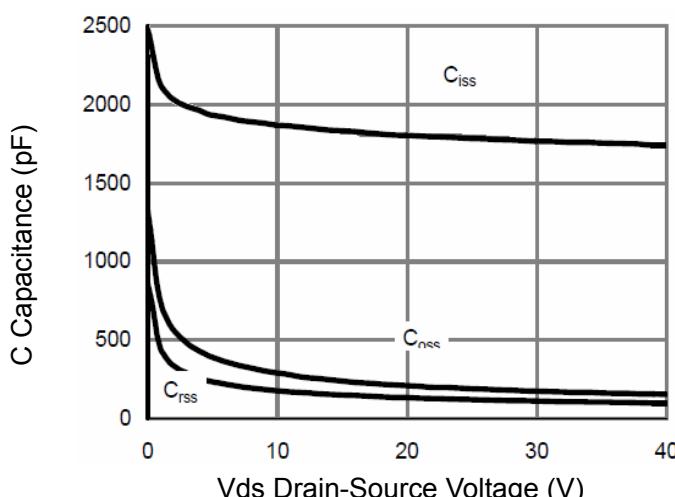


Figure 7 Capacitance vs Vds

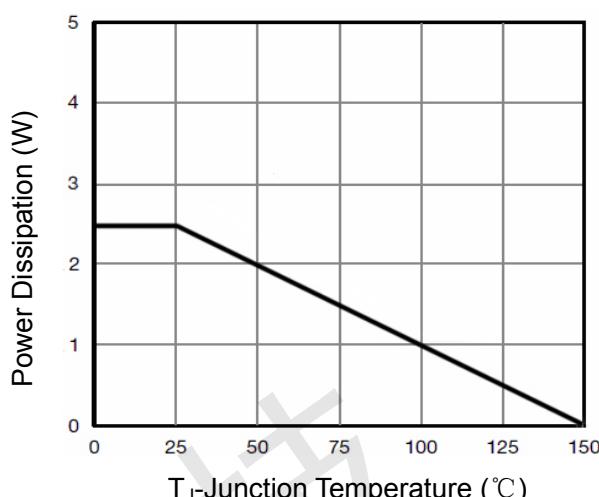


Figure 9 Power De-rating

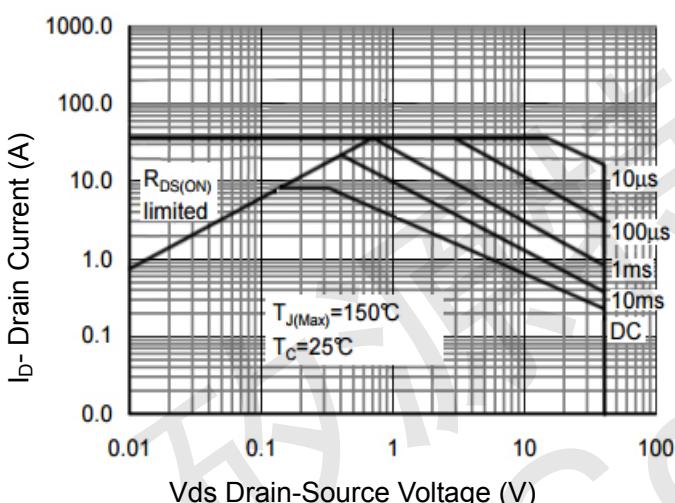


Figure 8 Safe Operation Area

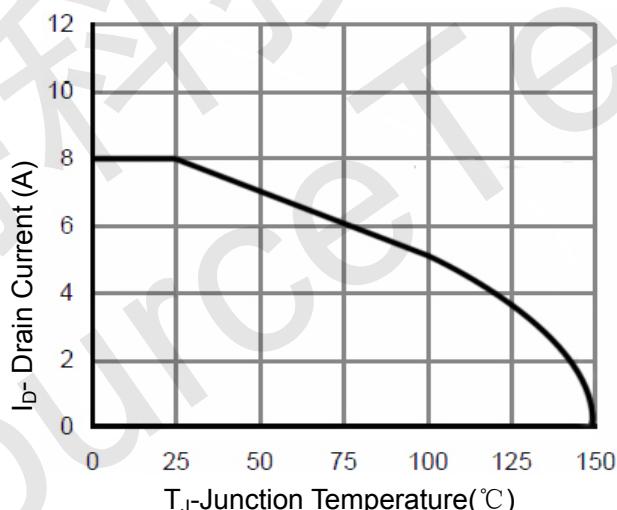


Figure 10 Current De-rating

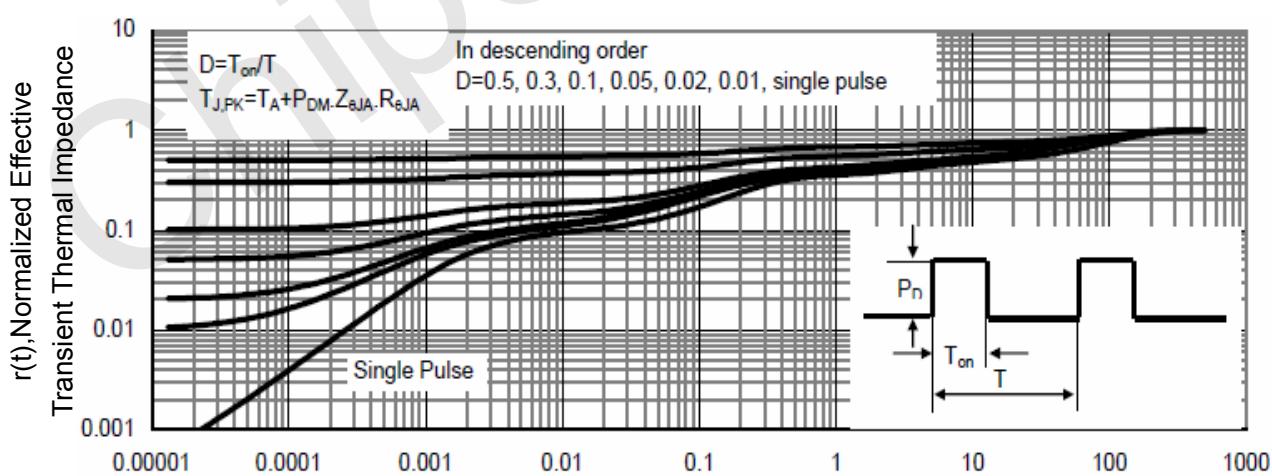


Figure 11 Normalized Maximum Transient Thermal Impedance



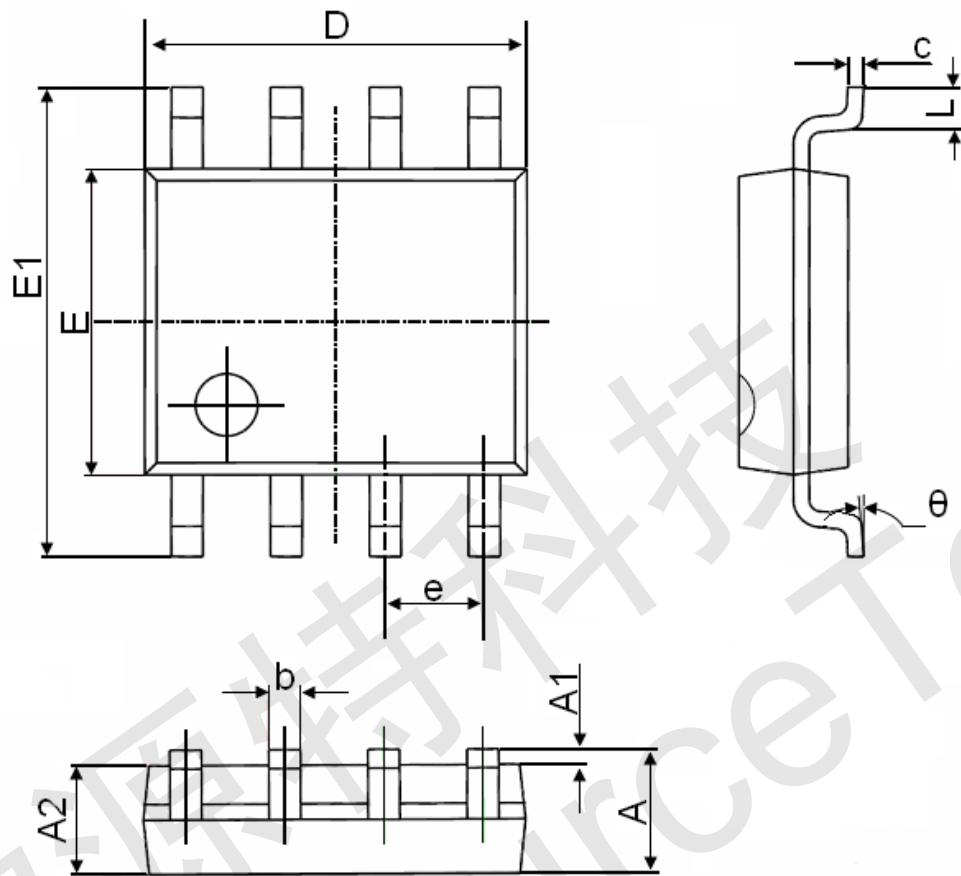
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SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°