PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

PE4249

SPST CATV MOSFET Switch

Features

- 75-ohm impedance switch
- Non-reflective at RF1, open reflective at RF2 when OFF
- 75-ohm (0.25 watt) termination
- High isolation: 85 dB at 5 MHz, 60 dB at 1 GHz
- Low insertion loss: 0.5 dB at 5 MHz, 0.8 dB at 1 GHz
- High input IP2: >80 dBm
- CMOS/TTL single-pin control
- Single +3 volt supply operation
- Extremely low bias: 33 µA @ 3V

Product Description

The PE4249 is a high-isolation MOSFET Switch designed for CATV applications, covering a broad frequency range from DC up to 1.3 GHz. This single-supply SPST switch integrates a single-pin CMOS control interface, and is non-reflective at port RF1 and open reflective at port RF2 when commanded OFF. It also provides low insertion loss with extremely low bias requirements while operating on a single 3-volt supply. In a typical CATV application, the high isolation PE4249 can replace bulky and expensive mechanical switches.

The PE4249 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

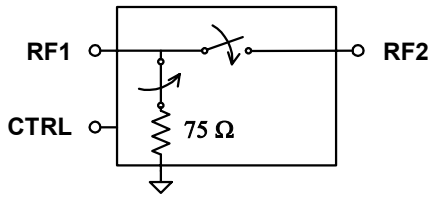


Figure 2. Pin Configuration

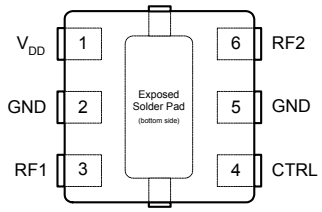


Table 1. Electrical Specifications @ +25 °C (Z_S = Z_L = 75 Ω)

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency[1]		DC		1300	MHz
Insertion Loss	DC – 50 MHz 1000 MHz		0.5 0.8	0.65 1.0	dB
Isolation	DC – 50 MHz 1000 MHz	80 58	85 60		dB
Return Loss	DC - 1000 MHz	16	20		dB
Input 1 dB Compression[2,4]	1000 MHz	30	33		dBm
Input IP2[2]	1000 MHz	80			dBm
Input IP3[2]	1000 MHz	50			dBm
Video Feedthrough[3]				15	mV_{pp}
Switching Time			2		µs

Notes: 1. Device linearity will begin to degrade below 1 MHz.
2. Measured in a 50 Ω system.
3. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.
4. Note Absolute Maximum ratings in Table 3.

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Nominal 3 V supply connection.[1]
2	GND	Ground connection. [3]
3	RF1	RF port. [2]
4	CTRL	CMOS or TTL logic level: High = RF1 to RF2 signal path Low = RF1 isolated from RF2
5	GND	Ground connection. [3]
6	RF2	RF port. [2]

Notes: 1. A bypass capacitor should be placed as close as possible to the pin.
2. Both RF pins must be DC blocked by an external capacitor or held at 0 V_{DC}.
3. The exposed pad must be soldered to the ground plane for proper switch performance.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on CTRL input	-0.3	5.5	V
T_{ST}	Storage temperature	-65	150	°C
T_{OP}	Operating temperature	-40	85	°C
P_{IN}	Input power (50Ω), CTRL=1/CTRL=0		33/24	dBm
V_{ESD}	ESD voltage (Human Body Model)		500	V

Table 4. DC Electrical Specifications @ 25 °C

Parameter	Min	Typ	Max	Unit
V_{DD} Power Supply	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		33	40	µA
Control Voltage High	70% V_{DD}		5	V
Control Voltage Low	0		30% V_{DD}	V

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Device Description

The PE4249 high isolation SPST CATV Switch is designed to support CATV applications such as premium channel service connect/disconnect switch blocks. This function is typically performed by bulky and expensive mechanical switches. The high isolation characteristics (60 dB at 1 GHz, 85 dB at 5 MHz), high compression point, and an integrated 75 Ω (0.25 watt) input termination make the PE4249 an ideal, low cost solution.

Figure 3. Typical Application Block Diagram

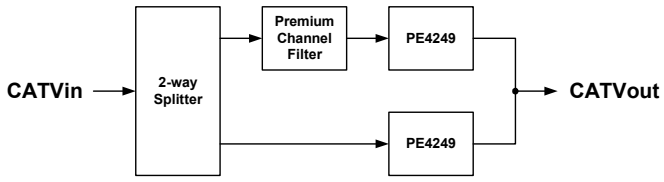


Table 5. Truth Table

Control Voltage (CTRL)	Signal Path (RF1 to RF2)
High[1]	ON
Low	OFF

Notes: 1. CTRL accepts both CMOS and TTL voltage leads.

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)
(75-ohm impedance except as indicated)

Figure 4. Insertion Loss

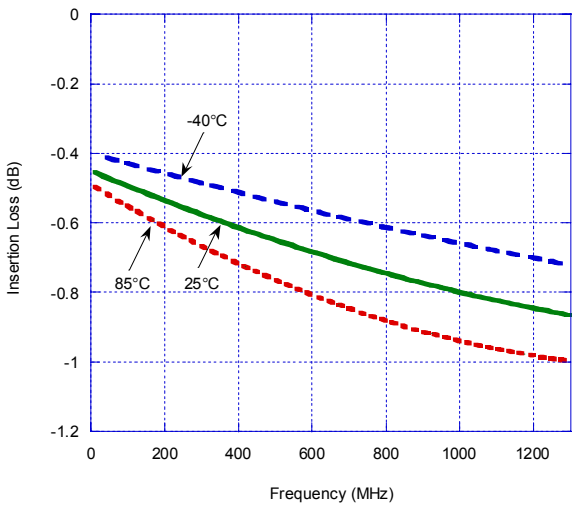


Figure 5. Input 1 dB Compression Point & IIP3 (50-ohm system impedance)

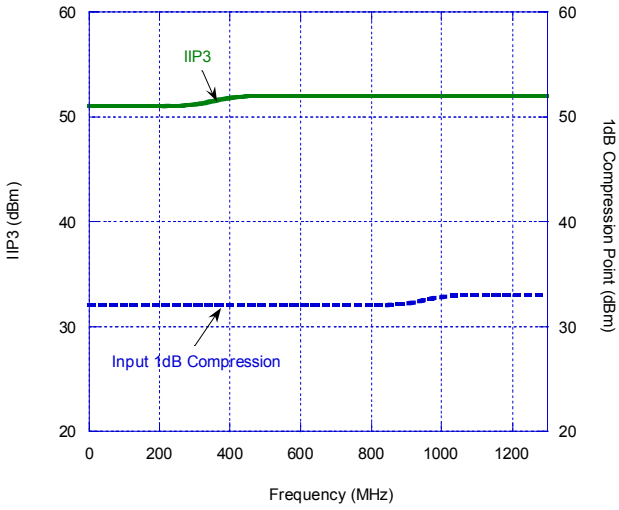
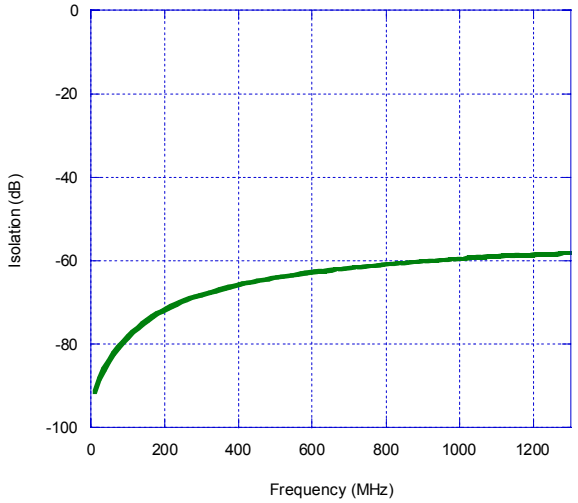


Figure 6. Isolation



Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)
(75-ohm impedance)

Figure 7. RF1 Return Loss (Switch = ON)

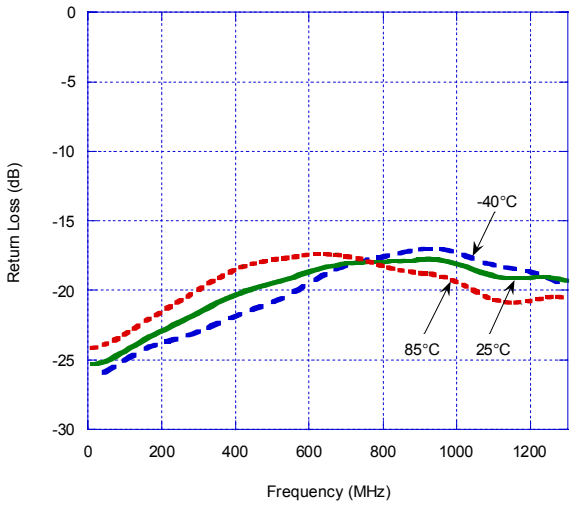


Figure 8. RF2 Return Loss (Switch = OFF)

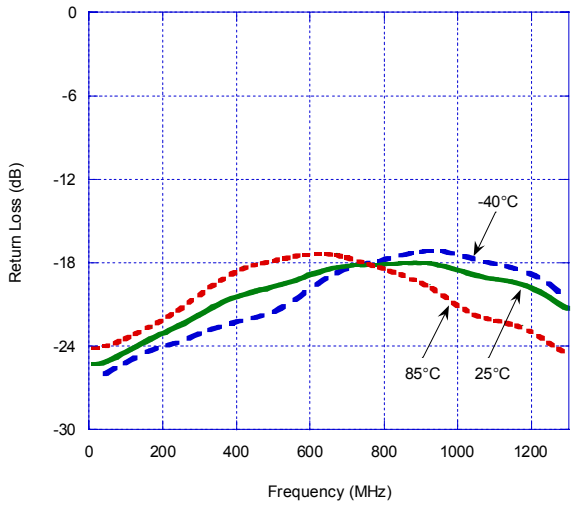
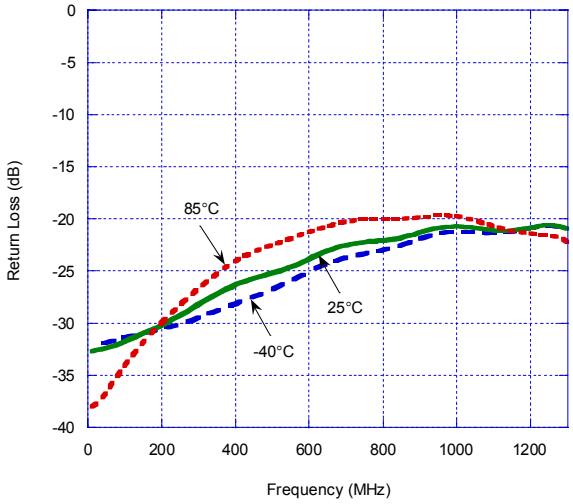


Figure 9. RF1 Return Loss (Switch = OFF)



Evaluation Kit Information

Evaluation Kit

The SPST Switch Evaluation Kit board was designed to ease customer evaluation of the PE4249 SPST switch. The RF1 port is connected through a 75Ω transmission line to the top left BNC connector, J1. The RF2 port is connected through a 75Ω transmission line to the BNC connector on the top right side of the board, J2. A through transmission line connects BNC connectors J3 and J4. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide model with trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.3. Note that the predominate mode for these transmission lines is coplanar waveguide with a ground plane.

J5 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J5-3) is connected to the device V_{DD} input. The fourth pin to the right (J5-7) is connected to the device CTRL input. A decoupling capacitor (100 pF) is provided on both traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 10. Evaluation Board Layouts

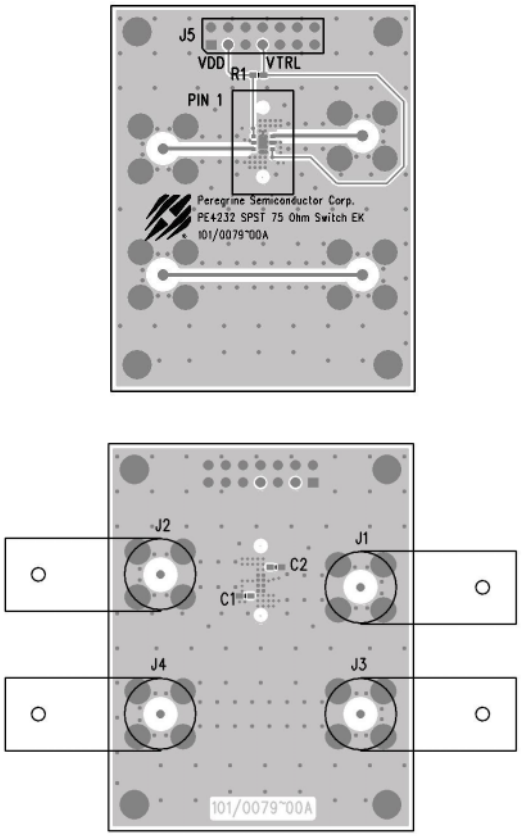


Figure 11. Evaluation Board Schematic

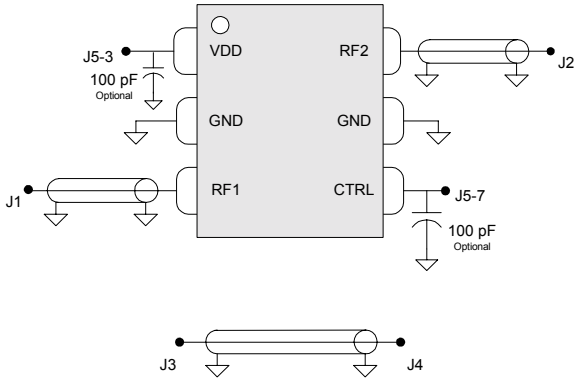
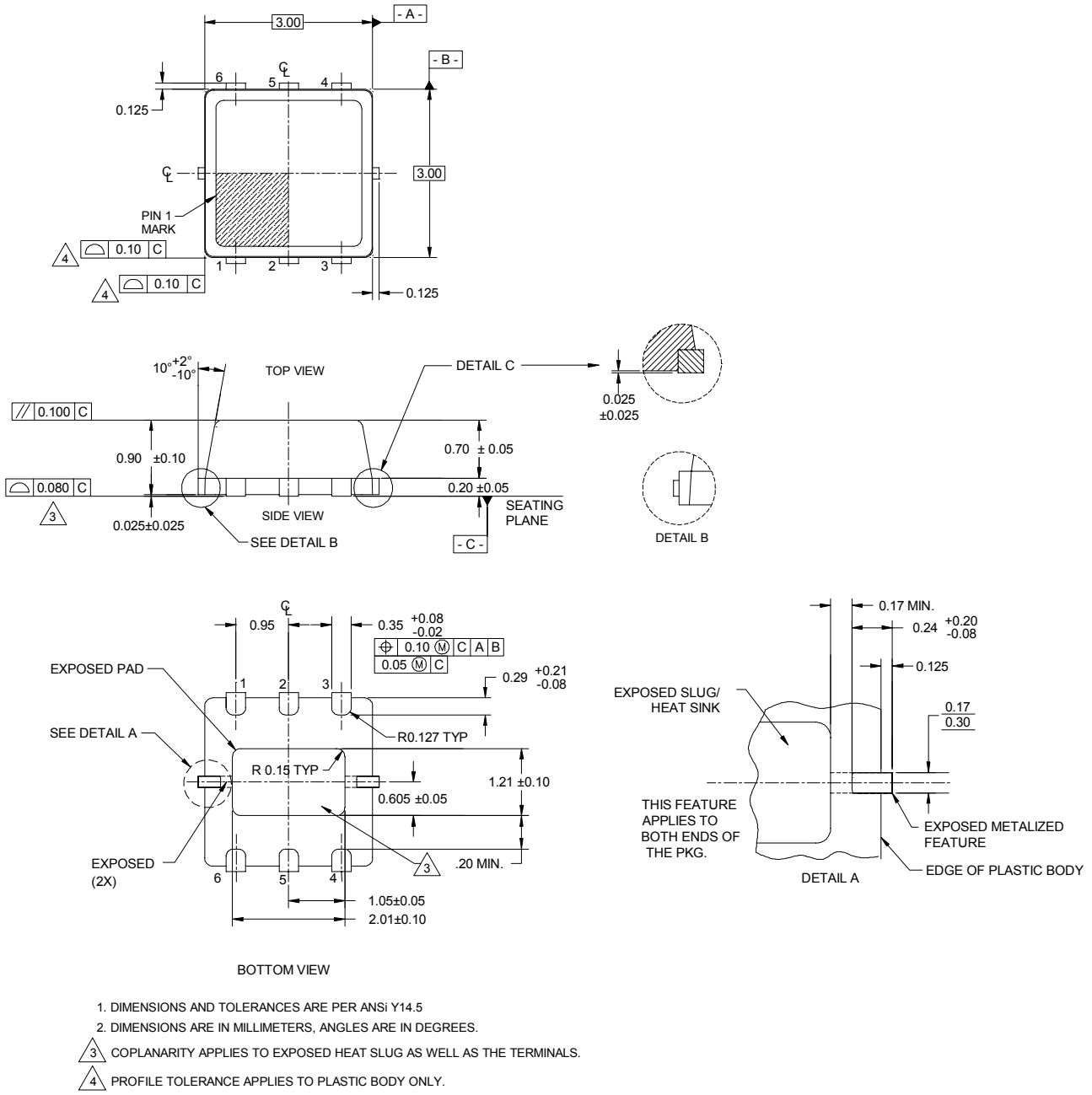


Figure 12. Package Drawing

6-lead MLPM



1. DIMENSIONS AND TOLERANCES ARE PER ANSi Y14.5
2. DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
3. COPLANARITY APPLIES TO EXPOSED HEAT SLUG AS WELL AS THE TERMINALS.
4. PROFILE TOLERANCE APPLIES TO PLASTIC BODY ONLY.

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4249-01	4249	PE4249-06MLP3x3-12800F	6-lead 3x3mm MLPM	12800 units / Canister
4249-02	4249	PE4249-06MLP3x3-3000C	6-lead 3x3mm MLPM	3000 units / T&R
4249-00	PE4249-EK	PE4249-06MLP3x3-EK	Evaluation Board	1 / Box

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For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents are pending.