Peregrine Semiconductor

Product Specification

PE4272

SPDT Broadband UltraCMOS™ DC – 3 GHz RF Switch

Features

- High ESD tolerance of 1.5 kV
- Single-pin CMOS logic control
- Low insertion loss: 0.5 dB at 1000 MHz, 0.6 dB at 2000 MHz
- Isolation of 43 dB at 1000 MHz, 33.5 dB at 2000 MHz
- Typical input 1 dB compression point of +32 dBm
- Small 8-lead MSOP package

Product Description

The PE4272 RF Switch is designed for the TV tuner, PCTV, set top box, DTV, DVR and general broadband applications. This device offers industry leading broadband linearity, 1.5 kV ESD tolerance and a simple CMOS interface. The device offers a simple alternative solution to pin diode and mechanical relay switches.

The PE4272 SPDT High Power RF Switch is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

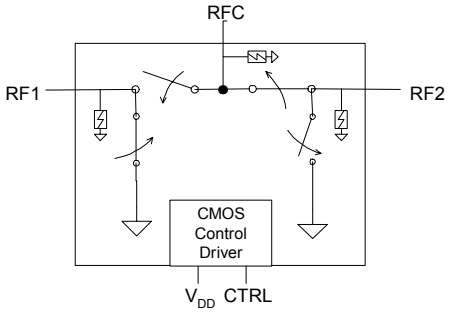


Figure 2. Package Type

8-lead MSOP

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 75 Ω)

Parameter	Conditions	Min	Typ	Max	Units
Operation Frequency[1]	DC – 3000				MHz
Insertion Loss	1000 MHz 2000 MHz		0.5 0.6	0.6 0.7	dB
Isolation – RFC to RF1/RF2	1000 MHz 2000 MHz	41 31.5	43 33.5		dB
Isolation – RF1 to RF2	1000 MHz 2000 MHz	41 32	43 34		dB
Return Loss	1000 MHz 2000 MHz		19.5 16		dB
'ON' Switching Time[3]	50% CTRL to 0.1 dB final value, 2 GHz		500	1000	ns
'OFF' Switching Time[3]	50% CTRL to 25 dB isolation, 2 GHz		500	1000	ns
Video Feedthrough[2,3]			<3		mV_{pp}
Input 1 dB Compression[3]	1000 MHz	30	32		dBm
Input IP3[3]	1000 MHz, 20 dBm input power		52		dBm

Notes: 1. Device linearity will begin to degrade below 5 MHz.
2. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.
3. Measured in a 50 Ω system.

Figure 3. Pin Configuration (Top View)

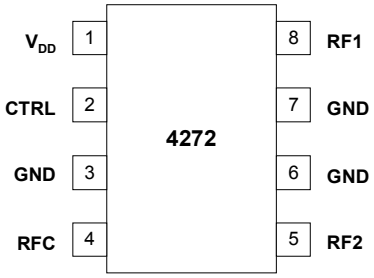


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Nominal +3 V supply connection.
2	CTRL	CMOS logic level: High = RFC to RF1 signal path Low = RFC to RF2 signal path
3	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
4	RFC	RF Common port.[4]
5	RF2	RF2 port.[4]
6	GND	Ground Connection. Traces should be physically short and connected to ground plane for best performance.
7	GND	Ground Connection. Traces should be physically short and connected to ground plane for best performance.
8	RF1	RF1 port.[4]

Note: 4. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3 V, CTRL = 3 V)		8	20	µA
Operating temperature range	-40		85	°C
Control Voltage High	$0.7xV_{DD}$			V
Control Voltage Low			$0.3xV_{DD}$	V

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50 Ω)		34	dBm
V_{ESD}	ESD voltage (HBM, ML_STD 883 Method 3015.7)		1500	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the Operating Ranges table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 1 (V_{DD}) = V_{DD} Pin 2 (CTRL) = High	RFC to RF1
Pin 1 (V_{DD}) = V_{DD} Pin 2 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 1 (V_{DD}) = Low Pin 2 (CTRL) = High	RFC to RF1
Pin 1 (V_{DD}) = High Pin 2 (CTRL) = Low	RFC to RF2

Control Logic Input

The PE4272 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 2) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection (pin 1). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS µProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and V_{DD} (pins 2 & 1), that can be directly driven by +3-volt CMOS logic or a suitable µProcessor I/O port. This enables the PE4272 to operate in positive control voltage mode within the PE4272 operating limits.

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4272 SPDT switch. The RF common port is connected through a 75 Ω transmission line to the bottom F connector, J2. Port 1 and Port 2 are connected through 75 Ω transmission lines to two F connectors on either side of the board, J1 and J3. A through transmission line connects F connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", copper thickness of 0.0021" and ε_r of 4.3.

J6 provides a means for controlling the DC inputs to the device. The lower right pin (J6-2) is connected to the device CTRL input. The upper right pin (J6-1) is connected to the device V_{DD} input. Footprints for decoupling capacitors are provided on both CTRL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 4. Evaluation Board Layouts
Peregrine specification 101/0243

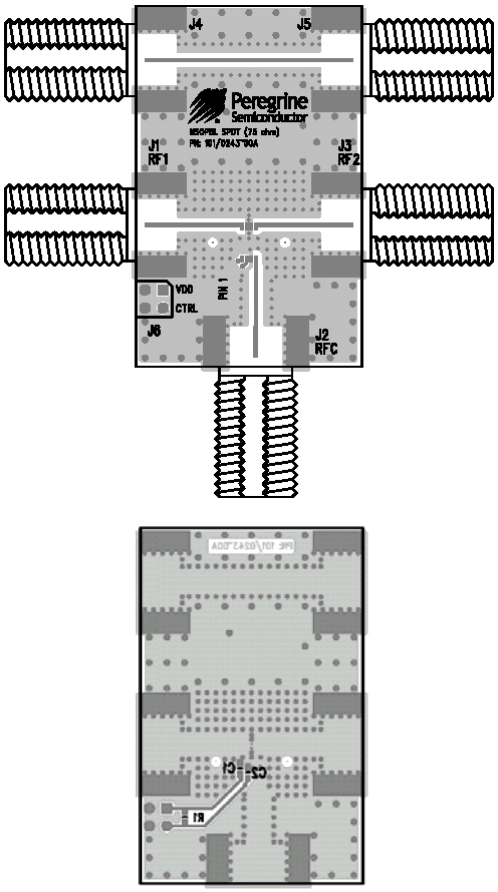
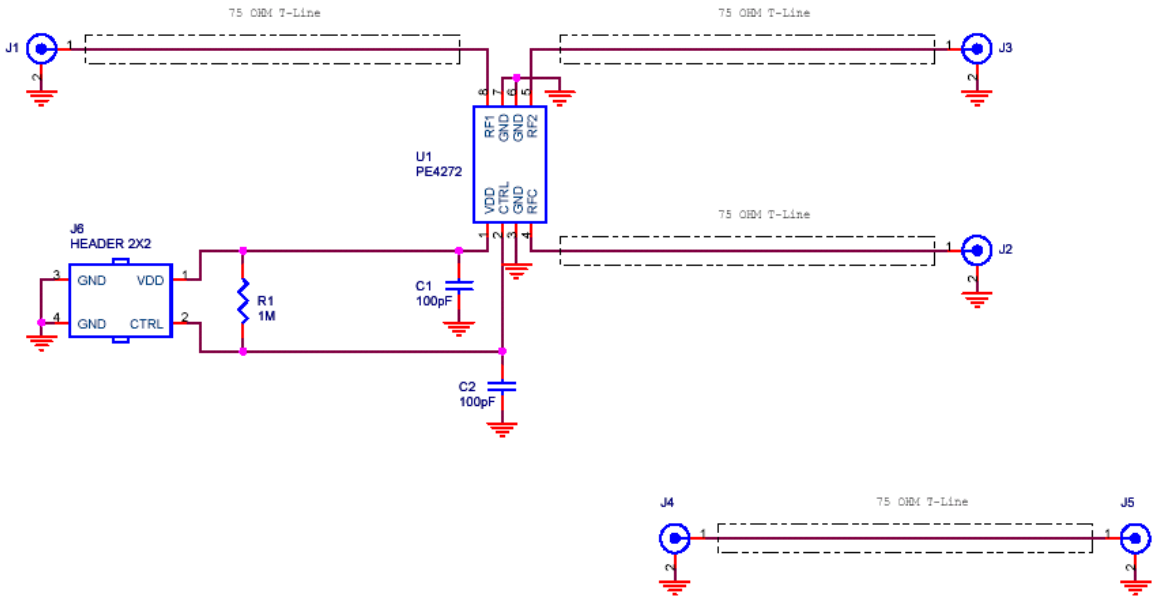


Figure 5. Evaluation Board Schematic
Peregrine specification 102/0309



Typical Performance Data

Figure 6. Insertion Loss: RFC-RF1 @ 25 °C

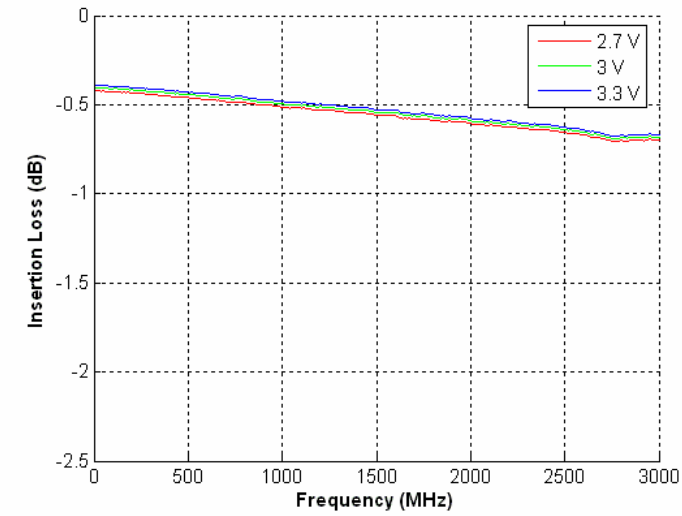


Figure 7. Insertion Loss: RFC-RF1 @ 3 V

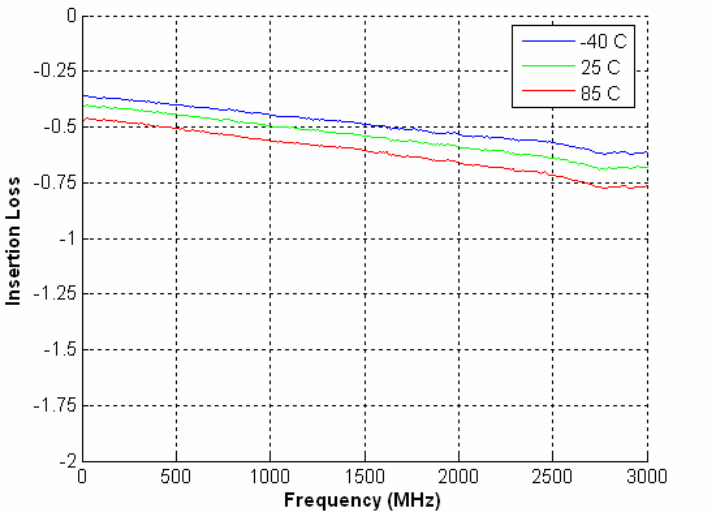


Figure 8. Insertion Loss: RFC-RF2 @ 25 °C

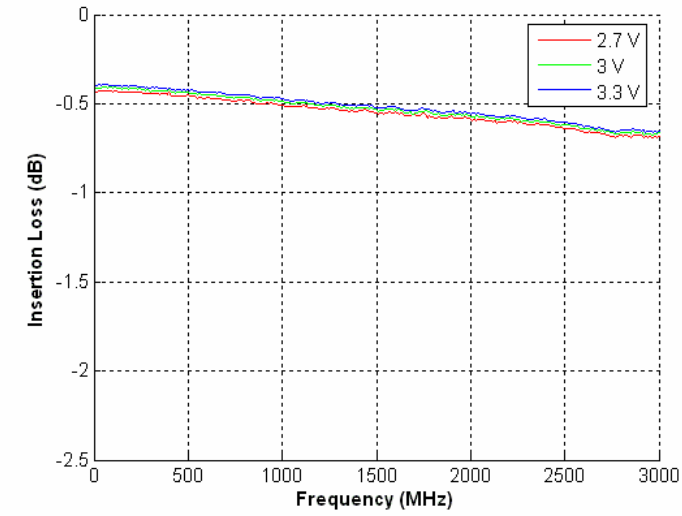
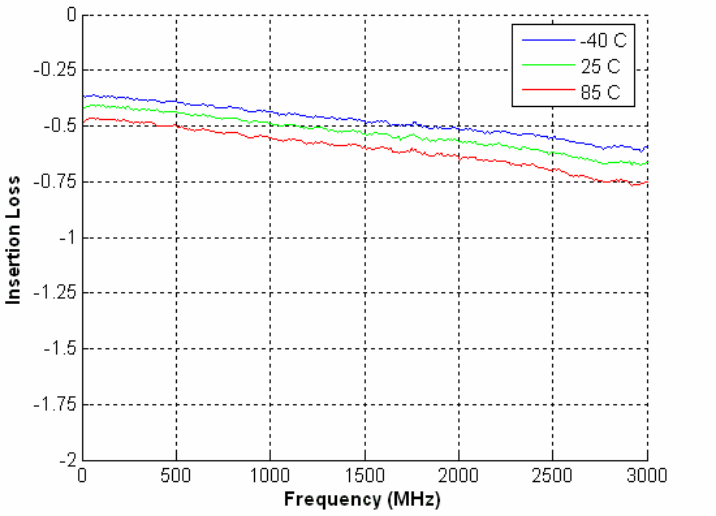


Figure 9. Insertion Loss: RFC-RF2 @ 3 V



Typical Performance Data

Figure 10. Isolation: RFC-RF1 @ 25 °C

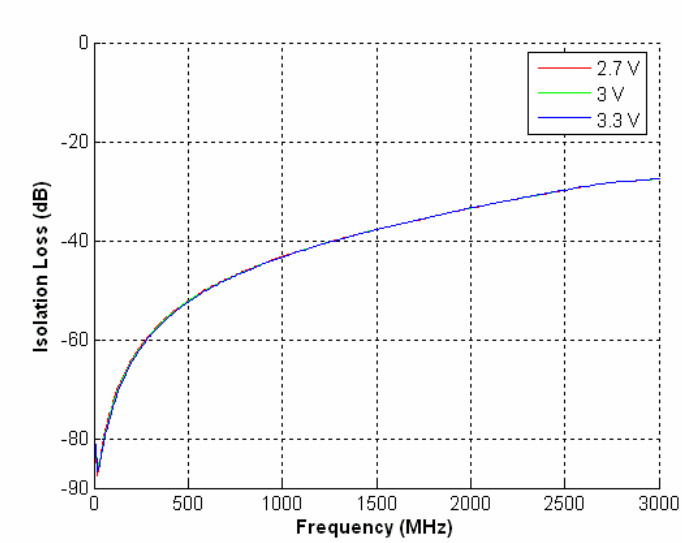


Figure 11. Isolation: RFC-RF1 @ 3 V

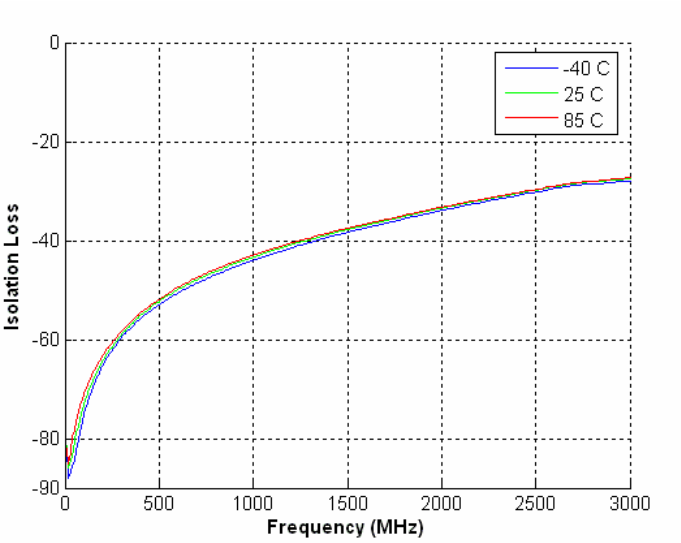


Figure 12. Isolation: RFC-RF2 @ 25 °C

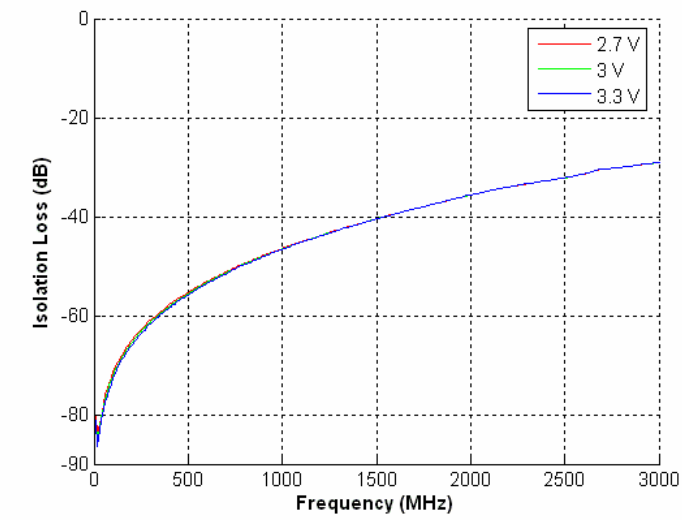
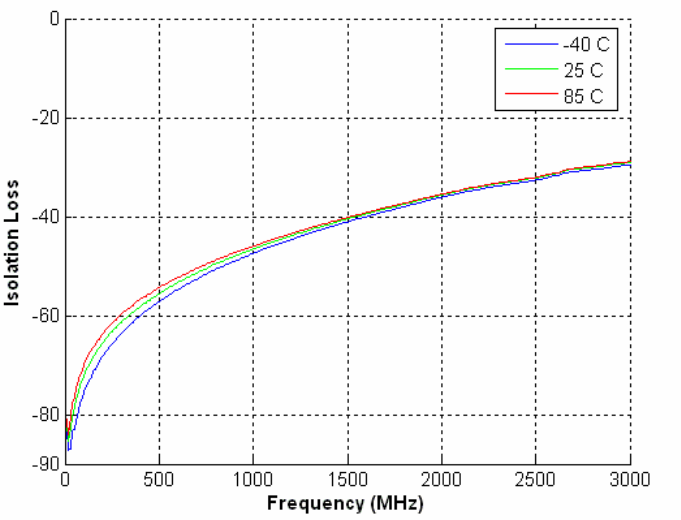


Figure 13. Isolation: RFC-RF2 @ 3 V



Typical Performance Data

Figure 14. Isolation: RF1-RF2 @ 25 °C

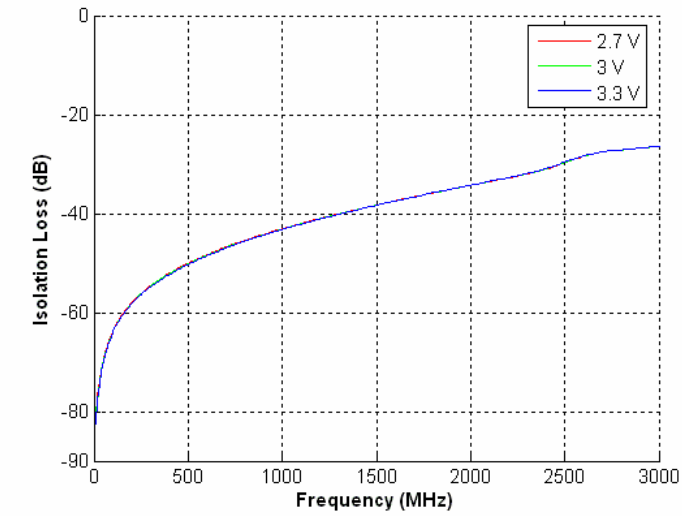


Figure 15. Isolation: RF1-RF2 @ 3 V

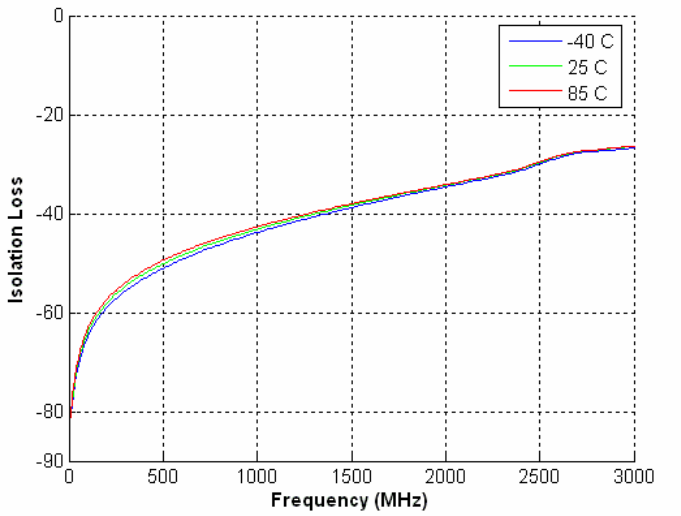


Figure 16. Return Loss: RFC-RF1 @ 25 °C

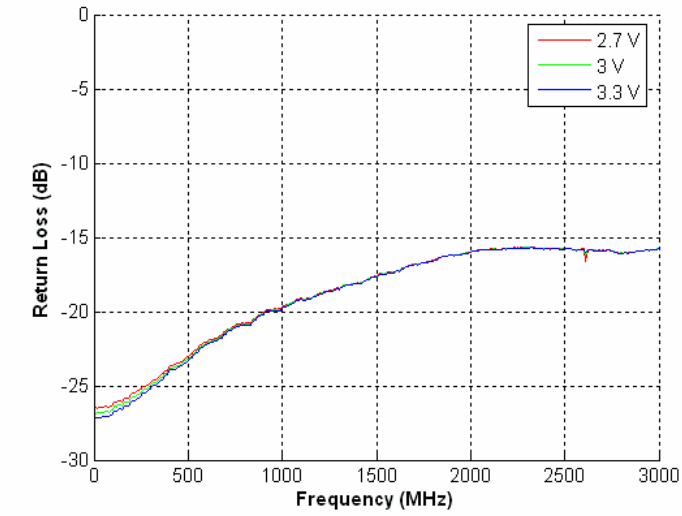
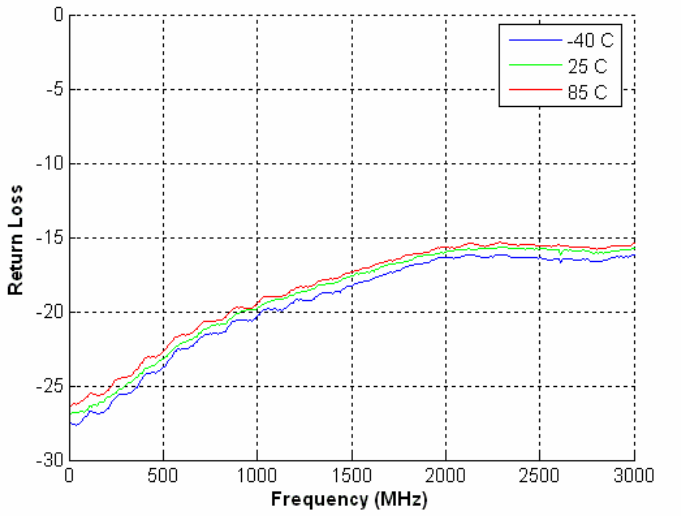


Figure 17. Return Loss: RFC-RF1 @ 3 V



Typical Performance Data

Figure 18. Return Loss: RFC-RF2 @ 25 °C

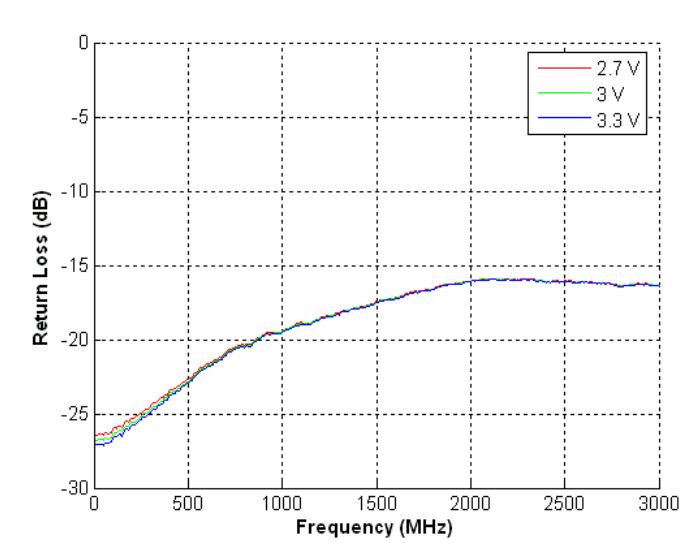


Figure 19. Return Loss RFC-RF2 @ 3 V

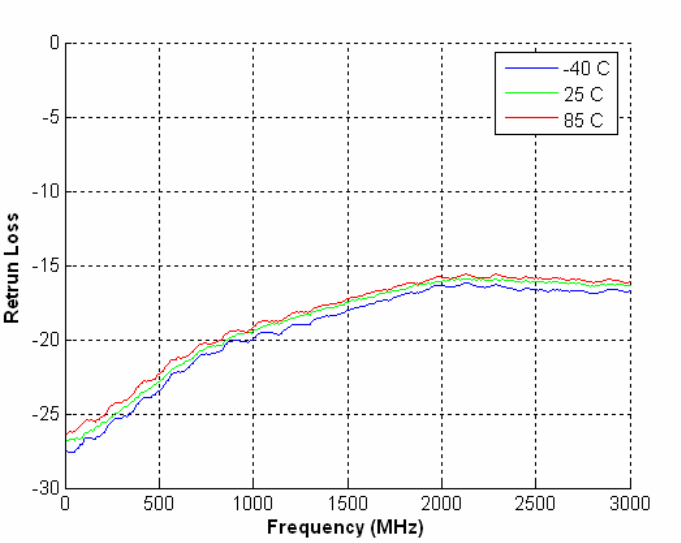


Figure 20. Return Loss: RFC-RF1/RF2 @ 25 °C

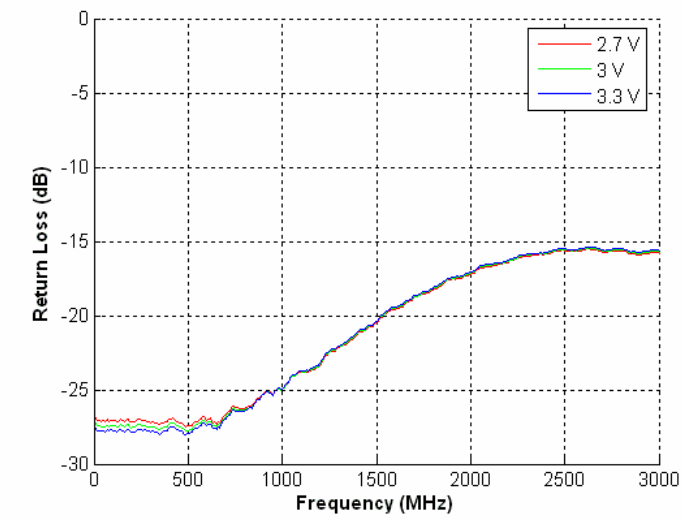


Figure 21. Return Loss: RFC-RF1/RF2 @ 3 V

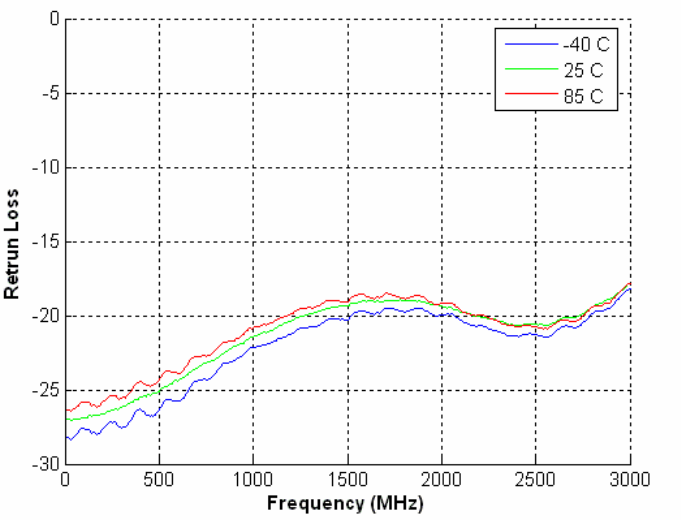


Figure 22. Package Drawing

8-lead MSOP

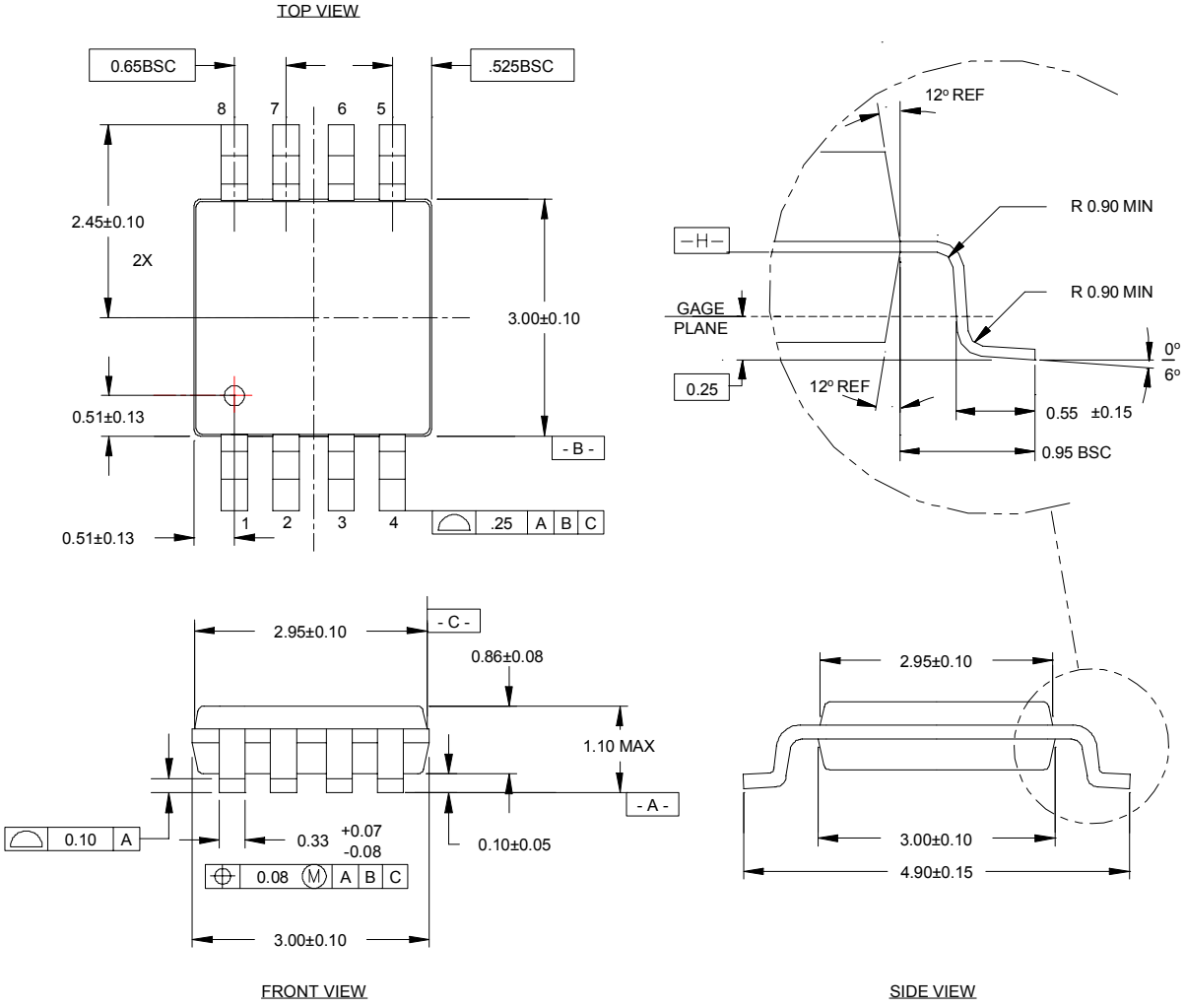
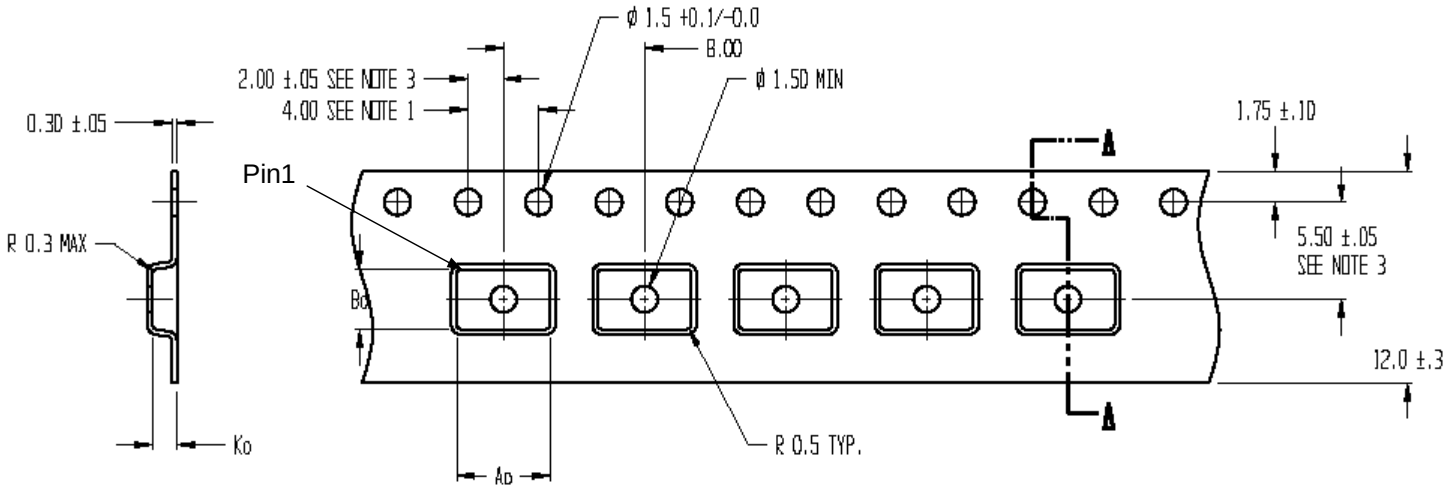


Figure 23. Tape and Reel Specifications

8-lead MSOP



Ao = 5.3D
Bo = 3.4D
Ko = 1.4D

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4272-01	4272	PE4272-08MSOP-50A	8-lead MSOP	50 units / Tube
4272-02	4272	PE4272-08MSOP-2000C	8-lead MSOP	2000 units / T&R
4272-00	PE4272-EK	PE4272-08MSOP-EK	Evaluation Kit	1 / Box
4272-51	4272	PE4272G-08MSOP-50A	Green 8-lead MSOP	50 units / Tube
4272-52	4272	PE4272G-08MSOP-2000C	Green 8-lead MSOP	2000 units / T&R

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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