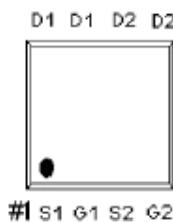


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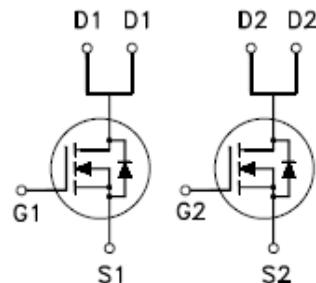
Dual N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D^3
30V	19mΩ @ $V_{GS} = 10V$	21A



G : GATE
D : DRAIN
S : SOURCE



PDFN 3X3S

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ³	I_D	21	A
		13	
		7.5	
		6	
Pulsed Drain Current ¹	I_{DM}	25	
Avalanche Current	I_{AS}	17	
Avalanche Energy	E_{AS}	15	mJ
Power Dissipation	P_D	14	W
		5	
		1.7	
		1.1	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$	70	8.5	°C / W
Junction-to-Case	$R_{\theta JC}$			

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

³Package limitation current is 9A.

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Dual N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1	1.5	2.5	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 24\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{\text{D}(\text{ON})}$	$V_{\text{DS}} = 5\text{V}, V_{\text{GS}} = 10\text{V}$	25			A
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 4.5\text{V}, I_D = 6.8\text{A}$		20	25	$\text{m}\Omega$
		$V_{\text{GS}} = 10\text{V}, I_D = 7.5\text{A}$		17	19	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 10\text{V}, I_D = 7.5\text{A}$		22		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1\text{MHz}$		526		pF
Output Capacitance	C_{oss}			76		
Reverse Transfer Capacitance	C_{rss}			62		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		2.2		Ω
Total Gate Charge ²	$Q_g(V_{\text{GS}}=10\text{V})$	$V_{\text{DS}} = 15\text{V}, I_D = 7.5\text{A}$		14.4		nC
	$Q_g(V_{\text{GS}}=4.5\text{V})$			7.8		
Gate-Source Charge ²	Q_{gs}			2		
Gate-Drain Charge ²	Q_{gd}			3.8		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 15\text{V}, I_D \approx 7.5\text{A}, V_{\text{GEN}} = 10\text{V}, R_G = 6\Omega$		14		nS
Rise Time ²	t_r			10		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			30		
Fall Time ²	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current ³	I_S				21	A
Forward Voltage ¹	V_{SD}	$I_F = 7.5\text{A}, V_{\text{GS}} = 0\text{V}$			1	V
Reverse Recovery Time	t_{rr}	$I_F = 7.5\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		12		nS
Reverse Recovery Charge	Q_{rr}			3		nC

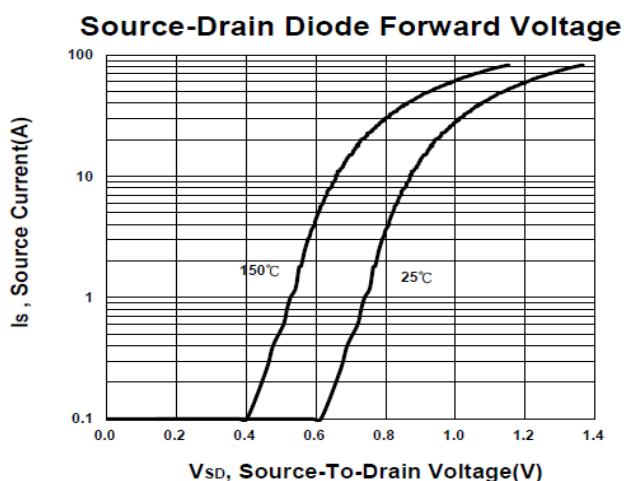
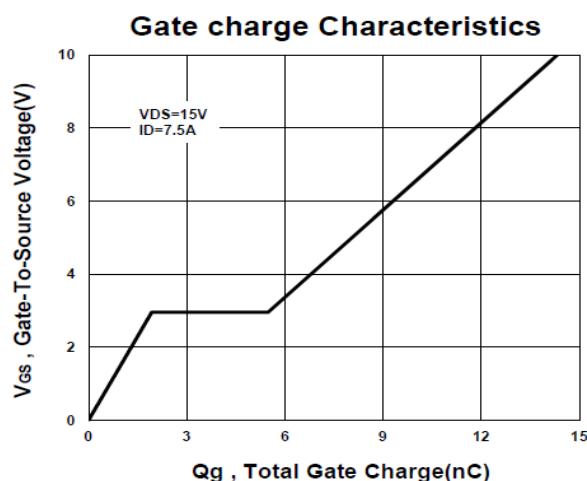
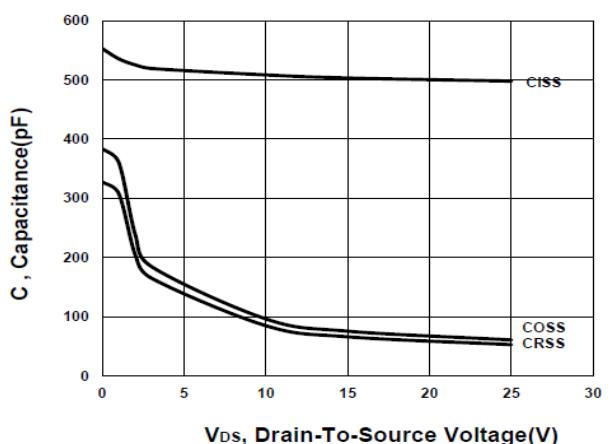
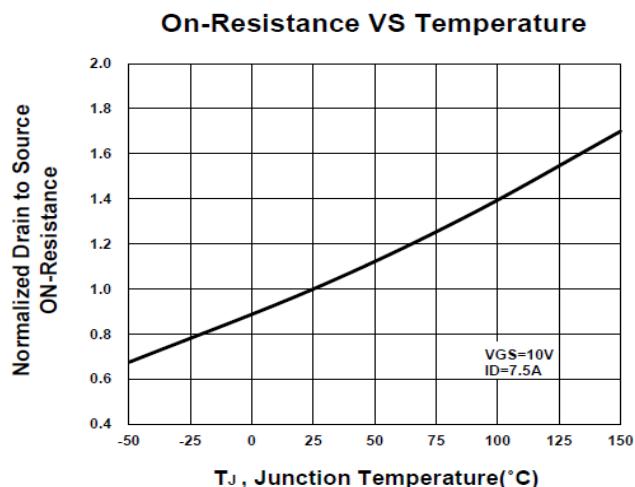
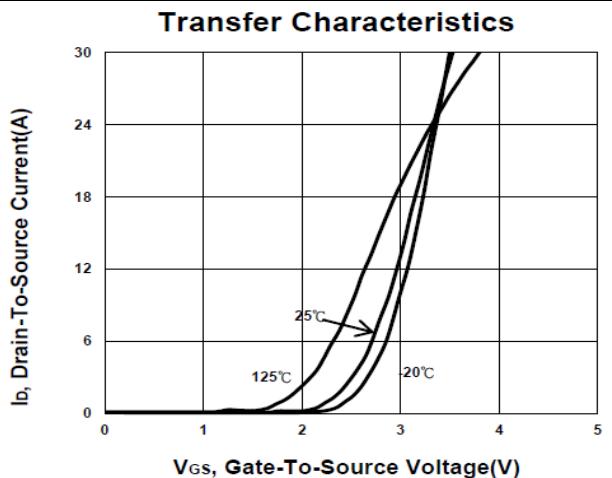
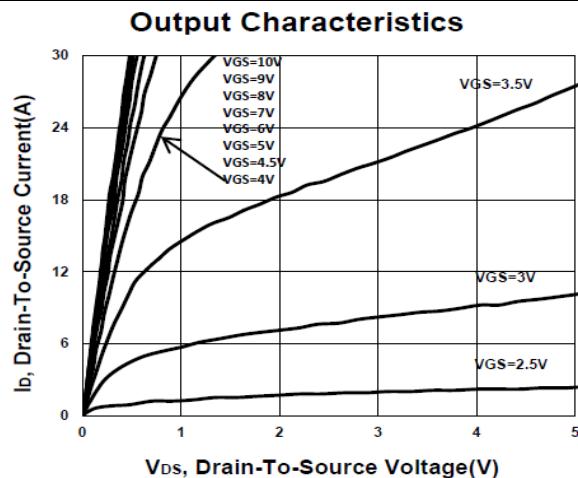
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Package limitation current is 9A.

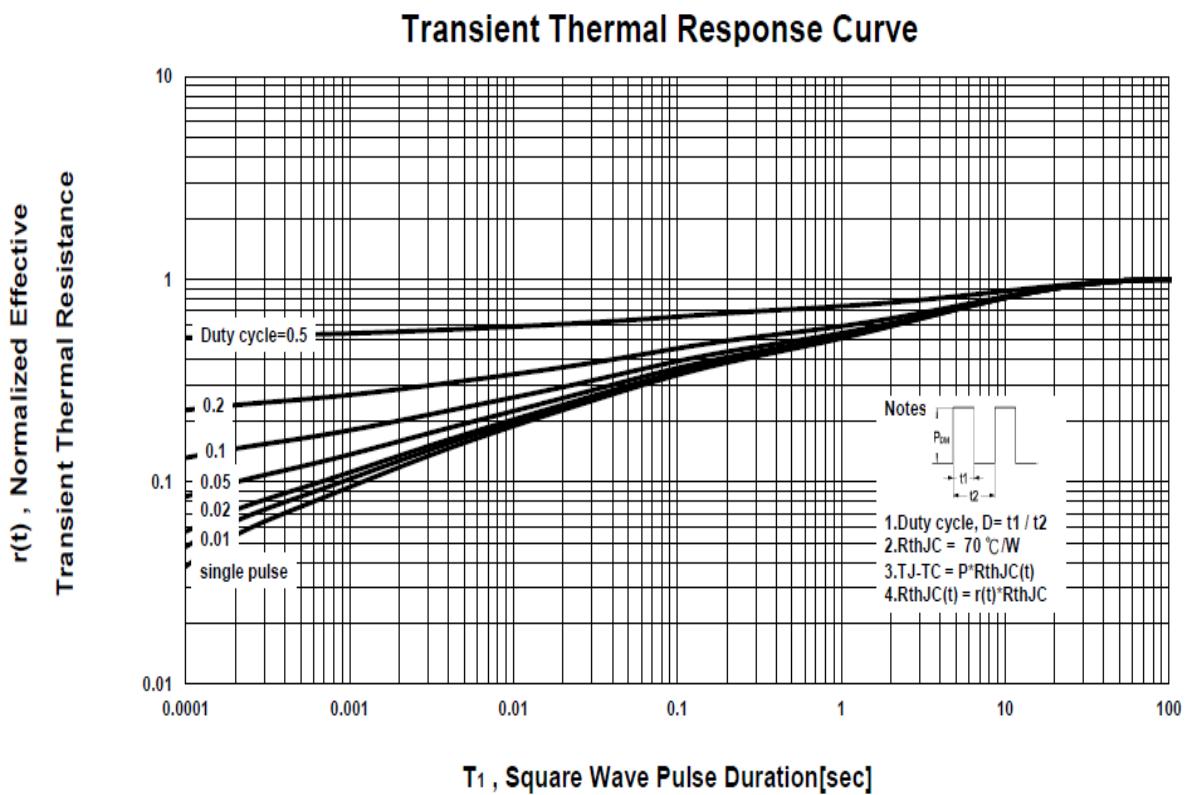
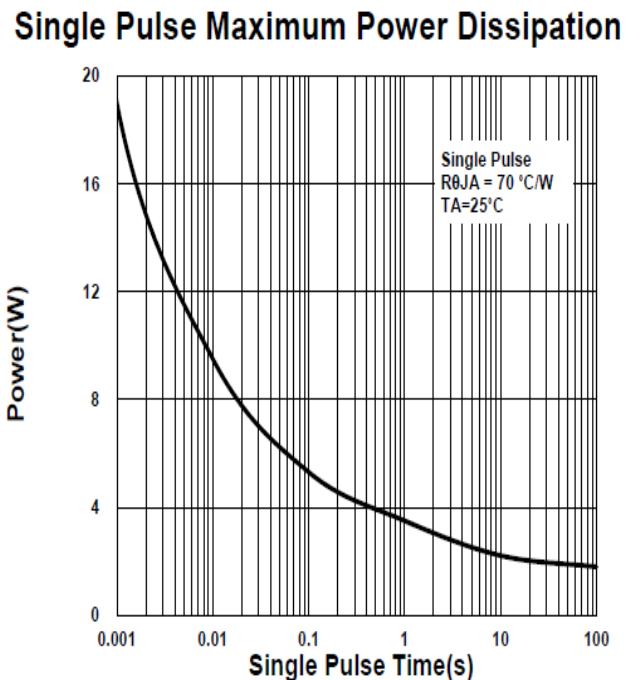
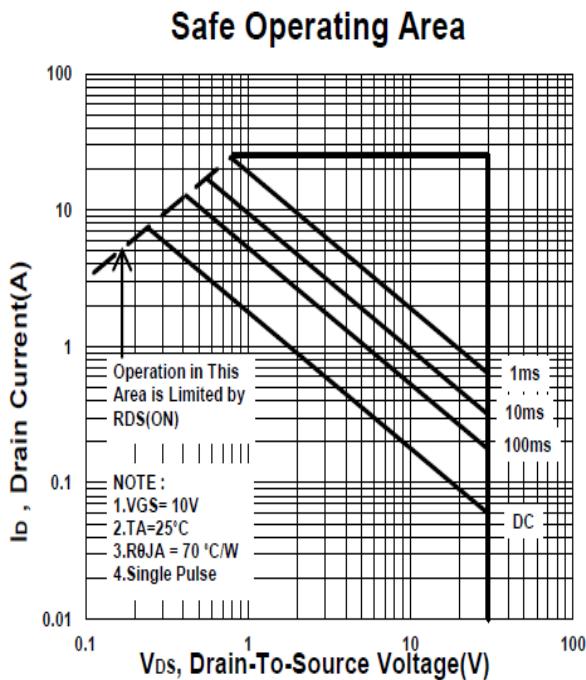
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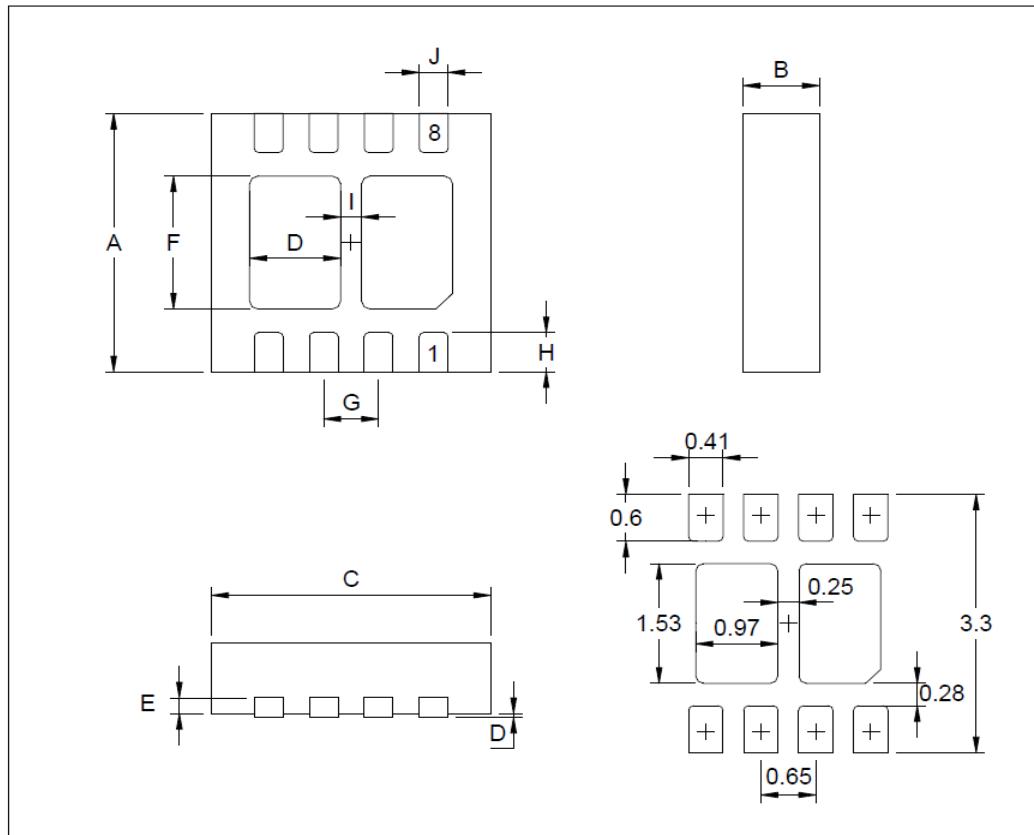
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Dual N-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 3x3S(Dual) MECHANICAL DATA

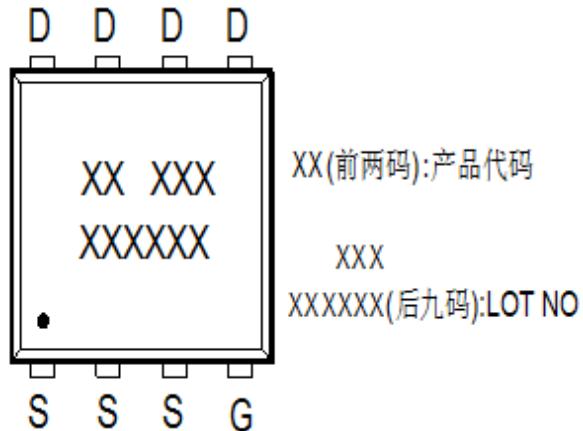
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.9		3.1	G		0.65	
B	0.8		0.9	H	0.37		0.47
C	2.9		3.1	I		0.25	
D	0		0.05				
E	0.195		0.211				
F	1.65		1.75				



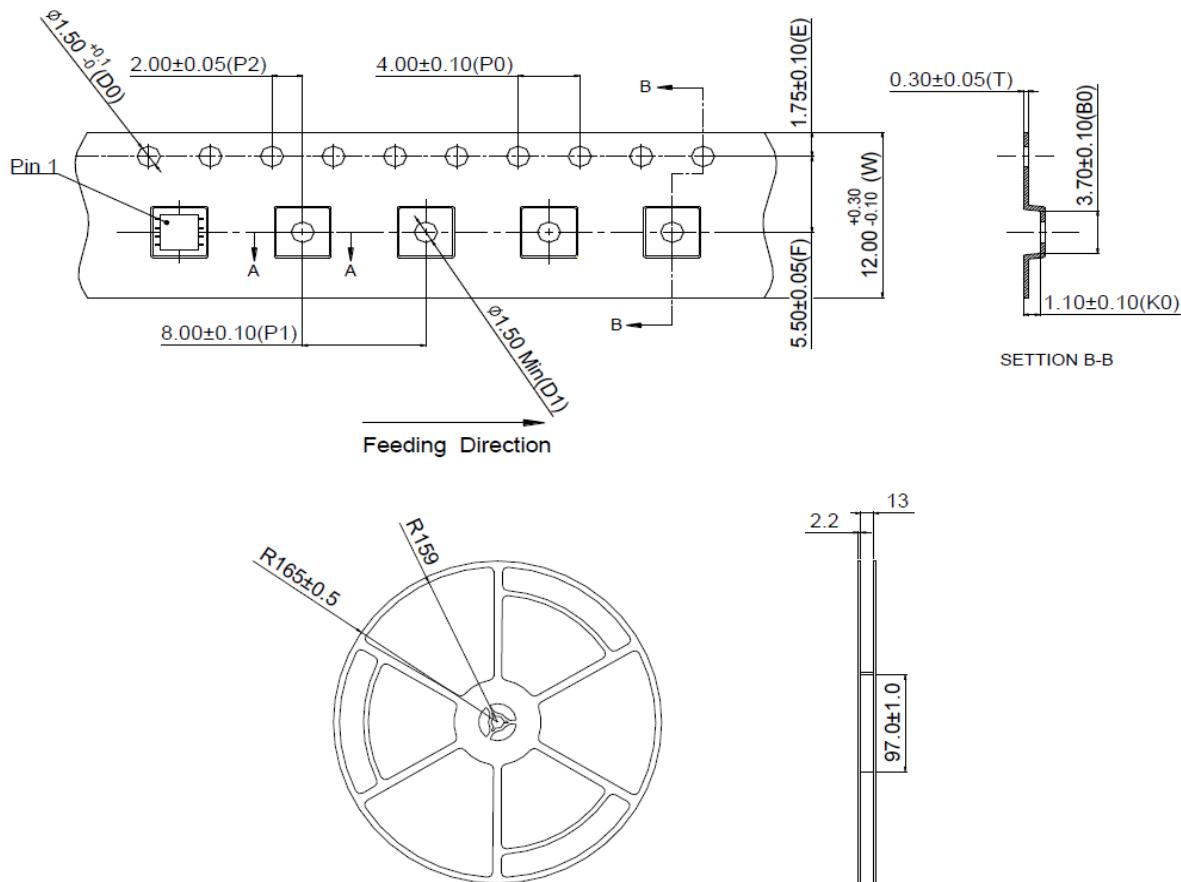
PE532DY

Dual N-Channel Enhancement Mode MOSFET

A. Marking Information(此产品代码为: E7)



B. Tape&Reel Information:5000pcs/Reel

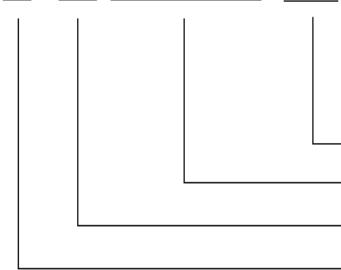


PE532DY **Dual N-Channel Enhancement Mode MOSFET**

C. Lot.No. & Date Code rule

1.LOT.NO.

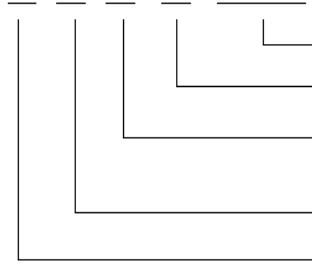
M N 15M21 03



- #8~9 Sub-lot No
- Order series no.
- Foundry site
- Assembly site

2.Date Code

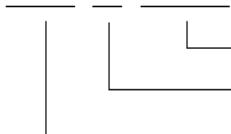
D Y M X XXX



- Order series no. & Sub-lot No
- Week
- M : Month (A:Jan , B:Feb , C:Mar ,D :Apr ,E:May ,F:Jun,G:Jul,H:Aug,I:Sep,J:Oct,K:Nov,L:Dec.)
- Y : Year (N : 2011, O : 2012 ...)
- Assembly site

3.Date Code (for Small package)

XX Y WW



- Week
- Y : Year (9: 2009,A : 2010, B : 2011 ...)
- Device Name

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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / ” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least