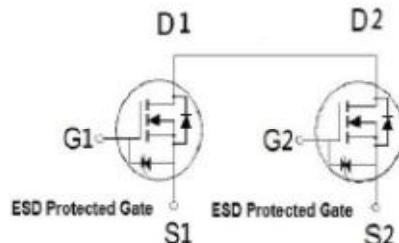
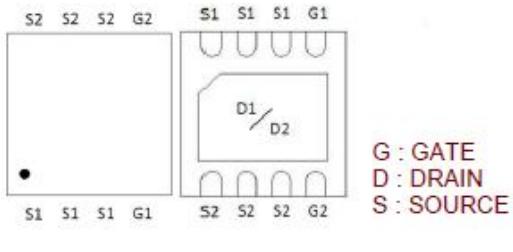


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Dual N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
20V	8.5mΩ @ $V_{GS} = 4.5V$	39A



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ²	I_D	39	A
		24	
		12	
		9.7	
Pulsed Drain Current ¹	I_{DM}	60	
Avalanche Current	I_{AS}	23.5	
Avalanche Energy	E_{AS}	27.6	mJ
Power Dissipation	P_D	23	W
		9.4	
		2.2	
		1.4	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ³	$R_{\theta JA}$	55	5.3	°C / W
Junction-to-case	$R_{\theta JC}$			

¹Pulse width limited by maximum junction temperature.

²Package limitation current is 24A.

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	0.35	0.67	1	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 8\text{V}$			± 30	uA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 16\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 4.5\text{V}, I_D = 3\text{A}$	5.1	6.8	8.5	mΩ
		$V_{\text{GS}} = 3.8\text{V}, I_D = 3\text{A}$	5.4	7.2	9	
		$V_{\text{GS}} = 3.1\text{V}, I_D = 3\text{A}$	5.7	7.6	9.5	
		$V_{\text{GS}} = 2.5\text{V}, I_D = 3\text{A}$	6.3	8.4	10.5	
		$V_{\text{GS}} = 1.8\text{V}, I_D = 3\text{A}$	7	11	15	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 5\text{V}, I_D = 3\text{A}$		32		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 10\text{V}, f = 1\text{MHz}$		1589		pF
Output Capacitance	C_{oss}			214		
Reverse Transfer Capacitance	C_{rss}			165		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		2.3		Ω
Total Gate Charge ²	$Q_{\text{g}}(\text{VGS}=4.5\text{V})$	$V_{\text{DS}} = 10\text{V}, I_D = 3\text{A}$		18.5		nC
	$Q_{\text{g}}(\text{VGS}=3.8\text{V})$			16		
Gate-Source Charge ²	Q_{gs}			1.7		
Gate-Drain Charge ²	Q_{gd}			4.5		
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 10\text{V}$ $I_D \approx 3\text{A}, V_{\text{GEN}} = 4.5\text{V}, R_G = 6\Omega$		38		nS
Rise Time ²	t_r			42		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			60		
Fall Time ²	t_f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current ³	I_S				1.8	A
Forward Voltage ¹	V_{SD}	$I_F = 3\text{A}, V_{\text{GS}} = 0\text{V}$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 3\text{A}, dI_F/dt = 100\text{A} / \mu\text{s}$		24		nS
Reverse Recovery Charge	Q_{rr}			8		nC

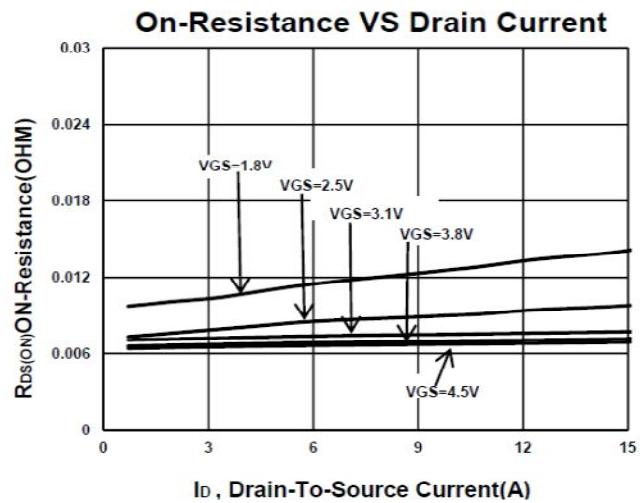
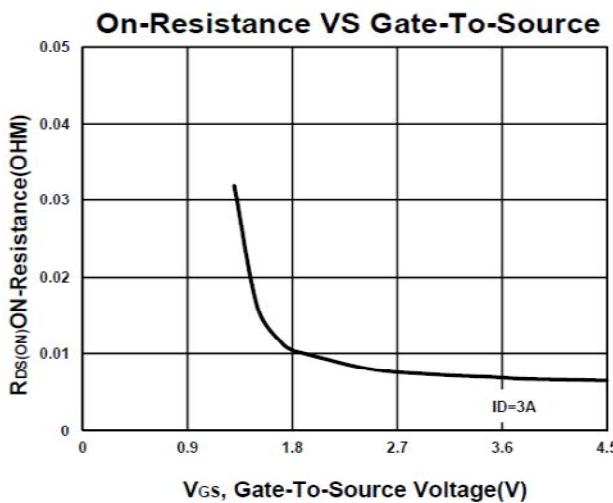
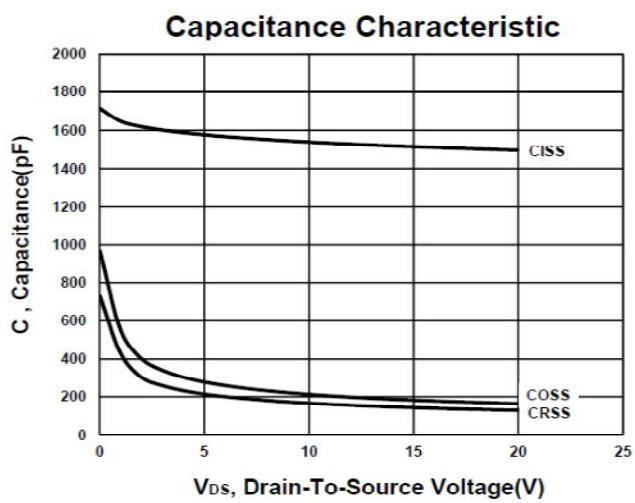
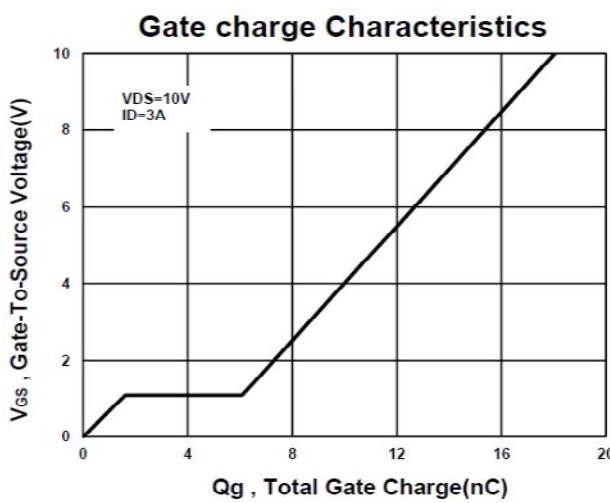
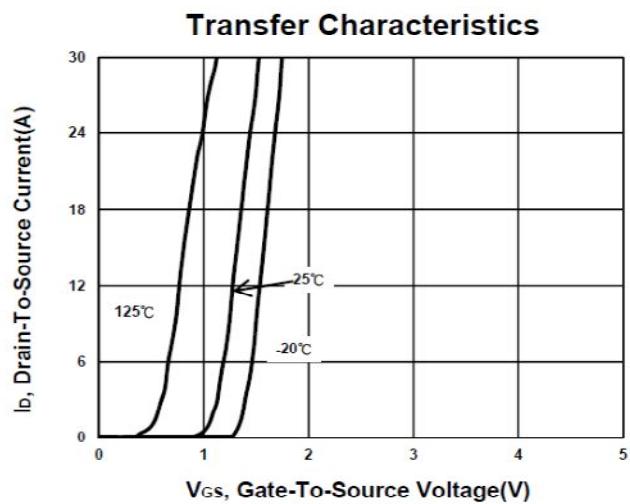
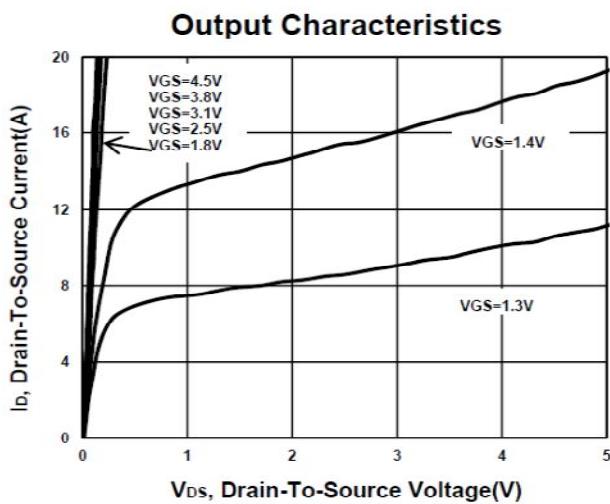
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Package limitation current is 24A.

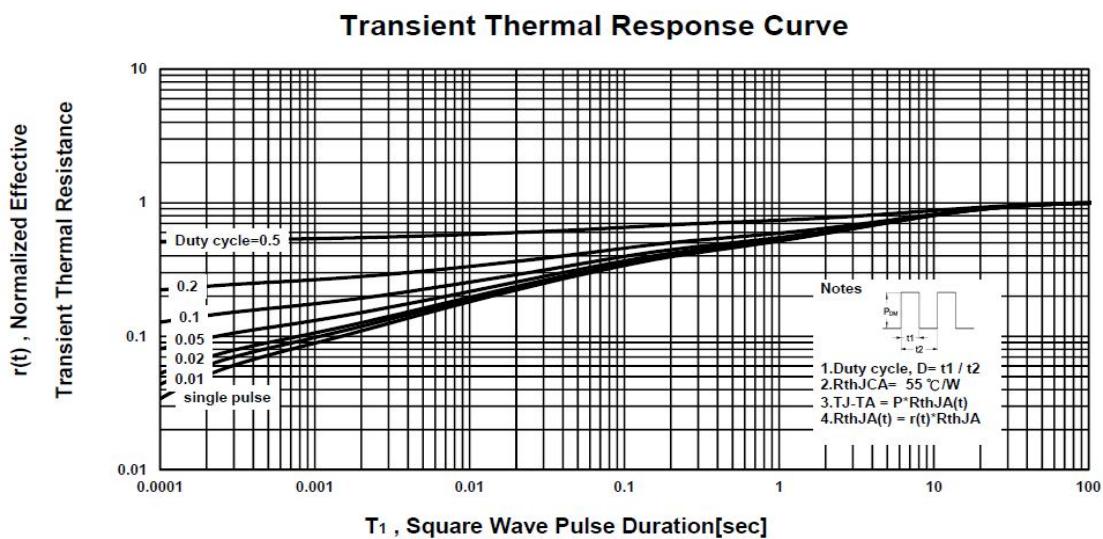
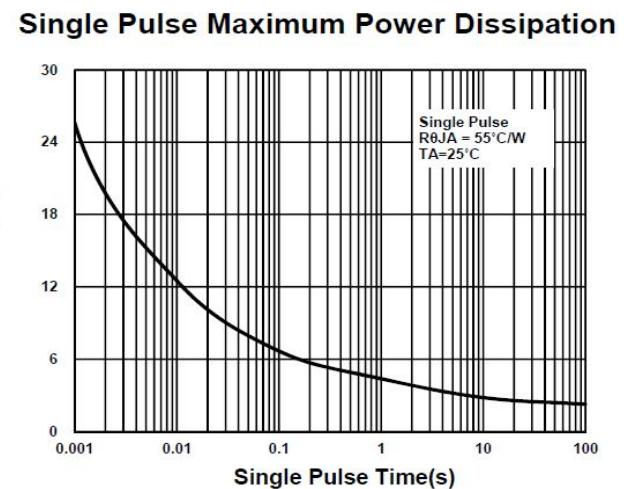
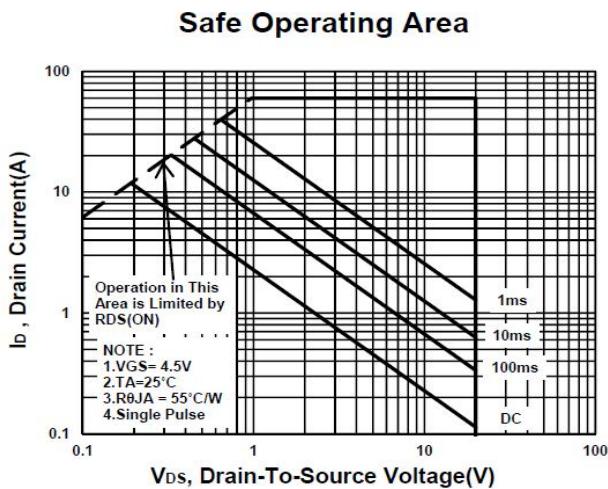
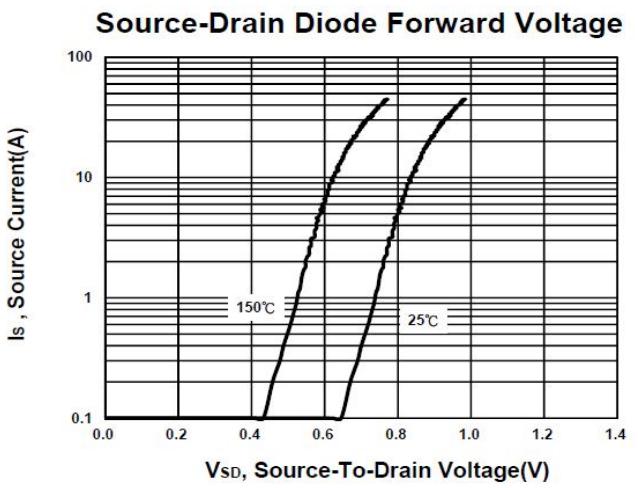
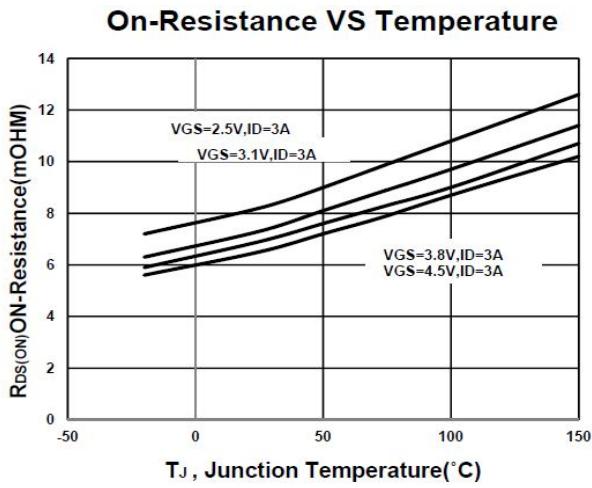
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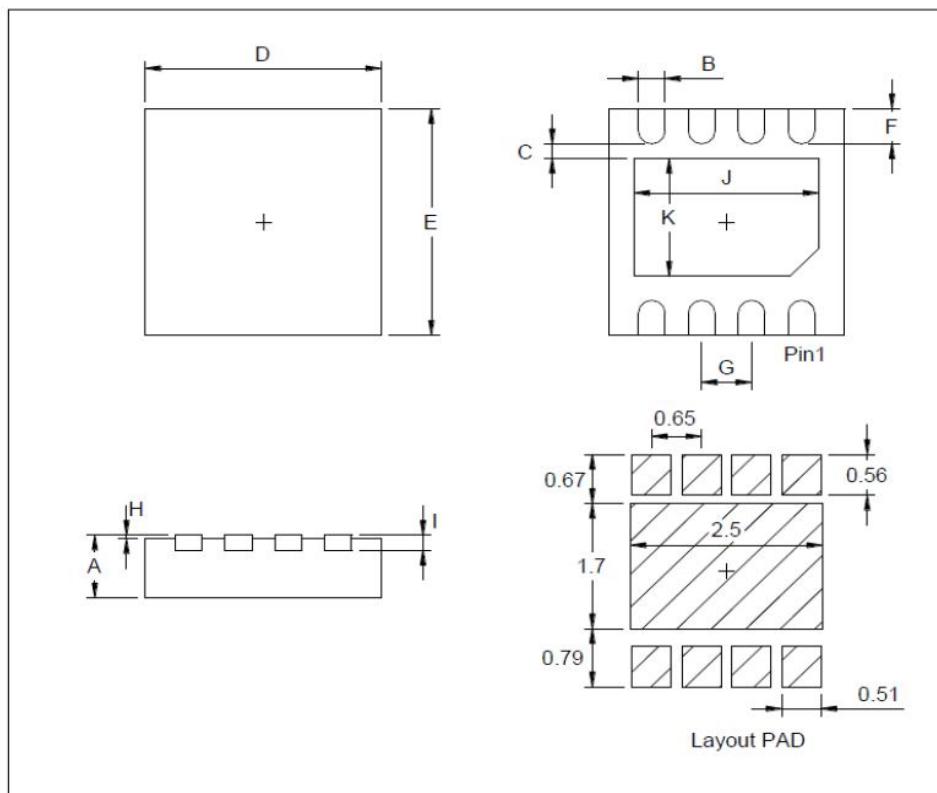
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Dual N-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 3x3S MECHANICAL DATA

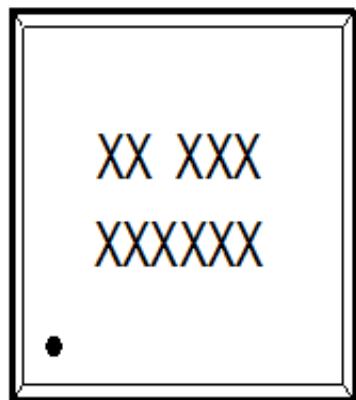
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.70		0.90	I	0.195		0.211
B	0.25		0.35	J	2.20		2.40
C	0.25		0.45	K	1.40		1.60
D	2.90		3.10				
E	2.90		3.10				
F	0.324		0.476				
G	0.55	0.65	0.75				
H	0		0.05				



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Dual N-Channel Enhancement Mode MOSFET

A. Marking Information(此产品代码为: L2)

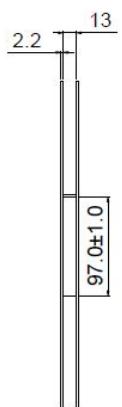
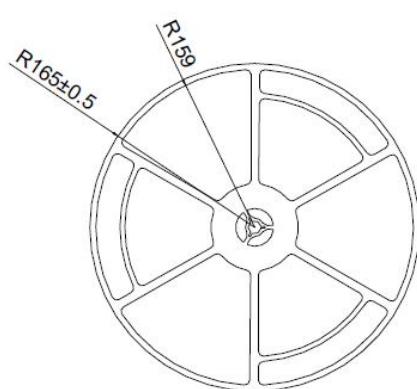
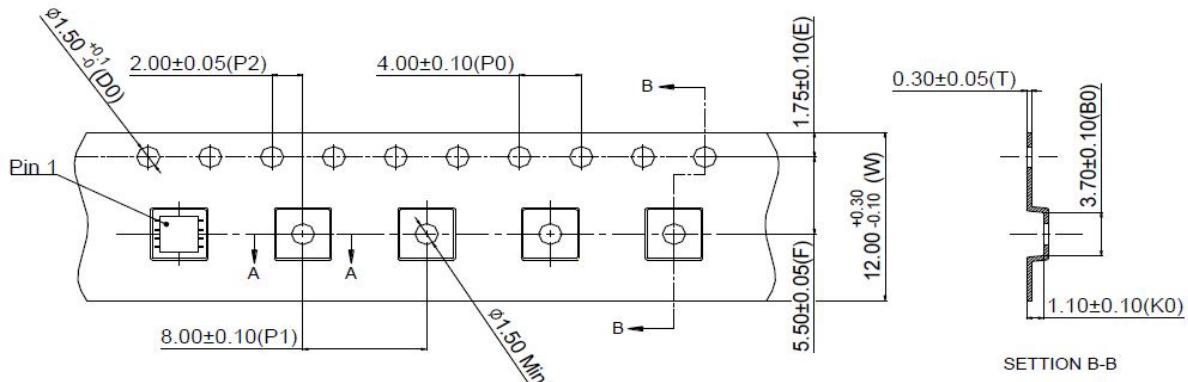


XX(前两码):产品代码

XXX

XXXXXX(后九码):LOT.NO

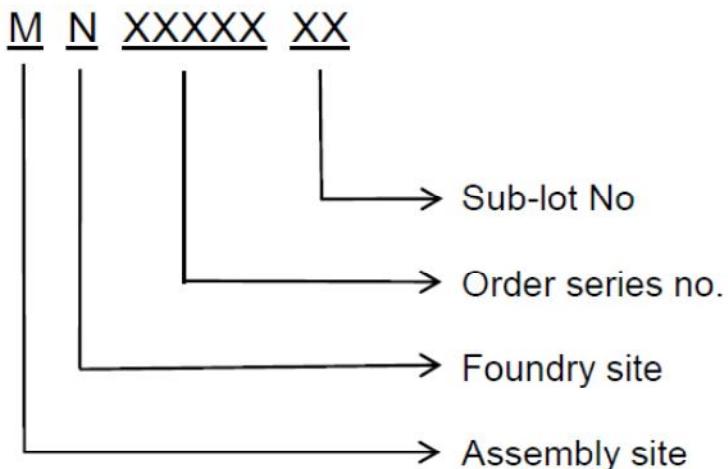
B. Tape&Reel Information:5000pcs/Reel



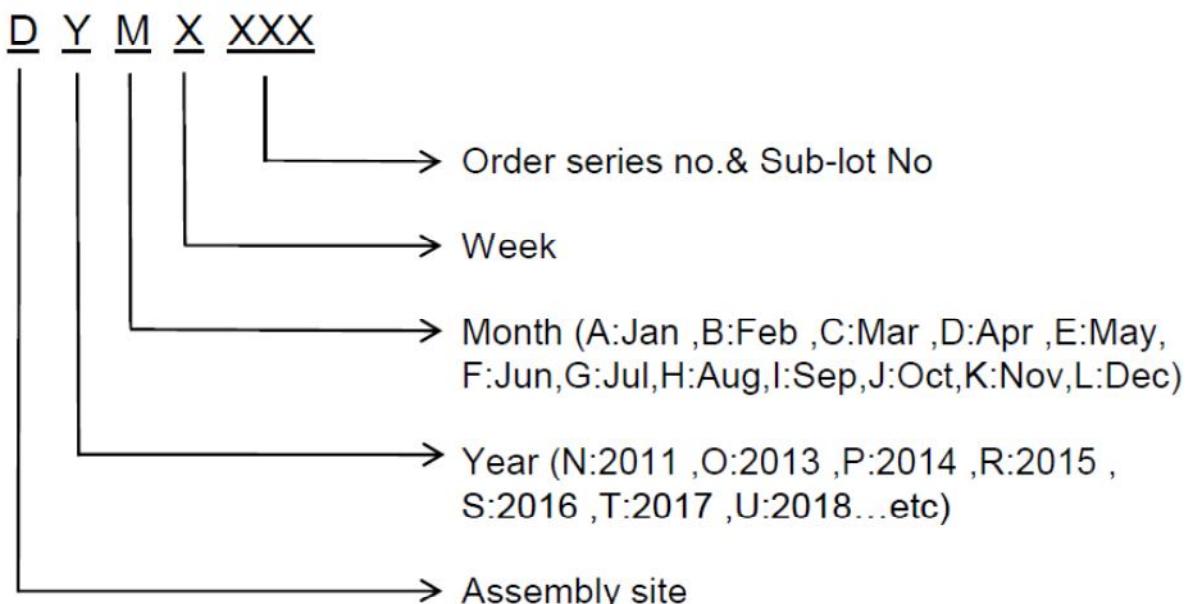
PE544JZ **Dual N-Channel Enhancement Mode MOSFET**

C. Lot No.&Date Code rule

1. Lot No.



2. Date Code



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Dual N-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文“0”和数字“0”，“G”和“Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “/” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least