PE613050

Document category: Product Specification

UltraCMOS® SP4T Tuning Control Switch, 5-3000 MHz



Features

- Open reflective architecture
- Low on-resistance: 1.6Ω
- · Low insertion loss:
 - 0.25 dB @ 900 MHz
 - 0.40 dB @ 2200 MHz
- High power handling:
 - 35.1 dBm @ 900 MHz
 - 35.1 dBm @ 2200 MHz
- Wide power supply range: 2.3–5.5V
- · High ESD tolerance: 2 kV HBM on all pins
- Packaging: 12-lead 2 × 2 × 0.5 mm QFN

Applications

- Tunable antennas
- Tunable matching networks
- · Bypassing applications
- RFID readers

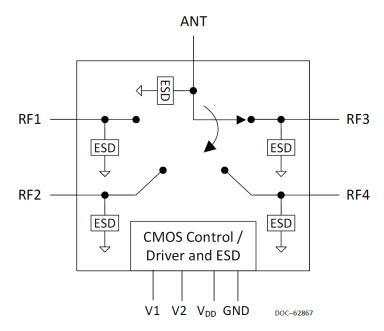


Figure 1. PE613050 functional diagram

Product description

The PE613050 is an SP4T tuning control switch based on pSemi's UltraCMOS® technology. This highly versatile switch supports a wide variety of tuning circuit topologies with emphasis on impedance matching and aperture tuning applications. PE613050 features low on-resistance and insertion loss across key cellular frequency bands from 5–3000 MHz.

The PE613050 offers high RF power handling and ruggedness, while meeting challenging harmonic and linearity requirements enabled by pSemi's HaRP technology. With two-pin low voltage CMOS control, all decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

UltraCMOS tuning devices feature ease of use while delivering superior RF performance. With built-in bias voltage generation and ESD protection, tuning control switches provide a monolithically integrated tuning solution for demanding RF applications.



Absolute maximum ratings



Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions



When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices.

Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE613050 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V _{DD}	-0.3	5.5	V
Digital input voltage, V1 and V2	V _{CTRL}	-0.3	3.6	V
Storage temperature range	T _{ST}	-65	+150	°C
ESD voltage HBM, all pins ^(*)	V _{ESD,HBM}	_	2000	V



 $^{^{\}star}$ Human Body Model (MIL_STD 883 Method 3015.7).



Recommended operating conditions

Table 2 lists the PE613050 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE613050 operating conditions

Parameter	Symbol	Min	Тур	Max	Unit
Supply voltage	V _{DD}	2.30	2.75	5.50	V
Power supply current (VDD = 2.75V, + 25 °C	I _{DD}	_	140	200	μA
Control voltage high	V _{IH}	1.2	1.5	3.1	V
Control voltage low	V _{IL}	0	0	0.5	V
Control input current	-	_	1	10	μA
Peak operating RF voltage: ⁽¹⁾⁽²⁾ - 5–100 MHz ⁽³⁾ - 100 MHz–1 GHz ⁽⁴⁾ - 1 GHz–3 GHz ⁽⁴⁾	_	_	_	10 18 18	V _{PK}
Operating temperature range	T _{OP}	-40	+25	+85	°C



- 1. Between all RF ports, and from the RF ports to GND.
- 2. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
- 3. RF input power of 30.0 dBm, 50Ω .
- 4. RF input power of 35.1 dBm, 50Ω .



Electrical specifications

Table 3 lists the PE613050 key electrical specifications at +25 $^{\circ}$ C and V_{DD} = 2.75V, unless otherwise specified.

Table 3. PE613050 electrical specifications

Parameter	Path	Condition	Min	Тур	Мах	Unit
Operating frequency	_	-	5	_	3000	MHz
R _{ON}	RF-ANT	ON state, DC measurement	_	1.6	-	Ω
C _{OFF}	RF-ANT	Any OFF state	_	0.14	_	pF
Insertion loss ⁽¹⁾	RF-ANT	5–100 MHz 100–698 MHz 698–960 MHz 960–1710 MHz 1710–2170 MHz 2170–2500 MHz 2500–2690 MHz	_	0.17 0.20 0.25 0.35 0.40 0.45 0.50	0.30 0.35 0.45 0.50 0.55 0.60	dB
Isolation ⁽²⁾	RF-ANT	5–100 MHz 100–698 MHz 698–960 MHz 960–1710 MHz 1710–2170 MHz 2170–2500 MHz 2500–2690 MHz 2690–3000 MHz	26 25 21 19 18 17	46 28 27 23 21 20 19	_	dB
Harmonics ⁽³⁾	RF-ANT	2fo: 5–100 MHz; +26 dBm @ TX 3fo: 5–100 MHz; +26 dBm @ TX 2fo: 698–915 MHz; +35 dBm @ TX 3fo: 698–915 MHz; +35 dBm @ TX 2fo: 1710–1910 MHz; +33 dBm @ TX 3fo: 1710–1910 MHz; +33 dBm @ TX 2fo: 698–798 MHz; +26 dBm @ TX 3fo: 698–798 MHz; +26 dBm @ TX 2fo: 2500–2570 MHz; +26 dBm @ TX	_	-58 -87 -62 -55 -58 -55 -80 -82 -70	-36 -36 -36 -36 -36 -36 -36	dBm
Input IP3	_	5–100 MHz 100–3000 MHz	_	80 72	_	dBm
IMD3	-	Bands I ,II, V, VIII, +20 dBm CW @ TX freq, –15 dBm CW @ 2TX–RX freq, 50Ω, SW _{ON}	_	-120	-105	dBm
Switching time	_	50% V _{CTRL} to 90% RF ON or 10% RF OFF	_	2	5	μs
Start-up time ⁽³⁾	_	Time from V _{DD} within specification to all performances within specification	_	_	70	μs



- 1. The tapered transmission lines on the evaluation board provide optimal matching. No additional components on the evaluation board are required to meet the specified performance. For the evaluation board layout, see Figure 3.
- 2. Open reflective architecture for flexible configuration of the switch in a tuning application.
- 3. Pulsed RF input with 4620-µs period, 50% duty cycle, measured per 3GPP TS 45.005.



Equivalent circuit model description

You can use the equivalent circuit model shown in Figure 2 to accurately model the impedance, insertion loss, and isolation of the SP4T tuning switch. It provides a close correlation to measured data and can easily be used in circuit simulation programs.

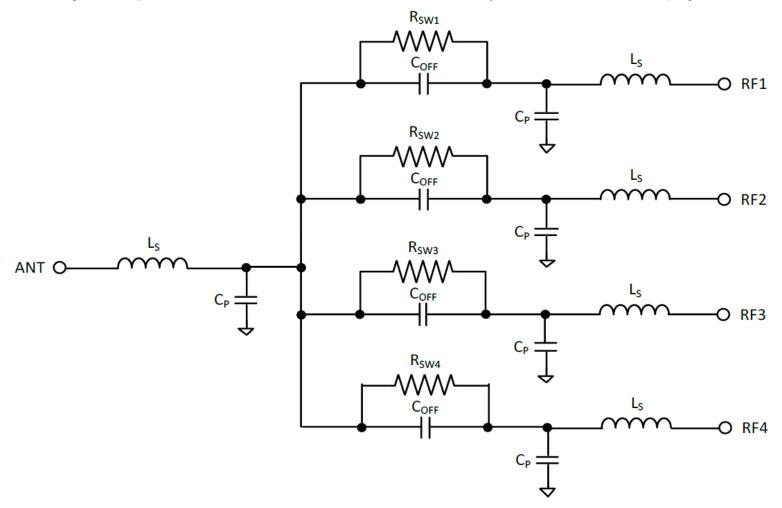


Figure 2. Equivalent circuit model schematic

Table 4 lists the mapping between the preferred switch RF state (RF1-RF4) and the state variables (SW1-SW4).

Table 4. Equivalent circuit model variables

RF st	ate			Vari	able	
Path	V2	V1	SW1	SW2	SW3	SW4
RF1-ANT	0	0	1	0	0	0
RF2-ANT	1	0	0	1	0	0
RF3-ANT	0	1	0	0	1	0
RF4-ANT	1	1	0	0	0	1



You can calculate the equivalent circuit model parameter values using the equations listed in Table 5.

Table 5. Equivalent circuit model parameters

Variable	Equation (SW = 0 for OFF and SW = 1 for ON)	Unit
C _P	0.25	pF
C _{OFF}	0.14	pF
R _{SW1}	If SW ₁ == 1 then 1.6, else 400e3	Ω
R _{SW2}	If SW ₂ == 1 then 1.6, else 400e3	Ω
R _{SW3}	If SW ₃ == 1 then 1.6, else 400e3	Ω
R _{SW4}	If SW ₄ == 1 then 1.6, else 400e3	Ω
L _S	0.4	nH



Evaluation kit

pSemi designed the SP4T switch evaluation board to ease your evaluation of the pSemi PE613050. The RF common port connects through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3, and RF4 connect through 50Ω transmission lines via SMA connectors J3, J5, J2, and J4, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board consists of a 4-layer stack with two outer layers made of Rogers 4350B ($\epsilon r = 3.48$) and two inner layers of FR4 ($\epsilon r = 4.80$). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

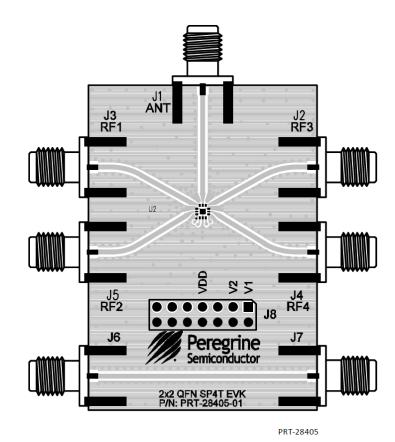


Figure 3. Evaluation board layout



Evaluation board schematic

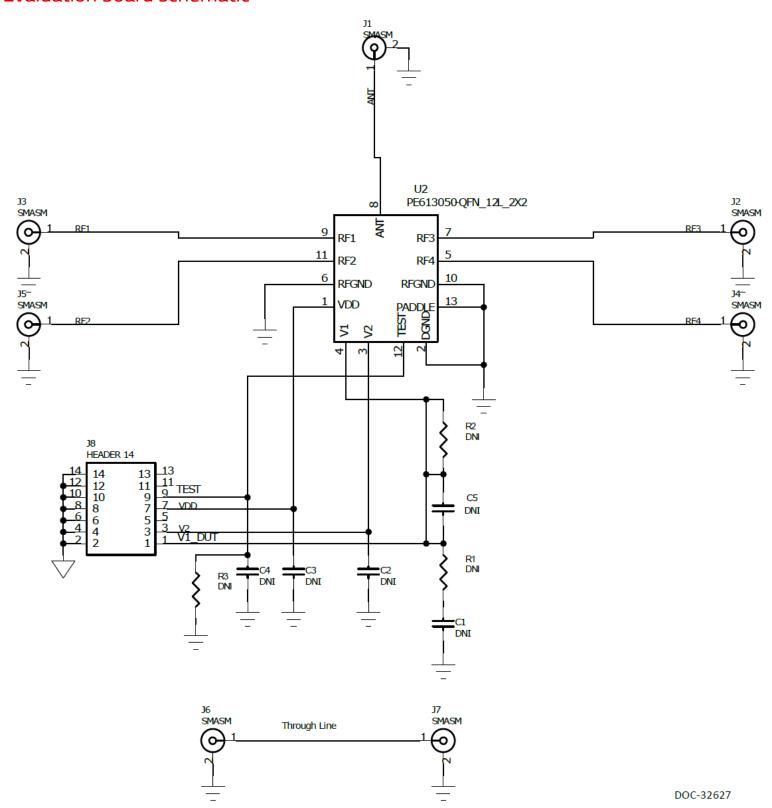


Figure 4. Evaluation board schematic



Pin information

Figure 5 shows the PE613050 pin map for the 12-lead 2 \times 2 \times 0.5 mm QFN package, and Table 6 lists the description for each pin.

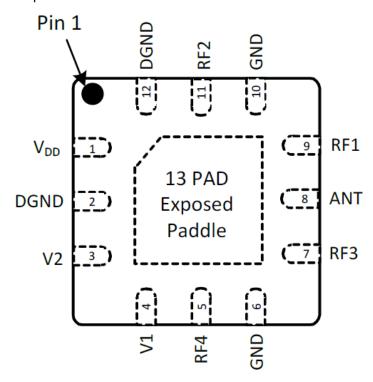


Figure 5. Pin configuration (top view)

Table 6. PE613050 pin descriptions

Pin no.	Pin name	Description
1	V_{DD}	Supply voltage
2, 12 ⁽¹⁾	DGND	Digital ground
3	V2	Switch control input, CMOS logic level
4	V1	Switch control input, CMOS logic level
5	RF4	RF port 4
6, 10 ⁽¹⁾	GND	Ground
7	RF3	RF port 3
8	ANT	RF common - Antenna
9	RF1	RF port 1
11	RF2	RF port 2
13 ⁽²⁾	Pad	Exposed pad.



- 1. Tie all ground pins (2, 6, 10, and 12) together.
- 2. Grounding recommended but can be left floating.



Packaging information

This section provides the following packaging data:

- · Moisture sensitivity level
- · Package drawing

- · Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE613050 moisture sensitivity level rating for the 12-lead 2 × 2 × 0.5 mm QFN package is MSL1.

Package drawing

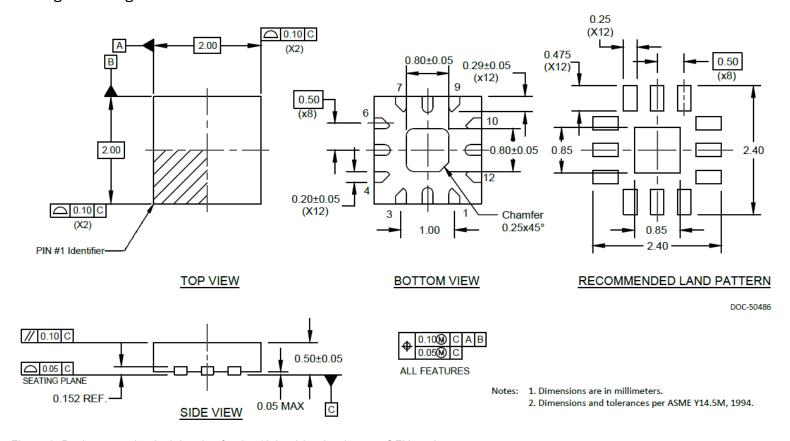


Figure 6. Package mechanical drawing for the 12-lead 2 × 2 × 0.5 mm QFN package



Top-marking specification



Marking Spec Symbol	Package Marking	Definition
PP	DS	Part number code for PE613050
ZZ	00–ZZ	Last two characters of lot code
YY	0–9	Last two digits of year, starting from 2010 (0 for 2010, 1 for 2011, etc.)
ww	01–53	Work week

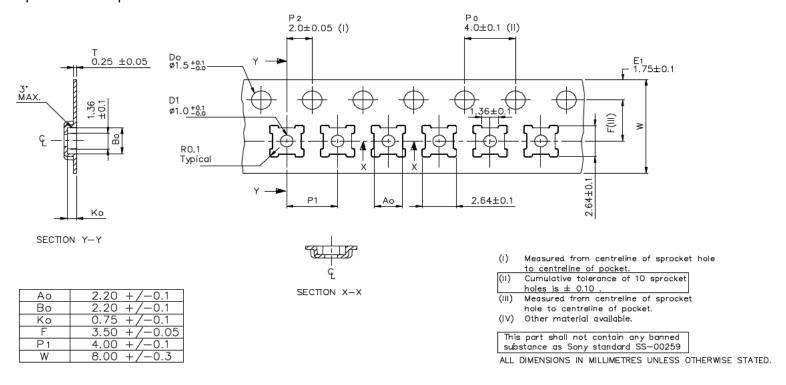
DOC-51207

Note: (PP), the package marking specific to the PE613050, is shown in the figure instead of the standard pSemi package marking symbol (P).

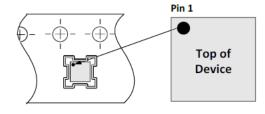
Figure 7. PE613050 package marking specification



Tape and reel specification



----- Tape Feed Direction



Device Orientation in Tape

Figure 8. Tape and reel specification for the 12-lead 2 × 2 × 0.5 mm QFN package



Ordering information

Order code	Description	Packaging	Shipping method
PE613050A-Z	PE613050 SP4T tuning control switch	12-lead 2 × 2 × 0.5 mm QFN	3000 units/T&R
EK613050-01	PE613050 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

Contact and legal information

Sales contact	For additional information, contact Sales at sales@psemi.com.
Disclaimers	The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
Patent statement	pSemi products are protected under one or more of the following U.S. patents: http://patents.psemi.com

Copyright and trademarks

©2013–2025, pSemi Corporation. All rights reserved. The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP, and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.