

**1–7 GHz Low Power UltraCMOS®
Divide-by-2 Prescaler
Radiation Tolerant for Space
Applications**

Features

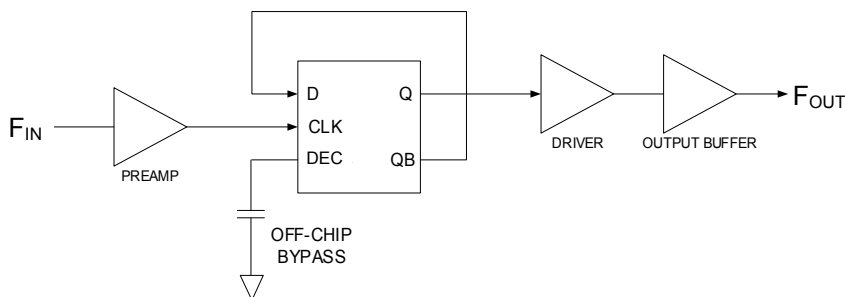
- Fixed divide ratio of 2
- Low-power operation: 13.5 mA typical @ 3V
- Small package: 8-lead CFP
- Guaranteed 100 kRad(Si) total dose performance
- Superior single event upset immunity

Product Description

The PE9304 is a high-performance UltraCMOS® prescaler with a fixed divide ratio of 2. Its operating frequency range is 1000–7000 MHz. The PE9304 operates on a nominal 3V supply and draws only 13.5 mA. It is packaged in a small 8-lead CFP and is ideal for frequency scaling and clock generation solutions.

The PE9304 is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram



**Figure 2. Package Type
8-lead CFP**

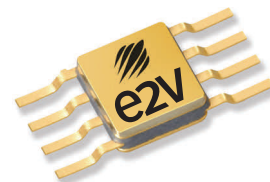


Table 1. Electrical Specifications ($Z_S = Z_L = 50\Omega$) $V_{DD} = 3.0V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise specified

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage		2.85	3.0	3.15	V
Supply current			13.5	18.0	mA
Input frequency, F_{IN}		1		7	GHz
Input sensitivity, P_{IN}	$1000 \text{ MHz} \leq F_{IN} < 2000 \text{ MHz}$	+5		+12	dBm
	$2000 \text{ MHz} \leq F_{IN} < 6000 \text{ MHz}$	0		+12	dBm
	$6000 \text{ MHz} \leq F_{IN} \leq 7000 \text{ MHz}$	+5		+12	dBm
Output power, P_{OUT}	$1000 \text{ MHz} \leq F_{IN} < 2000 \text{ MHz}$	0			dBm
	$2000 \text{ MHz} \leq F_{IN} < 6000 \text{ MHz}$	-7			
	$6000 \text{ MHz} \leq F_{IN} \leq 7000 \text{ MHz}$	-12			

Figure 3. Pin Configuration (Top View)

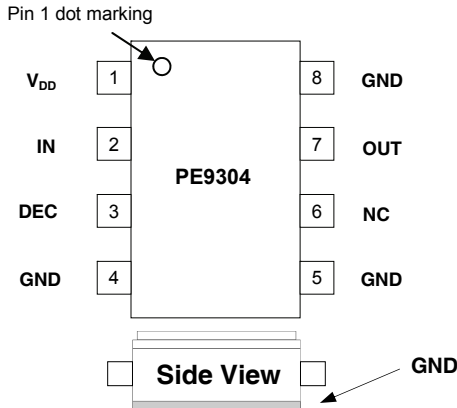


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	V _{DD}	Power supply pin. Bypassing is required (eg 1000 pF & 100 pF).
2	IN	Input signal pin. Should be coupled with a capacitor (eg 2.2 pF).
3	DEC	Decoupling pin. This pin should have two capacitors in parallel (eg 1000 pF, 10 nF).
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No connection. This pin should be left open.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 2.2 pF).
8	GND	Ground pin.
GND	GND	Bottom of the package is ground. Connecting the bottom of the package to ground is required

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Supply voltage		3.3	V
P _{IN}	Input power		+12	dBm
V _{IN}	Voltage on input	-0.3	V _{DD} + 0.3	V
T _{ST}	Storage temperature range	-65	+150	°C
T _{OP}	Operating temperature range	-40	+85	°C
Θ _{JC}	Theta JC		57	°C/W
T _J	Junction temperature maximum		+125	°C
V _{ESD}	ESD voltage, HBM ¹		500	V
	ESD voltage, MM ²		50	V
	ESD voltage, CDM ³		1000	V

Notes: 1. Human Body Model, MIL-STD 883 Method 3015.7
2. Machine Model, JEDEC, JESD22-A114-B
3. Charged Device Model, JEDEC, JESD22-C101

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating ranges maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 3*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements, and therefore do not exhibit enhanced low dose rate sensitivity.

Device Functional Considerations

The PE9304 divides a 1000–7000 MHz input signal by a factor of two thereby producing an output frequency at half the input frequency. To work properly at higher frequencies, the input and output signals (pins 2 and 7) must be AC coupled via an external capacitor, as shown in the test circuit in *Figure 5*.

The ground pattern on the board should be made as wide as possible to minimize ground impedance.

Typical Performance Data @ VDD = 3.0V

Figure 6. Input Sensitivity

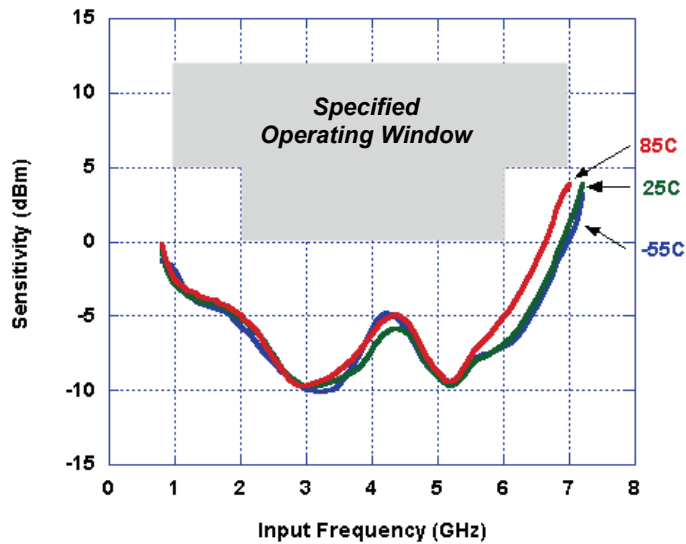


Figure 7. Device Current

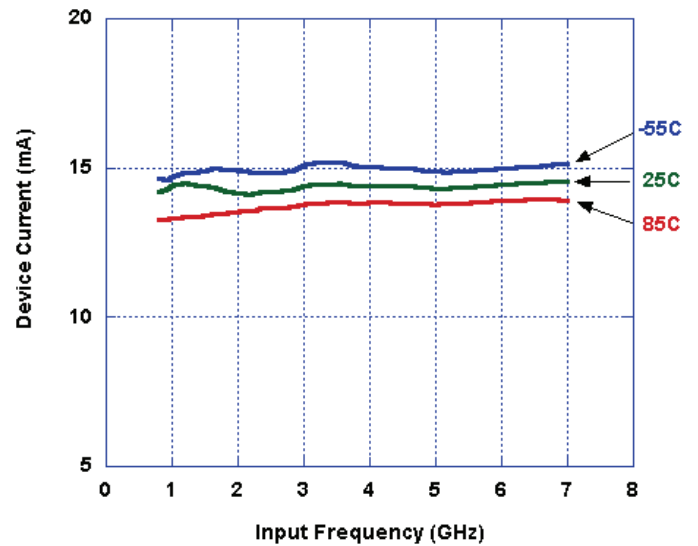


Figure 8. Output Power

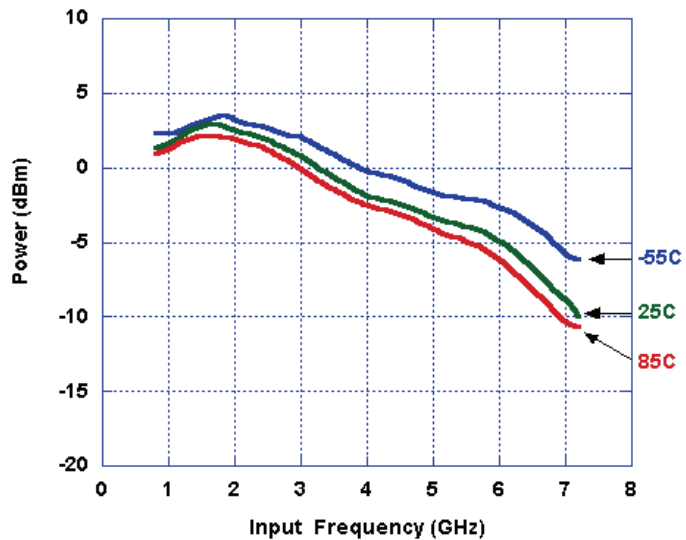
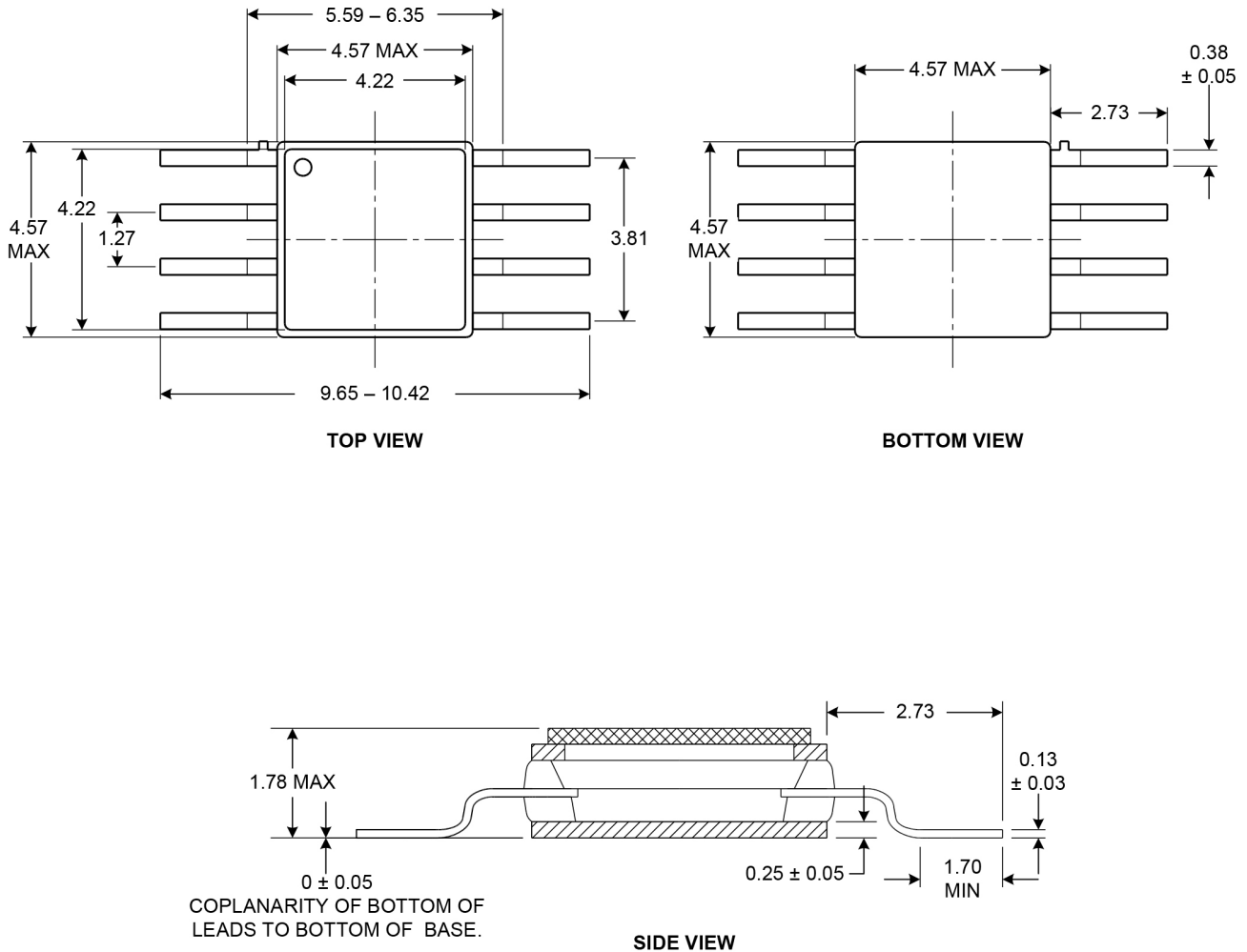


Figure 9. Package Drawing (dimensions are in millimeters)
8-lead CFP

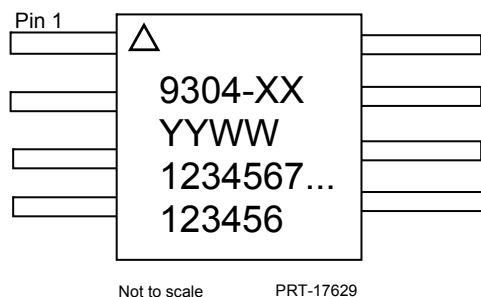
Note: Bottom of the package is ground. Connecting the bottom of the package to ground is required.



DIMS IN MM.
ALL TOLERANCES ARE ± 0.127
UNLESS OTHERWISE STATED.
NOT TO SCALE

Rev. 97 170809
IIGNALB

Figure 10. Top Marking Specifications



Line 1: Pin 1 indicator △ No e2v or Peregrine logos present
Line 2: Part number (XX will be specified by the purchase order)
Line 3: Date code (last two digits of the year and work week)
Line 4: Wafer lot # (as many characters as room allows)
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside symbolization on any of the Peregrine products.

Table 4. Ordering Information

Order Code	Description	Package	Shipping Method
9304-01*	PE9304-08CFPG-1A Engineering samples	8-lead CFP	20 / Tray
9304-11	PE9304-08CFPG-1A Flight units	8-lead CFP	50 / Tray
9304-00	PE9304 Evaluation kit	Evaluation kit	1 / Box

Note: * The PE9304-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE9304-11 flight units. The PE9304-01 device provides the same functionality and footprint as the PE9304-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
e2v ~ <http://www.teledyne-e2v.com> ~ inquiries@e2v-us.com

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