Product Specification

PE9304

1 GHz - 7 GHz Low Power UltraCMOS™ Divide-by-2 Prescaler
Rad-hard for Space Applications

Features

- Fixed divide ratio of 2
- Low-power operation: 13.5 mA typical @ 3 V
- Small package: 8-lead Ceramic SOIC
- Guaranteed 100 Krads(Si) Total Dose Performance
- Superior Single Event Upset Immunity

Product Description

The PE9304 is a high-performance UltraCMOS™ prescaler with a fixed divide ratio of 2. Its operating frequency range is 1000 MHz to 7000 MHz. The PE9304 operates on a nominal 3 V supply and draws only 13.5 mA. It is packaged in a small 8-lead ceramic SOIC and is ideal for frequency scaling and clock generation solutions.

The PE9301 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

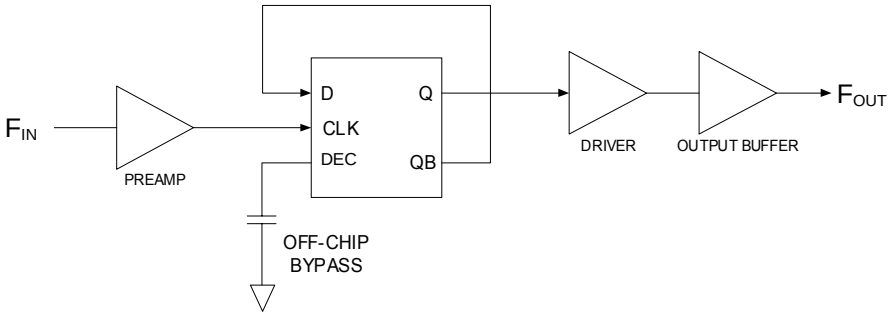


Figure 2. Package Type

8-lead CSOIC

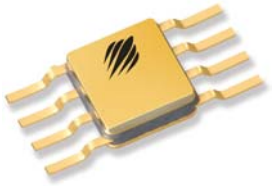


Table 1. Electrical Specifications ($Z_S = Z_L = 50\ \Omega$)

V_{DD} = 3.0 V, -40° C ≤ T_A ≤ 85° C, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			13.5	18.0	mA
Input Frequency (F_{IN})		1		7	GHz
Input Sensitivity (P_{IN})	1000 MHz ≤ F_{IN} < 2000 MHz	+5		+12	dBm
	2000 MHz ≤ F_{IN} < 6000 MHz	0		+12	dBm
	6000 MHz ≤ F_{IN} ≤ 7000 MHz	+5		+12	dBm
Output Power (P_{OUT})	1000 MHz ≤ F_{IN} < 2000 MHz	0			dBm
	2000 MHz ≤ F_{IN} < 6000 MHz	-7			
	6000 MHz ≤ F_{IN} ≤ 7000 MHz	-12			

Figure 3. Pin Configuration

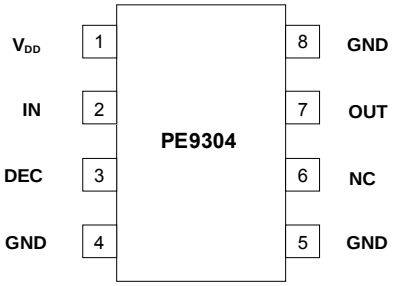


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Power supply pin. Bypassing is required (eg. 1000pF & 100pF).
2	IN	Input signal pin. Should be coupled with a capacitor (eg. 2.2pF).
3	DEC	Decoupling Pin. This pin should have two capacitors in parallel (eg. 1000pf, 10nF)
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No connection. This pin should be left open.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg. 2.2pF).
8	GND	Ground Pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		3.3	V
Pin	Input Power		+12	dBm
V_{IN}	Voltage on input	-0.3	V_{DD} +0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
VESD	ESD voltage (Human Body Model, MIL-STD 883 Method 3015.7)		500	V
	ESD voltage (Machine Model, JEDEC, JESD22-A114-B)		50	V
	ESD voltage (Charged Device Model, JEDEC, JESD22-C101)		1000	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The *PE9304* divides a 1000 MHz – 7000 MHz input signal by a factor of two thereby producing an output frequency at half the input frequency. To work properly at higher frequencies, the input and output signals (pins 2 & 7) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 5.

The ground pattern on the board should be made as wide as possible to minimize ground impedance.

Evaluation Kit Operation

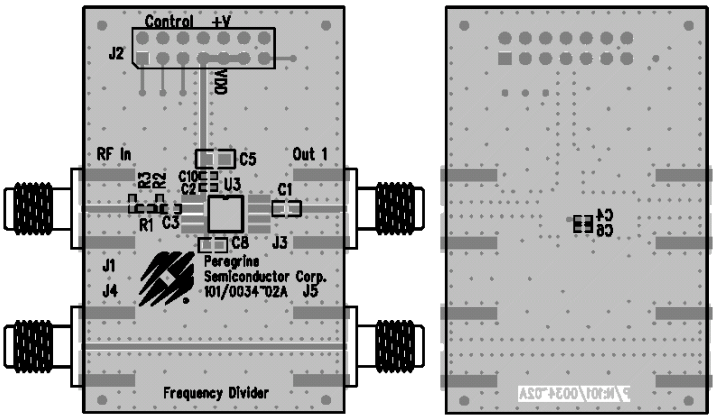
The Ceramic SOIC Prescaler Evaluation Board was designed to help customers evaluate the *PE9304* divide-by-2 prescaler. On this board, the device input (pin 2) is connected to the SMA connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. A value of 2.2 pF was used for the evaluation board; other applications may require a different value.

The device output (pin 7) is connected to SMA connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. This capacitor value must be chosen to have low impedance at the desired output frequency of the device. A value of 2.2 pF was chosen for the evaluation board.

J2 provides DC power to the device via pin 1. Two decoupling capacitors (C2=1000 pF, C10=100 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

The board is constructed using 4 layers. The top and bottom layers are comprised of Rogers low loss 4350 material having a core thickness of 0.010”; while the internal layers are comprised of FR-4. The overall board thickness is 0.062”.

Figure 4. Evaluation Board Layout
Peregrine specification 101/0034

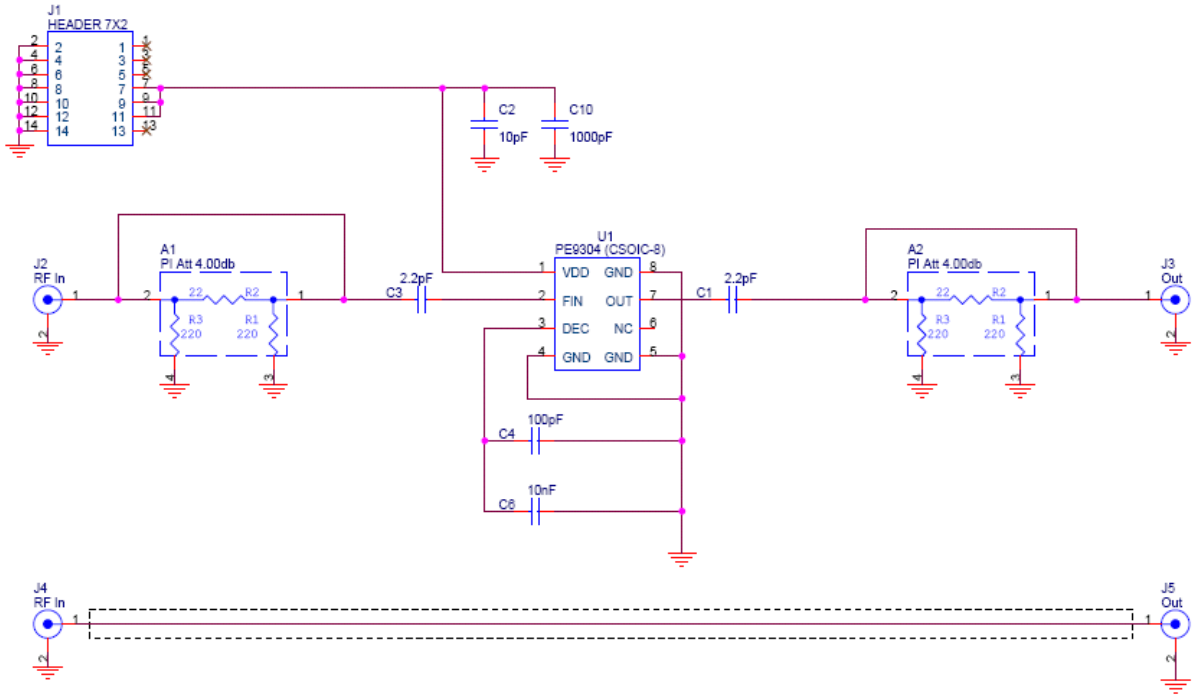


Applications Support

If you have a problem with your evaluation kit or if you have applications questions, please contact applications support:

E-Mail: help@psemi.com (fastest response)
Phone: (858) 731-9400

Figure 5. Evaluation Board Schematic
Peregrine specification 102/0223



Typical Performance Data @ +25 °C

Figure 6. Input Sensitivity

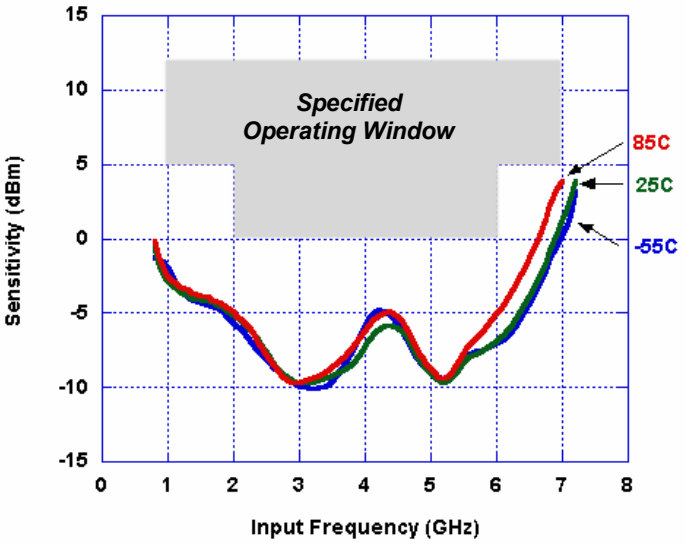


Figure 7. Device Current

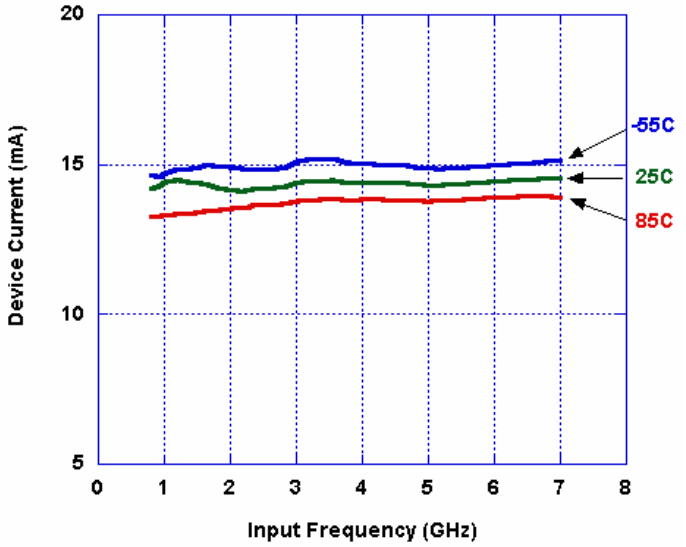


Figure 8. Output Power

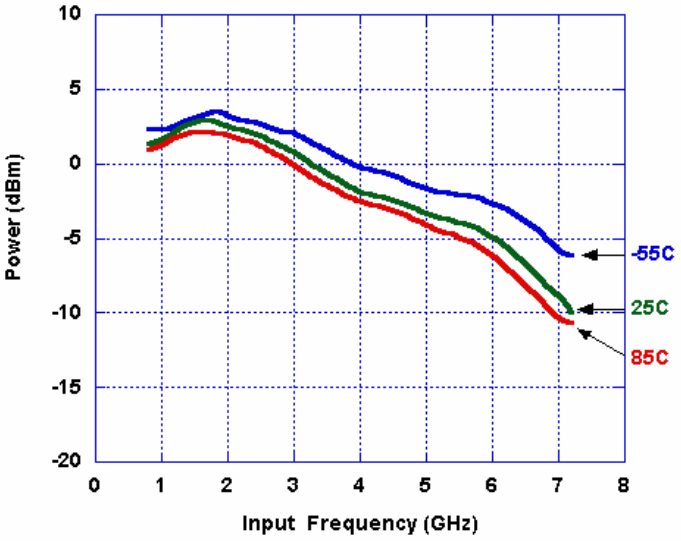


Figure 9. Package Drawing

8-lead CSOIC

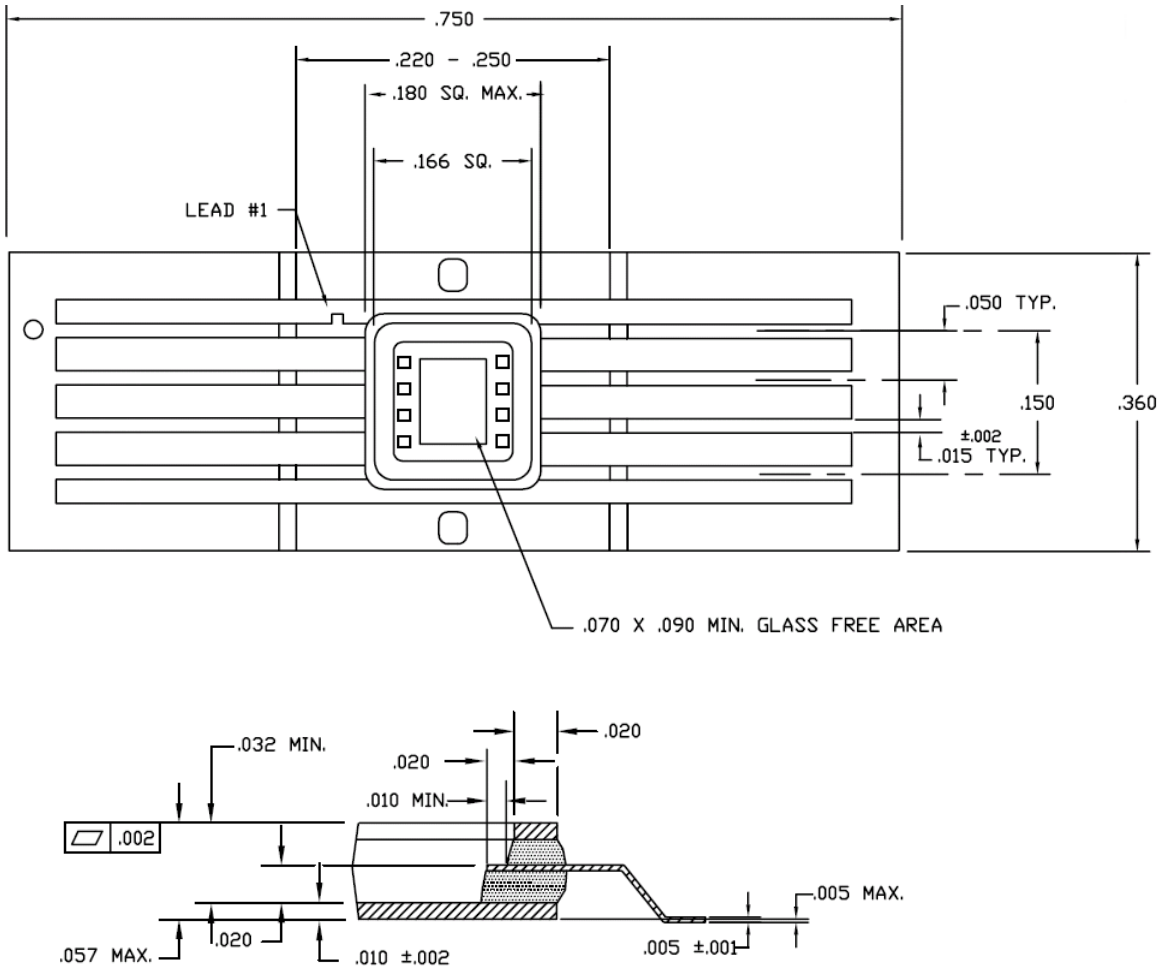


Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
9304-01	PE9304	PE9304-08CFPG-1A Engineering Samples	Gullwing Glass Flatpack	20 / Tray
9304-11	PE9304	PE9304-08CFPG-1A Flight Units	Gullwing Glass Flatpack	50 / Tray
9304-00	PE9304-EK	PE9304 Evaluation Kit	Evaluation Kit	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation
9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:
180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

Peregrine Semiconductor, Korea
#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

South Asia Pacific

Peregrine Semiconductor, China
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.