

PE9312

**1500 MHz Low Power UltraCMOS®
Divide-by-4 Prescaler
Radiation Tolerant for Space
Applications**

Features

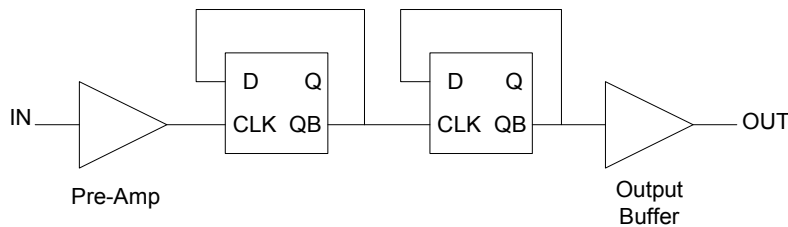
- DC to 1500 MHz operation
- Fixed divide ratio of 4
- Low-power operation: 6.5 mA typical @ 3V
- Small package: 8-lead CFP
- Guaranteed 100 kRad(Si) total dose performance
- Superior single event upset immunity

Product Description

The PE9312 is a high-performance static UltraCMOS® prescaler with a fixed divide ratio of 4. Its operating frequency range is DC to 1500 MHz. The PE9312 operates on a nominal 3V supply and draws only 6.5 mA. It is packaged in a small 8-lead CFP and is ideal for frequency scaling and clock generation solutions.

The PE9312 is manufactured on Peregrine’s UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram



**Figure 2. Package Type
8-lead CFP**



Table 1. Electrical Specifications (Z_S = Z_L = 50Ω) V_{DD} = 3.0V, -40 °C ≤ T_A ≤ +85 °C, unless otherwise specified

Parameter	Condition	Minimum	Typical	Maximum	Unit
Supply voltage		2.85	3.0	3.15	V
Supply current			6.5	11	mA
Input frequency, F _{IN}		DC		1500	MHz
Input power, P _{IN}	DC < F _{IN} ≤ 1000 MHz	-8		+10	dBm
	1000 < F _{IN} ≤ 1500 MHz	0		+10	dBm
Output power, P _{OUT}	DC < F _{IN} ≤ 1500 MHz	0			dBm

Figure 3. Pin Configuration

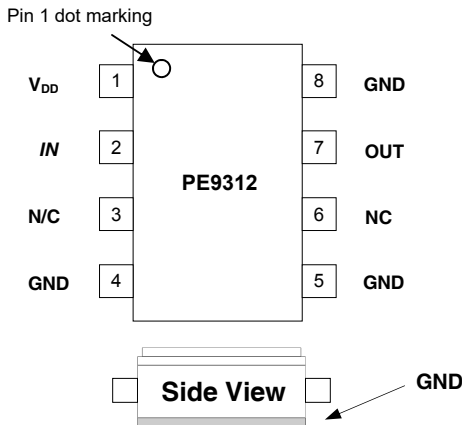


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	V _{DD}	Power supply pin. Bypassing is required (eg 1000 pF & 100 pF).
2	IN	Input signal pin. Should be coupled with a capacitor (eg 1000 pF).
3	NC	No connection. This pin should be left open.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No connection. This pin should be left open.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 1000 pF).
8	GND	Ground pin.
GND	GND	Bottom of the package is ground. Connecting the bottom of the package to ground is required

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Supply voltage		4.0	V
P _{IN}	Input power		15	dBm
V _{IN}	Voltage on input	-0.3	V _{DD} + 0.3	V
T _{ST}	Storage temperature range	-65	+150	°C
T _{OP}	Operating temperature range	-40	+85	°C
Θ _{JC}	Theta JC		57	°C/W
T _J	Maximum junction temperature		+125	°C
V _{ESD}	ESD voltage (Human Body Model, MIL-STD 883)		1000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted

to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Device Functional Considerations

The PE9312 divides an input signal, up to a frequency of 1500 MHz, by a factor of four thereby producing an output frequency at a quarter of the input frequency. To work properly at higher frequency, the input and output signals (pins 2 and 7) must be AC coupled via an external capacitor, as shown in the test circuit in *Figure 7*. The input may be DC coupled for low frequency operation with care taken to remain within the specified DC input range for the device.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See *Figure 8* for a layout example.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements, and therefore do not exhibit enhanced low dose rate sensitivity.

Typical Performance Data @ $V_{DD} = 3.0V$

Figure 4. Input Sensitivity

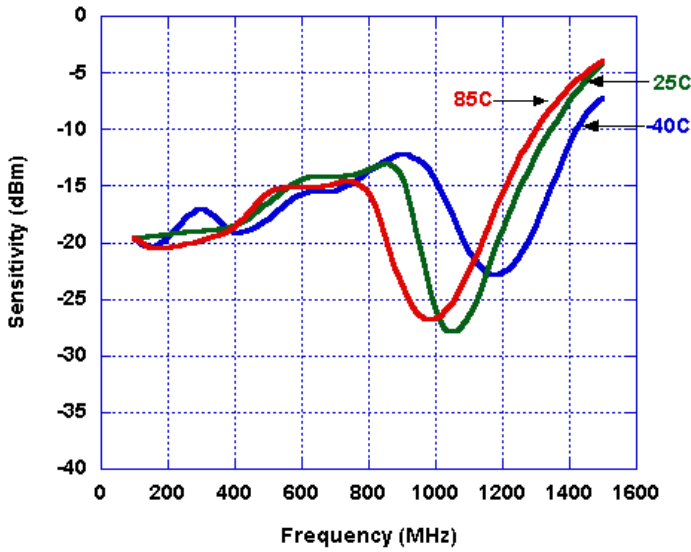


Figure 5. Device Current

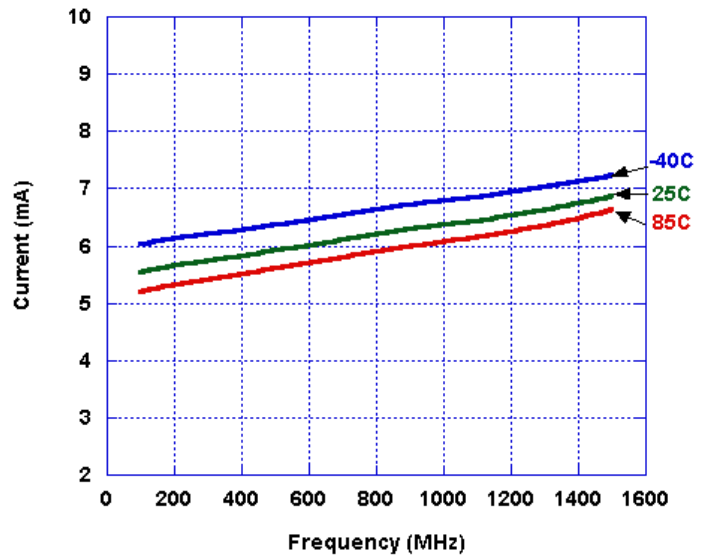


Figure 6. Output Power

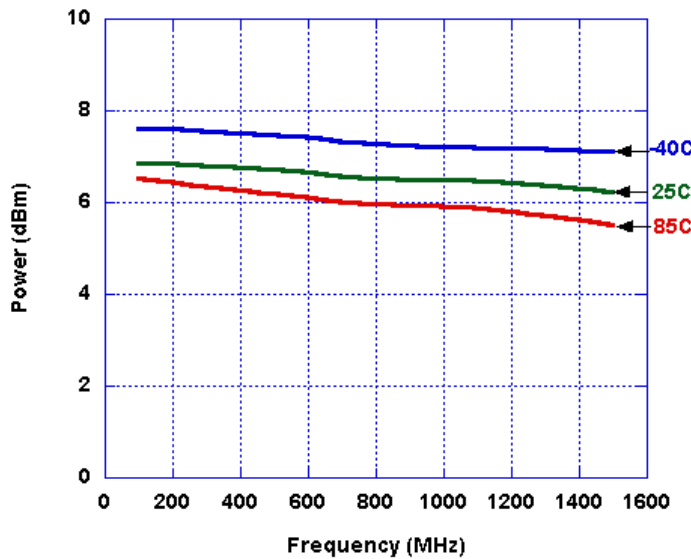


Figure 7. Test Circuit Block Diagram

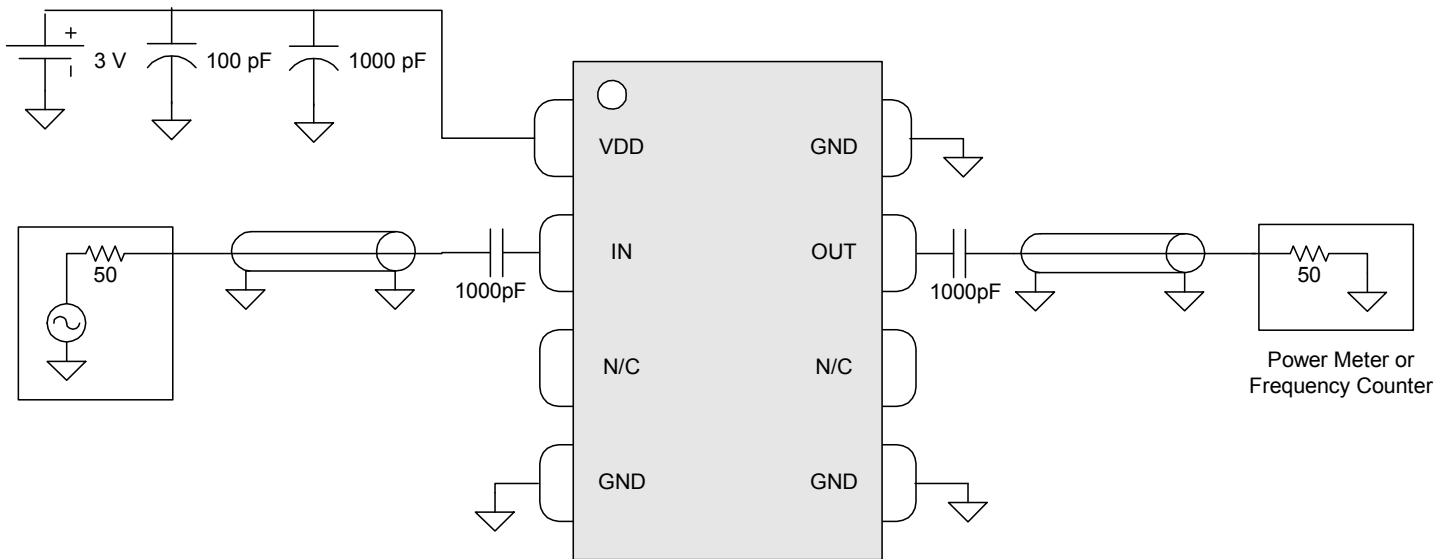
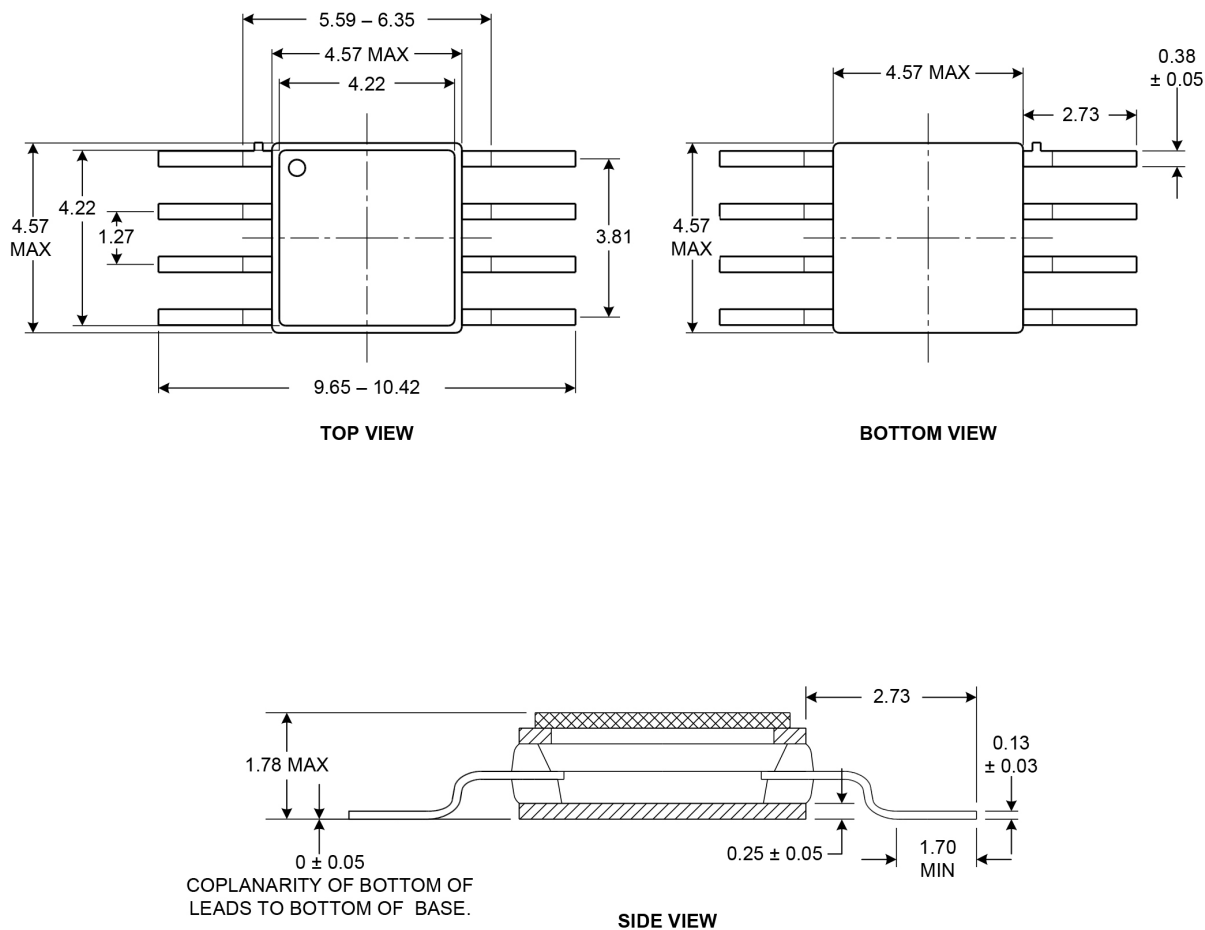


Figure 10. Package Drawing (dimensions are in millimeters)
8-lead CFP

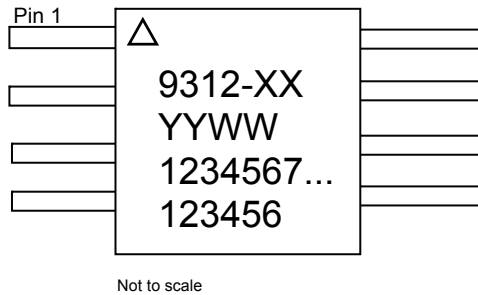
Note: Bottom of the package is ground. Connecting the bottom of the package to ground is required.



DIMS IN MM.
ALL TOLERANCES ARE +/- 0.127
UNLESS OTHERWISE STATED.
NOT TO SCALE

Rev. 97 170809
IIGNALB

Figure 11. Top Marking Specifications



- Line 1: Pin 1 indicator \triangle No e2v or Peregrine logos present
- Line 2: Part number (XX will be specified by the purchase order)
- Line 3: Date code (last two digits of the year and work week)
- Line 4: Waferlot # (as many characters as room allows)
- Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
- Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside symbolization on any of the Peregrine products.

Table 4. Ordering Information

Order Code	Description	Package	Shipping Method
9312-01*	PE9312 Engineering samples	8-lead CFP	50 / Tray
9312-11	PE9312 Flight units	8-lead CFP	50 / Tray
9312-00	PE9312 Evaluation kit	Evaluation kit	1 / Box
8PCFP-MS	8 Pin Mechanical Samples	8 Pin CFP	1/Tray

Note: * The 9312-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE9312-11 flight units. The PE9312-01 device provides the same functionality and footprint as the PE9312-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
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Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.
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