

P-Channel Enhancement Mode Power MOSFET

**DESCRIPTION**

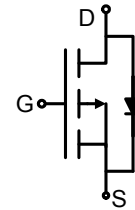
The PE9435 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.

**GENERAL FEATURES**

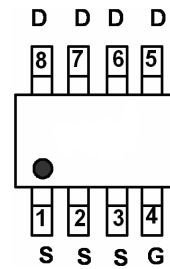
- $V_{DS} = -30V, I_D = -5.1A$   
 $R_{DS(ON)} < 105m\Omega @ V_{GS} = -4.5V$   
 $R_{DS(ON)} < 55m\Omega @ V_{GS} = -10V$
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

**Application**

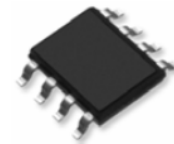
- PWM applications
- Load switch
- Power management



Schematic diagram



Marking and pin Assignment



SOP-8 top view

**Absolute Maximum Ratings (TA=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous	$I_D$	-5.1	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	-20	A
Maximum Power Dissipation	$P_D$	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	°C/W
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**Electrical Characteristics (TA=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-33	-	V

Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.6	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5.1A$	-	48	55	m $\Omega$
		$V_{GS}=-4.5V, I_D=-4.2A$	-	73	105	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-15V, I_D=-4.5A$	4	7	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	1040	-	PF
Output Capacitance	$C_{OSS}$		-	420	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	150	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A,$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	15	-	nS
Turn-on Rise Time	$t_r$		-	13	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	58	-	nS
Turn-Off Fall Time	$t_f$		-	21	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-15V, I_D=-5.1A, V_{GS}=-10V$	-	12	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.2	-	nC
Gate-Drain Charge	$Q_{gd}$		-	3	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=-1.7A$	-	-	-1.2	V

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



Figure 1: Switching Test Circuit

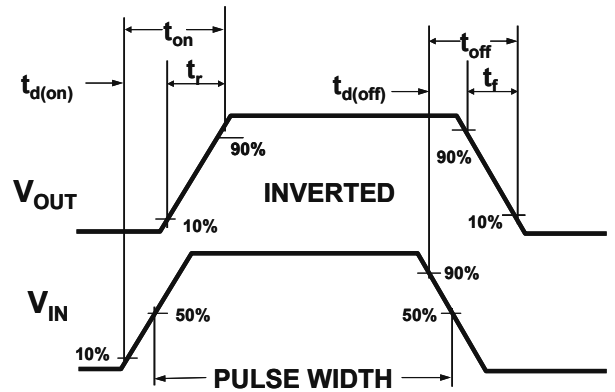


Figure 2: Switching Waveforms

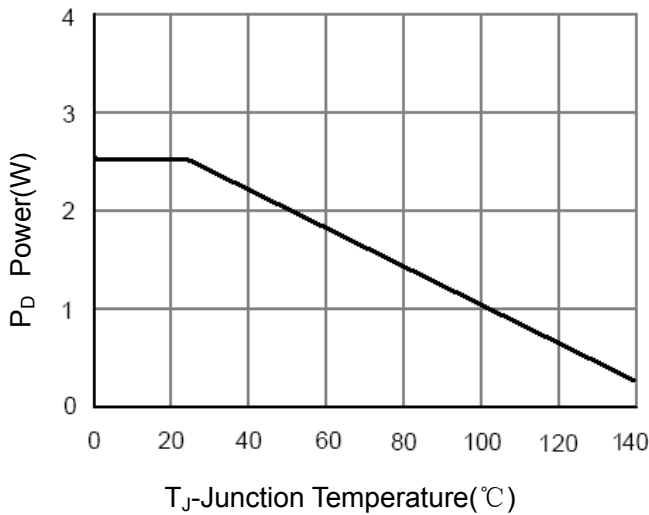


Figure 3 Power Dissipation

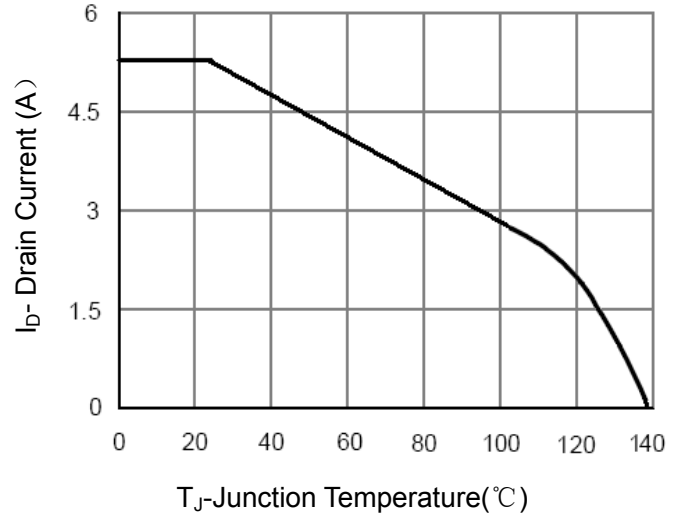


Figure 4 Drain Current

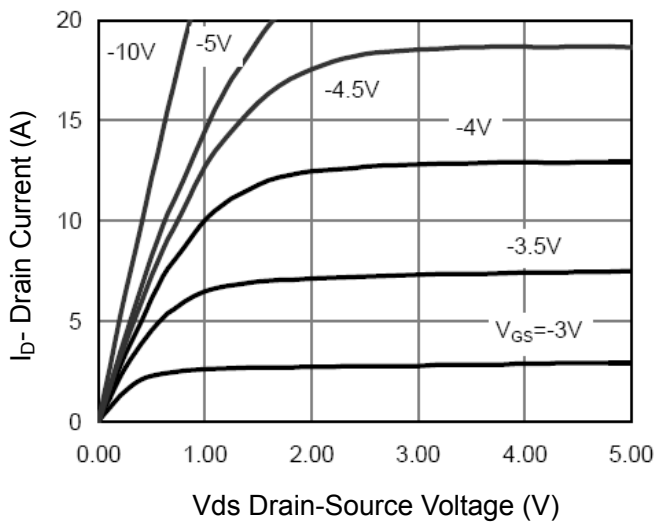


Figure 5 Output CHARACTERISTICS

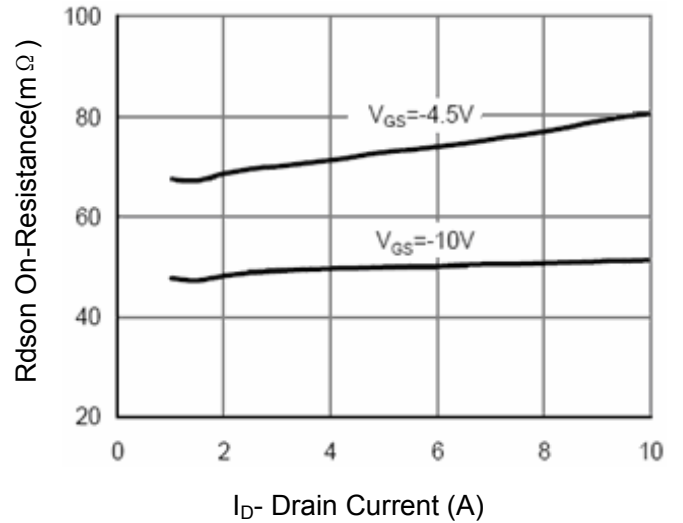


Figure 6 Drain-Source On-Resistance

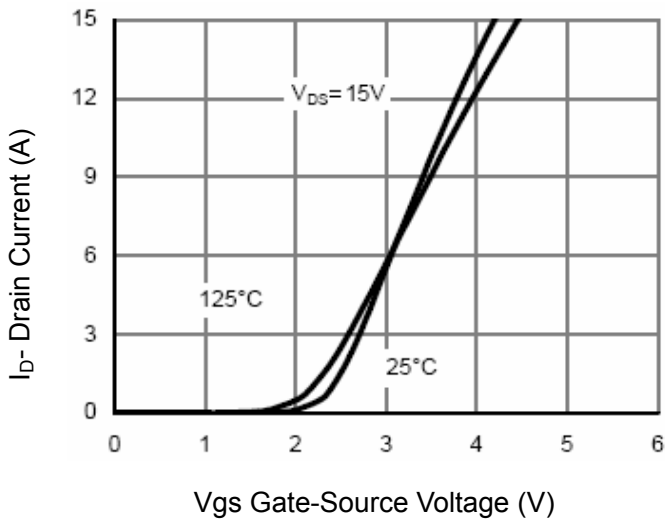


Figure 7 Transfer Characteristics

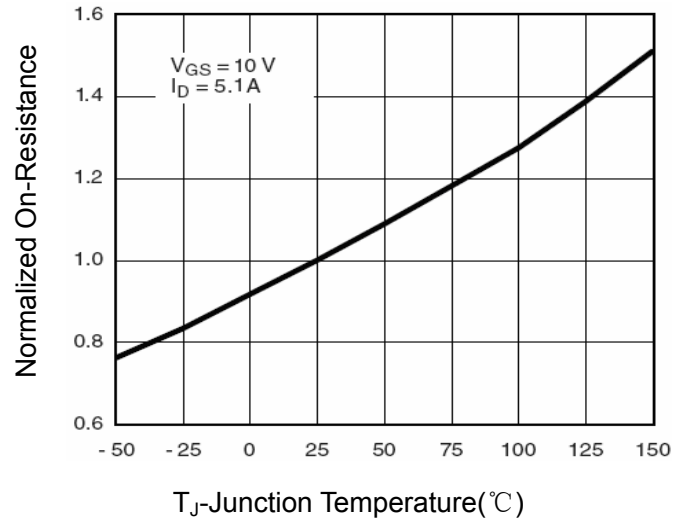


Figure 8 Drain-Source On-Resistance

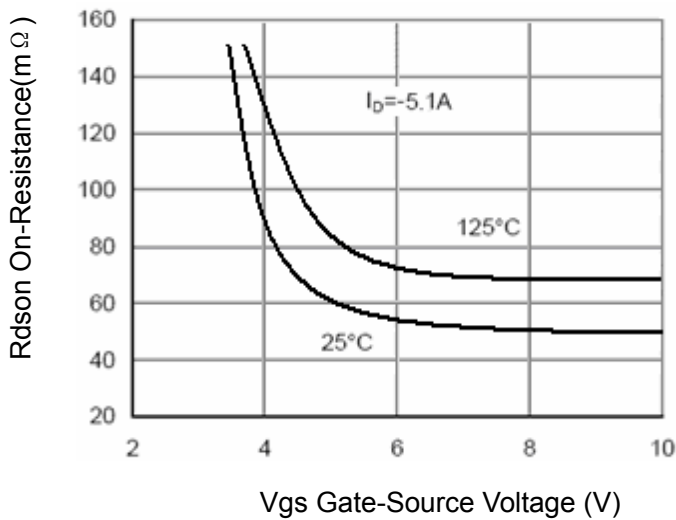


Figure 9 Rdson vs Vgs

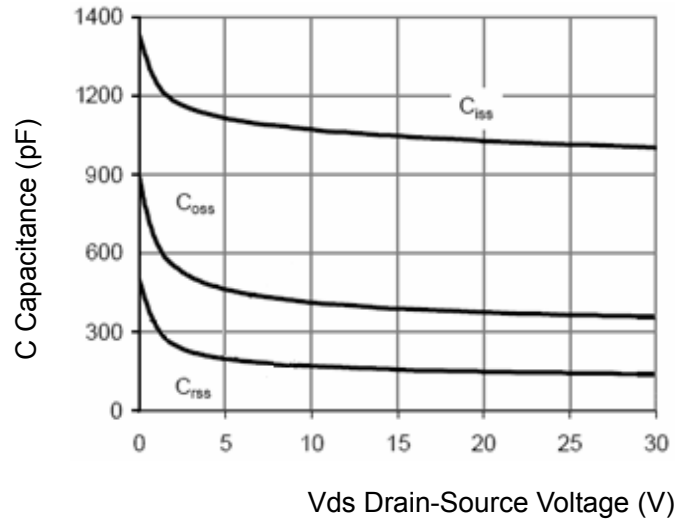


Figure 10 Capacitance vs Vds

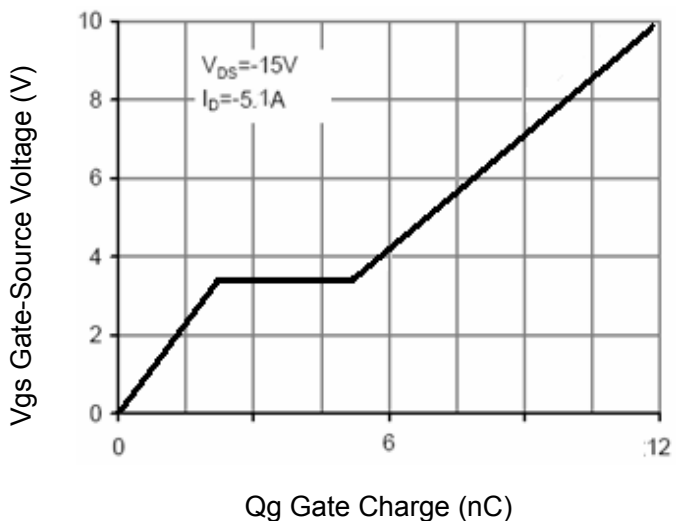


Figure 11 Gate Charge

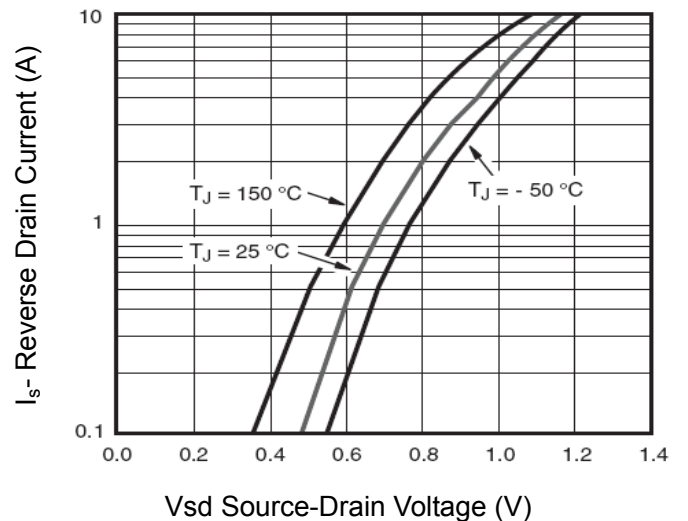


Figure 12 Source- Drain Diode Forward

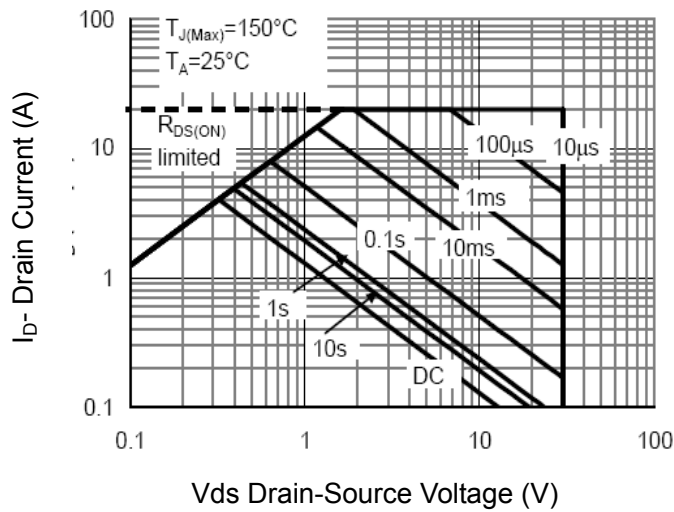


Figure 13 Safe Operation Area

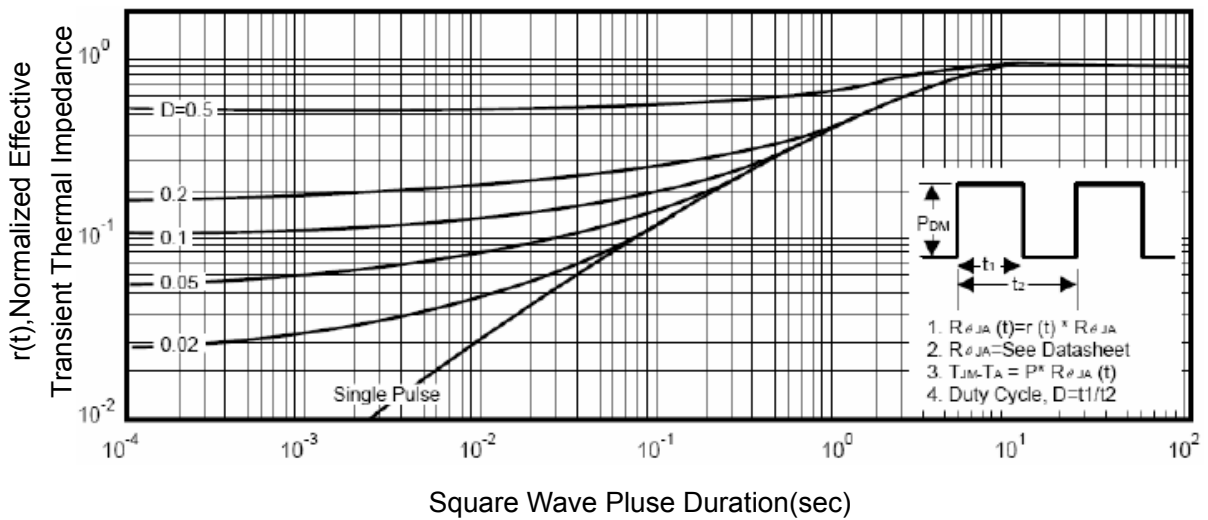
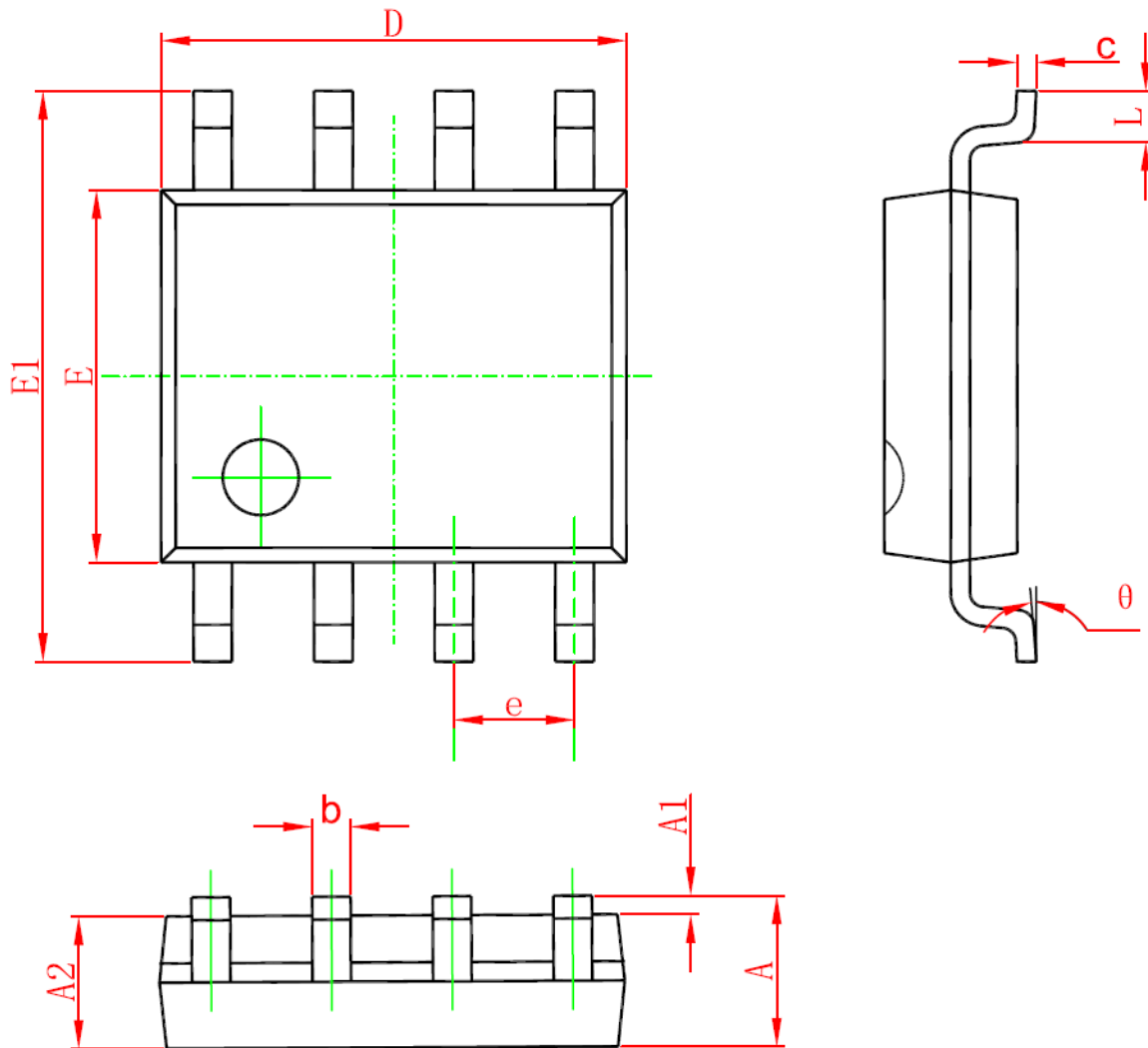


Figure 14 Normalized Maximum Transient Thermal Impedance

### SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°