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Peregrine Semiconductor

Product Specification

PE97632

Radiation Tolerant UltraCMOS® Delta-Sigma Modulated Fractional-N Frequency Synthesizer for Low Phase Noise Applications

Features

- 3.5 GHz operation
- ÷10/11 dual modulus prescaler
- Phase detector output
- Serial or direct hardwired mode
- Frequency selectivity: comparison frequency / 2^{18}
- Low power: 40 mA a@ 3.3V
- Phase noise figure of merit: -216 dBc/Hz
- 100 kRad (Si) total dose
- 68-lead CQFJ
- Pin compatible with the PE9763 *(reference application note AN24 at www.psemi.com)*

Product Description

Peregrine's PE97632 is a radiation tolerant, high performance fractional-N PLL capable of frequency synthesis up to 3.5 GHz. The device is designed for commercial space use and optimized for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLLs.

The PE97632 features a ÷10/11 dual modulus prescaler, counters, a delta sigma modulator and a phase comparator as shown in *Figure 1*. Counter values are programmable through a serial or direct hardwired mode.

The PE97632 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Figure 1. Block Diagram

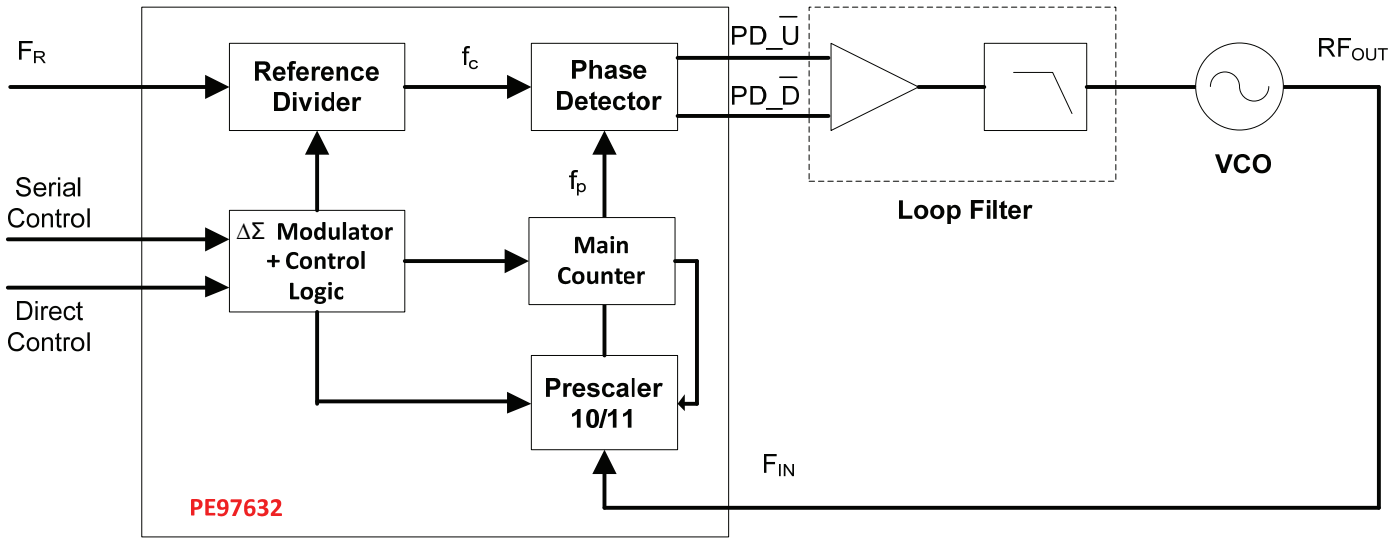


Figure 2. Pin Configuration (Top View)

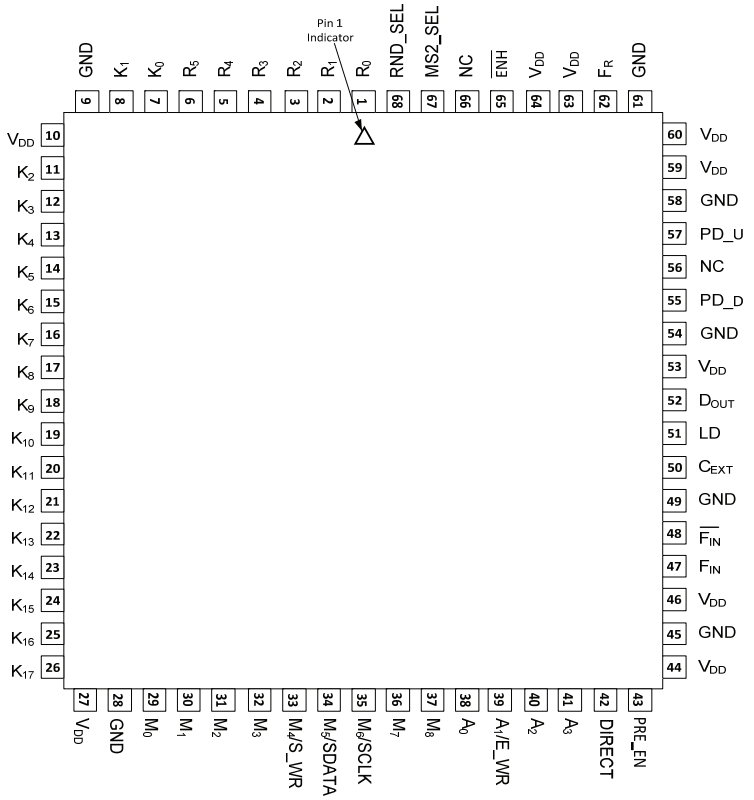


Figure 3. Package Type

68-lead CQFJ

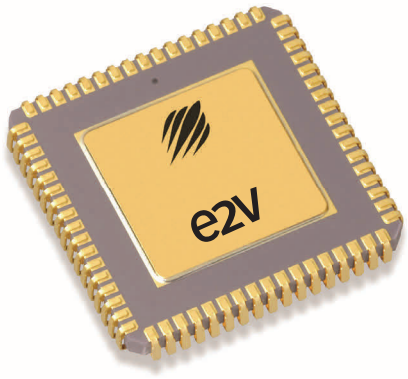


Table 1. Pin Descriptions

Pin #	Pin Name	Valid Mode	Type	Description
1	R_0	Direct	Note 2	R counter bit0 (LSB)
2	R_1	Direct	Note 2	R counter bit1
3	R_2	Direct	Note 2	R counter bit2
4	R_3	Direct	Note 2	R counter bit3
5	R_4	Direct	Note 2	R counter bit4
6	R_5	Direct	Note 2	R counter bit5 (MSB)
7	K_0	Direct	Note 2	K counter bit0 (LSB)
8	K_1	Direct	Note 2	K counter bit1
9	GND		Downbond	Ground
10	V_{DD}		Note 1	Digital core V_{DD}
11	K_2	Direct	Note 2	K counter bit2
12	K_3	Direct	Note 2	K counter bit3
13	K_4	Direct	Note 2	K counter bit4
14	K_5	Direct	Note 2	K counter bit5
15	K_6	Direct	Note 2	K counter bit6

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
16	K_7	Direct	Note 2	K counter bit7
17	K_8	Direct	Note 2	K counter bit8
18	K_9	Direct	Note 2	K counter bit9
19	K_{10}	Direct	Note 2	K counter bit10
20	K_{11}	Direct	Note 2	K counter bit11
21	K_{12}	Direct	Note 2	K counter bit12
22	K_{13}	Direct	Note 2	K counter bit13
23	K_{14}	Direct	Note 2	K counter bit14
24	K_{15}	Direct	Note 2	K counter bit15
25	K_{16}	Direct	Note 2	K counter bit16
26	K_{17}	Direct	Note 2	K counter bit17 (MSB)
27	V_{DD}		Note 1	Digital core V_{DD}
28	GND		Downbond	Ground
29	M_0	Direct	Note 2	M counter bit0 (LSB)
30	M_1	Direct	Note 2	M counter bit1
31	M_2	Direct	Note 2	M counter bit2
32	M_3	Direct	Note 2	M counter bit3
33	M_4	Direct	Note 2	M counter bit4
	S_WR	Serial	Note 2	Serial load enable input. While S_WR is “low”, SDATA can be serially clocked. Primary register data are transferred to the secondary register on S_WR rising edge.
34	M_5	Direct	Note 2	M counter bit5
	SDATA	Serial	Note 2	Binary serial data input. Input data entered MSB first.
35	M_6	Direct	Note 2	M counter bit6
	SCLK	Serial	Note 2	Serial clock input. SDATA is clocked serially into the 21-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
36	M_7	Direct	Note 2	M counter bit7
37	M_8	Direct	Note 2	M counter bit8 (MSB)
38	A_0	Direct	Note 2	A counter bit0 (LSB)
39	A_1	Direct	Note 2	A counter bit1
	E_WR	Serial	Note 2	Enhancement register write enable. While E_WR is “high”, SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
40	A_2	Direct	Note 2	A counter bit2
41	A_3	Direct	Note 2	A counter bit3 (MSB)
42	DIRECT	Both	Note 2	Direct mode select. “High” enables direct mode. “Low” enables serial mode.
43	$\overline{\text{PRE\_EN}}$	Direct	Note 2	Prescaler enable, active “low”. When “high”, F_{IN} bypasses the prescaler.
44	V_{DD}		Note 1	Digital core V_{DD}
45	GND		Downbond	Ground

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
46	V_{DD}		Note 1	Prescaler V_{DD}
47	F_{IN}	Both	Input	Prescaler input from the VCO, 3.5 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and terminated with a 50Ω resistor to ground.
48	$\overline{F_{IN}}$	Both	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground.
49	GND		Downbond	Ground
50	C_{EXT}	Both	Output	Logical “NAND” of PD_$\overline{U}$ and PD_$\overline{D}$ terminated through an on chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Both	Output	Lock detect and open drain logical inversion of C_{EXT}. When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).
52	D_{OUT}	Both	Output	Data out function, enabled in enhancement mode.
53	V_{DD}		Note 1	Output driver/V_{DD}
54	GND		Downbond	Ground
55	PD_$\overline{D}$	Both	Output	PD_$\overline{D}$ pulses down when f_p leads f_c.
56	NC	Both	Note 3	No connect
57	PD_$\overline{U}$	Both	Output	PD_$\overline{U}$ pulses down when f_c leads f_p.
58	GND		Downbond	Ground
59	V_{DD}		Note 1	Output driver/V_{DD}
60	V_{DD}		Note 1	Phase detector V_{DD}
61	GND		Downbond	Ground
62	F_R	Both	Input	Reference frequency input
63	V_{DD}		Note 1	Reference V_{DD}
64	V_{DD}		Note 1	Digital core V_{DD}
	GND		Downbond	Ground
65	$\overline{ENH}$	Both	Note 2	Enhancement mode. When asserted low (“0”), enhancement register bits are functional.
66	NC	Both	Note 3	No connect
67	MS2_SEL	Both	Note 2	MASH 1-1 select. “High” selects MASH 1-1 mode. “Low” selects the MASH 1-1-1 mode.
68	RND_SEL	Both	Note 2	K register LSB toggle enable. “1” enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the phase detector comparison frequency / 2^{19}.

Notes: 1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-down resistors to ground.
3. No Connect pins can be left open or floating.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	–0.3	4.0	V
V_I	Voltage on any input	–0.3	V_{DD} + 0.3	V
I_I	DC into any input	–10	+10	mA
I_O	DC into any output	–10	+10	mA
θ_{JC}	Theta JC		12	°C/W
T_j	Junction temperature maximum		+125	°C
T_{stg}	Storage temperature range	–65	+150	°C
V_{ESD}	ESD voltage HBM[1] All pins except pin 52		1000	V
	ESD voltage HBM[1,2] On pin 52		300	V

Notes: 1. Human Body Model (MIL-STD-883 Method 3015).
2. Pin 52 is a test pin only. It is not used in normal operation.

Table 3. Operating Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.85	3.45	V
T_A	Operating ambient temperature range	–40	+85	°C

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating ranges maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 3*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements and therefore do not exhibit enhanced low dose rate sensitivity.

Table 4. Single Event Effects[1]

SEE Mode	Effective Linear Energy Transfer (LET)[2]
SEL	90 MeV•cm^2/mg [3]
SEB, SEGR, SEFI	90 MeV•cm^2/mg [3]
SEU	60 MeV•cm^2/mg [4]
SET	60 MeV•cm^2/mg [5]

Notes: 1. Testing performed using serial programming mode.
2. Au ion/60° incidence.
3. No SEL, SEB, SEGR, SEFI observed.
4. No frequency upsets observed at LET<60.
5. Minor transients (phase errors) observed resulting in self-recovering operation without intervention.

Table 5. DC Characteristics @ V_{DD} = 3.3V –40°C < T_A < +85 °C, unless otherwise specified

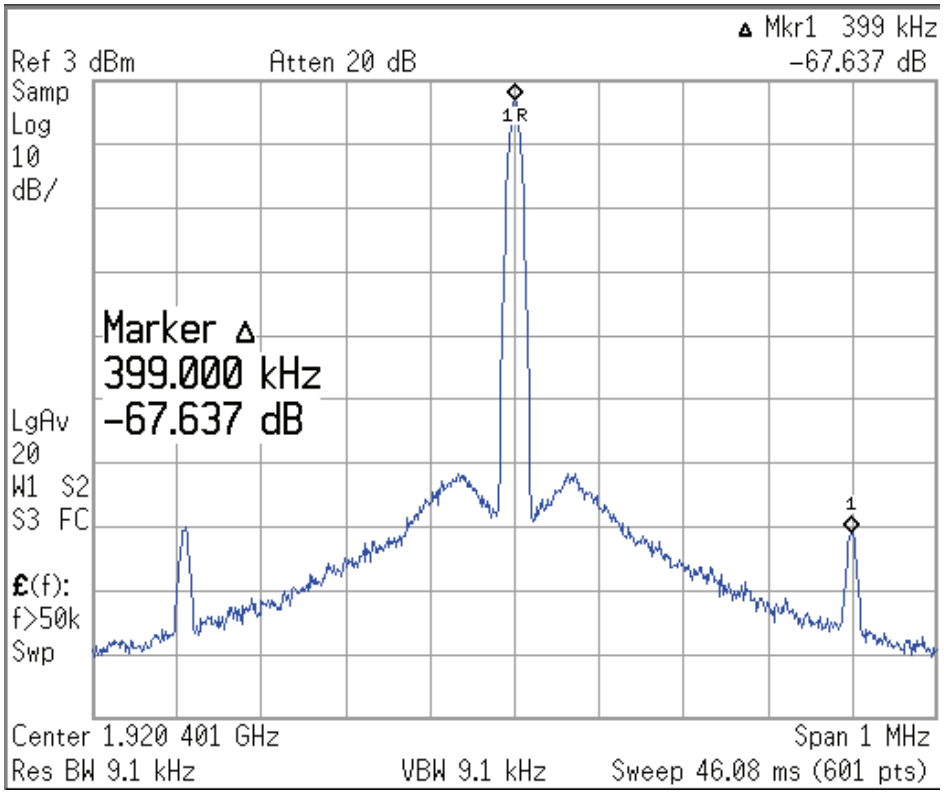
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Operational supply current;	Prescaler enabled V_{DD} = 2.85–3.45V		40	50	mA
		Prescaler disabled V_{DD} = 2.85–3.45V		15	20	mA
All digital inputs: K[17:0], R[5:0], M[8:0], A[3:0], DIRECT, $\overline{PRE\_EN}$, RND_SEL, MS2_SEL, $\overline{ENH}$ (have a 70 kΩ pull-down resistor)						
V_{IH}	High level input voltage	V_{DD} = 2.85–3.45V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85–3.45V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.45V			100	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.45V	–1			µA
Reference divider input: F_R						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.45V			100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.45V	–100			µA
Counter and phase detector outputs: PD_$\overline{D}$, PD_$\overline{U}$						
V_{OLD}	Output voltage LOW	I_{OUT} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{OUT} = –3 mA	V_{DD} – 0.4			V
Digital test outputs: D_{OUT}						
V_{OLD}	Output voltage LOW	I_{OUT} = 200 µA			0.4	V
V_{OHD}	Output voltage HIGH	I_{OUT} = –200 µA	V_{DD} – 0.4			V
Lock detect outputs: (C_{EXT}, LD)						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{OUT} = 0.1 mA			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{OUT} = –0.1 mA	V_{DD} – 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{OUT} = 1 mA			0.4	V

Table 6. AC Characteristics @ V_{DD} = 3.3V, –40°C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see *Figure 10*)						
f_{Clk}	Serial data clock frequency[1]				10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	SDATA set-up time to SCLK rising edge		10			ns
t_{DHLD}	SDATA hold time after SCLK rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	SCLK rising edge to S_WR rising edge		30			ns
t_{CE}	SCLK falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to SCLK rising edge		30			ns
t_{EC}	E_WR transition to SCLK rising edge		30			ns
Main divider (prescaler enabled)						
P_{Fin}	Input level range	External AC coupling 275 MHz ≤ Freq ≤ 3200 MHz	–5		5	dBm
		External AC coupling 3.2 GHz < Freq ≤ 3.5 GHz 3.15 V ≤ V_{DD} ≤ 3.45 V	0		5	dBm
Main divider (prescaler bypassed)						
F_{IN}	Operating frequency		50		300	MHz
P_{Fin}	Input level range	External AC coupling	–5		5	dBm
Reference divider						
F_R	Operating frequency[3]				100	MHz
P_{FR}	Reference input power[2]	Single ended input	–2		10	dBm
Phase detector						
f_c	Comparison frequency[3]				50	MHz
SSB phase noise (F_{IN} = 1.9 GHz, F_R = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.3V)						
Φ_N	Phase noise	100 Hz offset		–89	–83	dBc/Hz
Φ_N	Phase noise	1 kHz offset		–96	–91	dBc/Hz
Φ_N	Phase noise	10 kHz offset		–101	–96	dBc/Hz
SSB phase noise (F_{IN} = 1.9 GHz, F_R = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.0V)						
Φ_N	Phase noise	100 Hz offset		–84	–70	dBc/Hz
Φ_N	Phase noise	1 kHz offset		–92	–81	dBc/Hz
Φ_N	Phase noise	10 kHz offset		–100	–89	dBc/Hz

Notes: 1. f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{Clk} specification.
2. CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of the PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled. For Sin wave inputs, the minimum amplitude needs to be 0.5 V_{PP}. The maximum level should be limited to prevent ESD diodes at the pin input from turning on. Diodes will turn on at one forward-bias diode drop above V_{DD} or below GND. The DC voltage at the Reference input is V_{DD}/2.
3. Parameter is guaranteed through characterization only and is not tested.

Figure 4. Typical Spurious Plot



Test conditions: MASH 1-1 mode. F_{OUT} = 1.9204 GHz, $f_{COMPARISON}$ = 20 MHz, frequency step = 400 KHz, V_{DD} = 3.3V, temp = 25 °C , loop bandwidth = 50 kHz

Figure 5. RF Sensitivity vs Frequency (typical device at temperature = +25 °C)

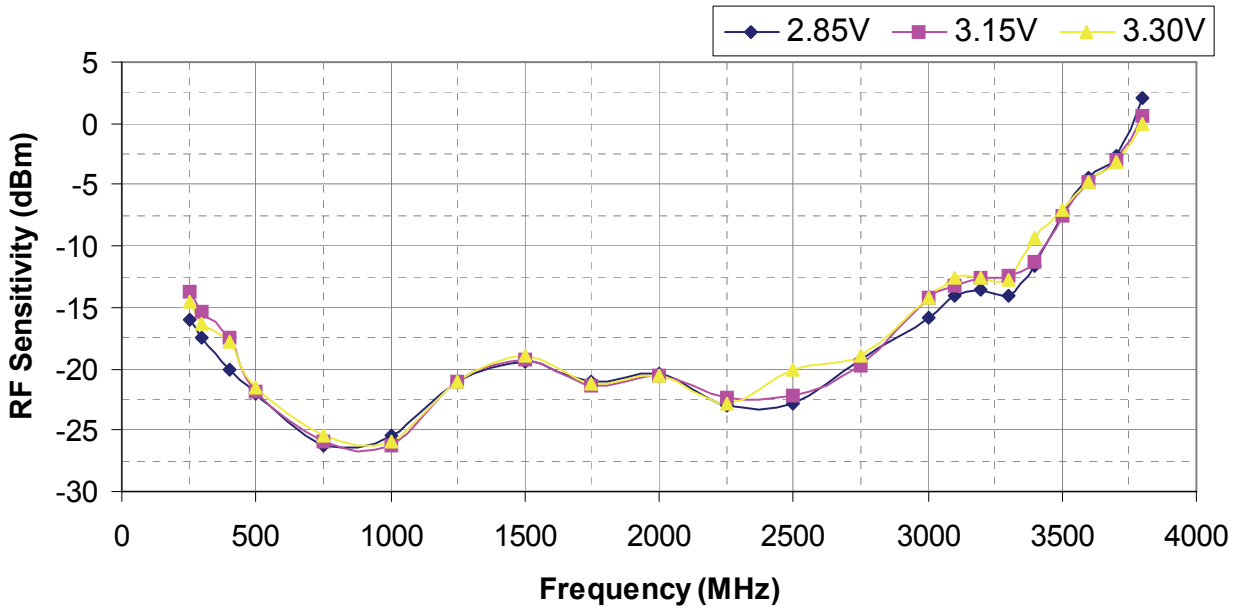


Figure 6. Equivalent Input Diagram: Reference Input

Reference Input

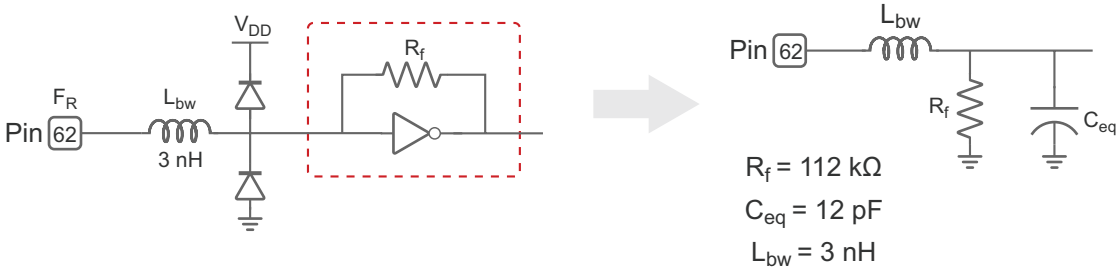


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Figure 7. Equivalent Input Diagram: Main Input

Main Input

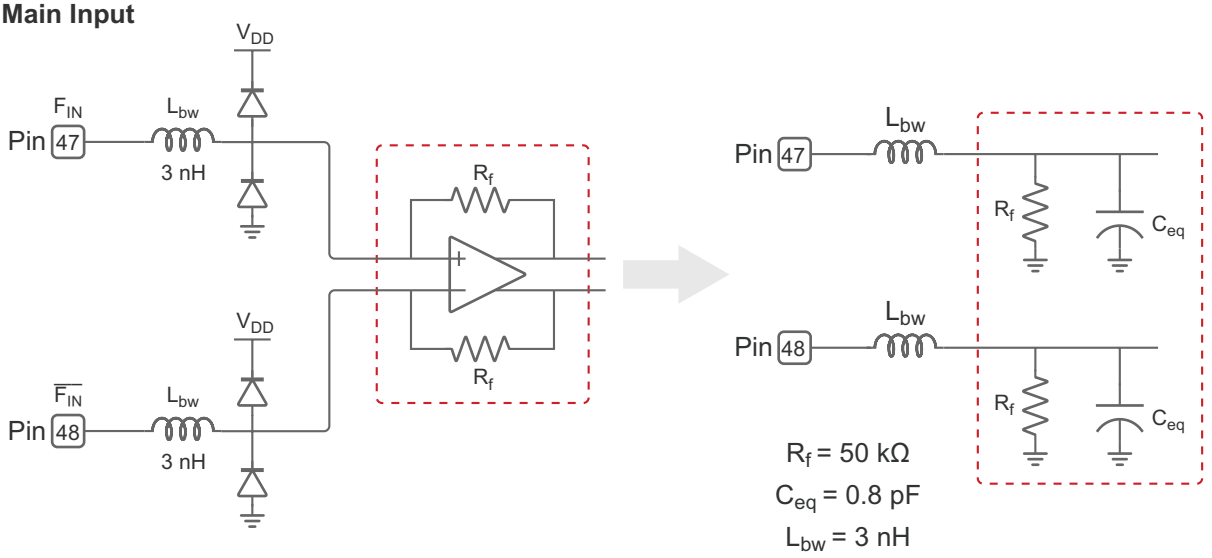

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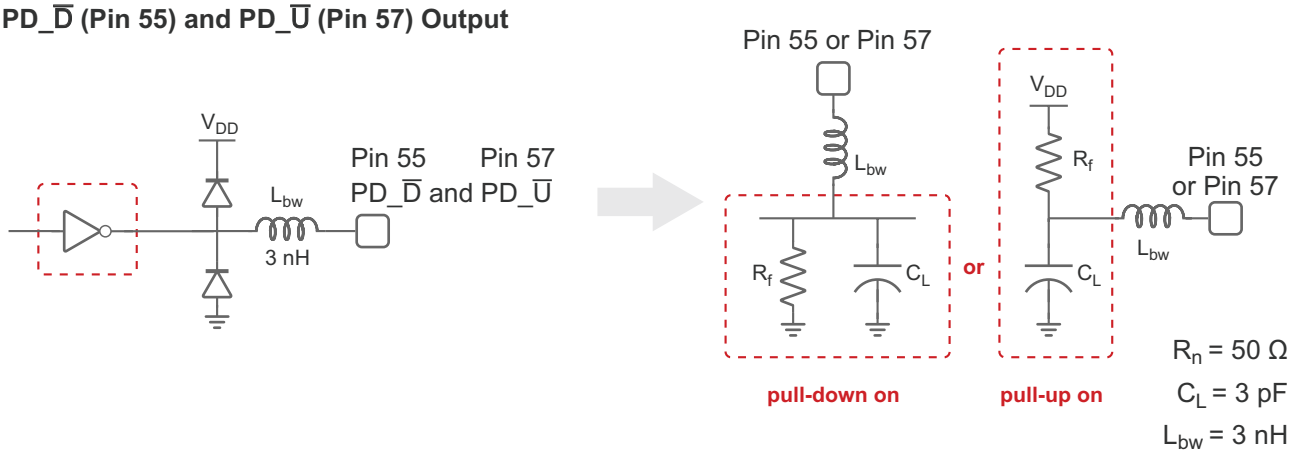
Figure 8. Equivalent Output Diagram: PD_$\overline{D}$ & PD_$\overline{U}$ Outputs

PD_$\overline{D}$ (Pin 55) and PD_$\overline{U}$ (Pin 57) Output



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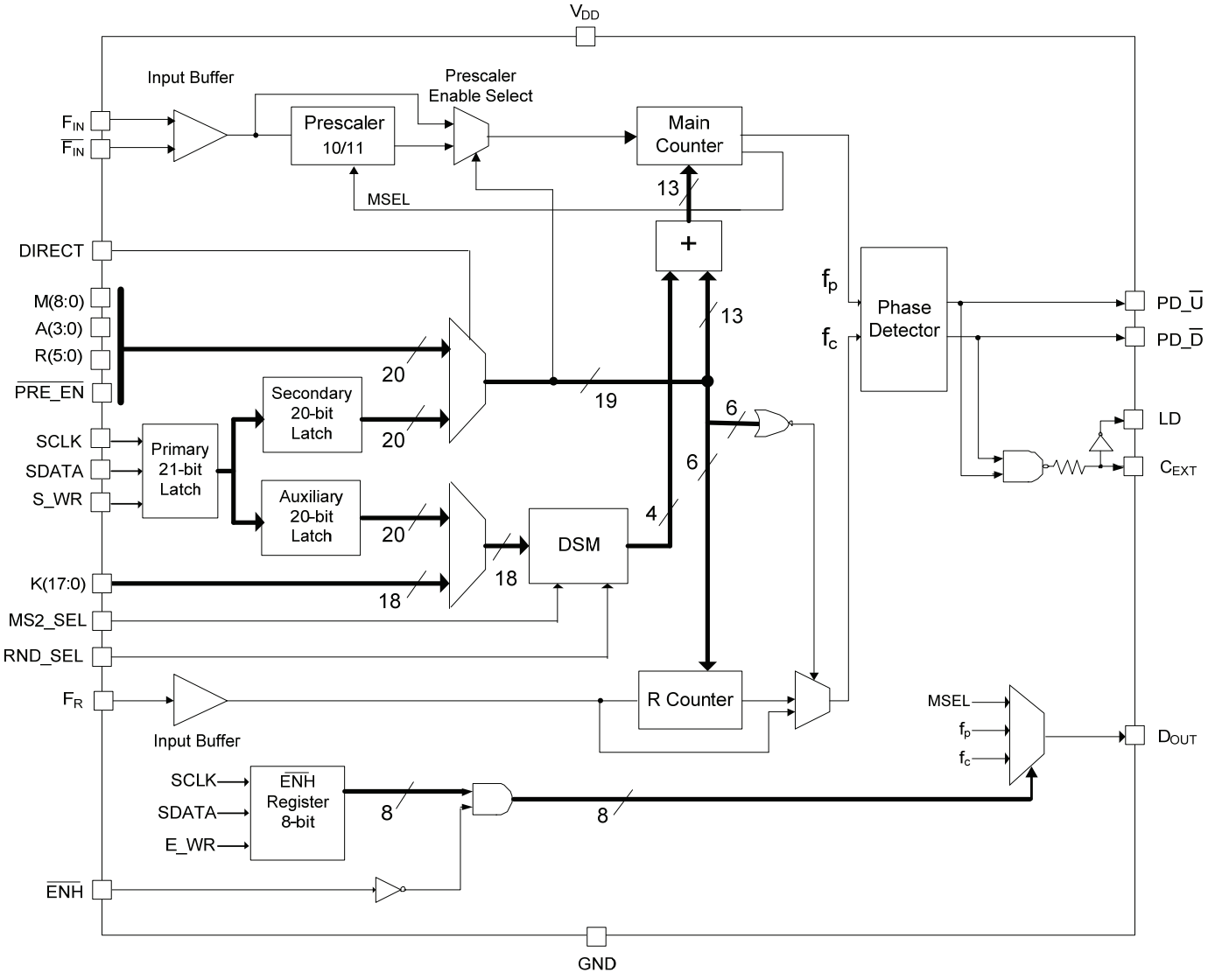
Functional Description

The PE97632 consists of a prescaler, counters, an 18-bit delta-sigma modulator (DSM) and a phase detector. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The DSM modulates the “A” counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. Data is written into the internal registers via the three wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 9. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

The main counter chain divides the RF input frequency (F_{IN}) by an integer or fractional number derived from the values in the M and A counters, and the DSM input word K.

The part can be operated in integer-N mode or in two different fractional-N modes. Setting K and RND_SEL = 0 operates the part in integer-N mode. Setting K to a non-zero value operates the part in either fractional-N mode.

The fractional-N modes use a MASH (**M**ulti-st**A**ge noise **SH**aping) decimation structure.

The MASH-1-1 mode is a 2nd order fractional dithering using four (2^2) N values: N-1, N, N+1, N+2.

MASH-1-1-1 mode is a 3rd order fractional dithering using eight (2^3) N values: N-3, N-2, N-1, N, N+1, N+2, N+3, N+4.

Setting the MS2_SEL pin HIGH enables MASH-1-1 mode and LOW enables MASH-1-1-1 mode. MASH -1-1 has a 40 dB/dec slope away from the carrier while MASH-1-1-1 has a 60 dB/dec slope.

The 18-bit accumulator size fixes the fractional value to $K/2^{18}$. However, there is an additional bit in the DSM that acts like an extra bit (19^{th} bit). This bit is enabled by setting the RND_SEL pin HIGH. Enabling this bit has the benefit of reducing the spurious levels. However, a small, positive frequency offset will occur which is calculated as:

$$F_{offset} = [F_R / (R + 1)] / 2^{19} \quad (1)$$

Using the part in either MASH mode will yield a fractional spur at

$$F_{spur} =$$
$$[(2K + RND\_SEL) / 2^{19}] \times f_c \quad 1 \leq K \leq 2^{17} \quad (2)$$
$$[1 - (2K + RND\_SEL) / 2^{19} \times f_c \; (2^{17} + 1) \leq K \leq (2^{18} - 1)$$

Where f_c is the comparison frequency.

MASH-1-1-1 mode reduces this spur for an increase in the phase noise and decrease in the number of valid programming frequencies.

All of the following equations do not take into account the frequency offset from RND_SEL. If this offset is important to a specific frequency plan, it should be taken into account accordingly.

During normal operation, the output from the main counter chain (f_p) is related to the VCO frequency (F_{IN}) by the following equations:

$$f_p = F_{IN} / (N + K/2^{18}) \quad (3)$$

where

$$N = 10 \times (M + 1) + A$$

$$A \leq M + 1, \; 1 \leq M \leq 511$$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{IN} = (N + K/2^{18}) \times [F_R / (R + 1)] \quad (4)$$

where

$$N = 10 \times (M + 1) + A$$

$$A \leq M + 1, \; 1 \leq M \leq 511$$

A consequence of the upper limit on A is that:
In integer-N mode, to obtain contiguous channels, F_{IN} must be $\geq 90 \times [F_R / (R + 1)]$.

In MASH-1-1 mode, to obtain contiguous channels, F_{IN} must be $\geq 91 \times [F_R / (R + 1)]$.

In MASH-1-1-1 mode, to obtain contiguous channels, F_{IN} must be $\geq 93 \times [F_R / (R + 1)]$.

The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M. Programming the M counter with the minimum allowed value of “1” will result in a minimum M counter divide ratio of “2”.

Prescaler Bypass Mode (*)

Setting the frequency control register bit $\overline{\text{PRE\_EN}}$ HIGH allows F_{IN} to bypass the ÷ 10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly.

The following equation relates F_{IN} to the reference frequency F_R:

$$F_{IN} = (M + 1) \times [F_R / (R + 1)] \quad (5)$$

where

$$1 \leq M \leq 511$$

(*) Only Integer-N mode

In the frequency bypass mode, neither A counter nor K counter is used; therefore, only integer-N operation is possible.

Reference Counter

The reference counter chain divides the reference frequency (F_R) down to the phase detector comparison frequency f_C.

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_C = F_R / (R + 1) \quad (6)$$

where

$$0 \leq R \leq 63$$

Note that programming R with a “0” will pass the reference frequency (F_R) directly to the phase detector.

Register Programming

Serial Interface Mode

While the E_WR input is LOW and the S_WR input is LOW, serial input data (SDATA input), B_0 to B_{20}, are clocked serially into the primary register on the rising edge of SCLK, MSB (B_0) first. The LSB is used as an address bit. When 0, the contents from the primary register are transferred into the secondary register on the rising edge of either S_WR according to the timing diagrams shown in *Figure 10*. When 1, data is transferred to the auxiliary register according to the same timing diagram. The secondary register is used to program the various counters, while the auxiliary register is used to program the DSM.

Data are transferred to the counters as shown in *Table 8*.

While the E_WR input is HIGH and the S_WR input is LOW, serial input data (SDATA input), B_0 to B_7, are clocked serially into the enhancement register on the rising edge of SCLK, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in *Figure 10*. After the falling edge of E_WR, the data provide control bits as shown in *Table 9* will have their bit functionality enabled by asserting the $\overline{\text{ENH}}$ input LOW.

Direct Interface Mode

Direct Interface mode is selected by setting the DIRECT input HIGH.

Counter control bits are set directly at the pins as shown in *Table 7* and *Table 8*.

Table 7. Secondary Register Programming

Interface Mode	$\overline{\text{ENH}}$	R_5	R_4	M_8	M_7	$\overline{\text{PRE\_EN}}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	Addr
Direct	1	R_5	R_4	M_8	M_7	$\overline{\text{PRE\_EN}}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	0

Note: * Serial data clocked serially on SCLK rising edge while E_WR LOW and captured in secondary register on S_WR rising edge.

MSB (first in)

(last in) LSB

Table 8. Auxiliary Register Programming

Interface Mode	$\overline{\text{ENH}}$	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	Rsrv	Rsrv	Addr
Direct	1	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	X	X	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	1

Note: * Serial data clocked serially on SCLK rising edge while E_WR LOW and captured in auxiliary register on S_WR rising edge.

MSB (first in)

(last in) LSB

Table 9. Enhancement Register Programming

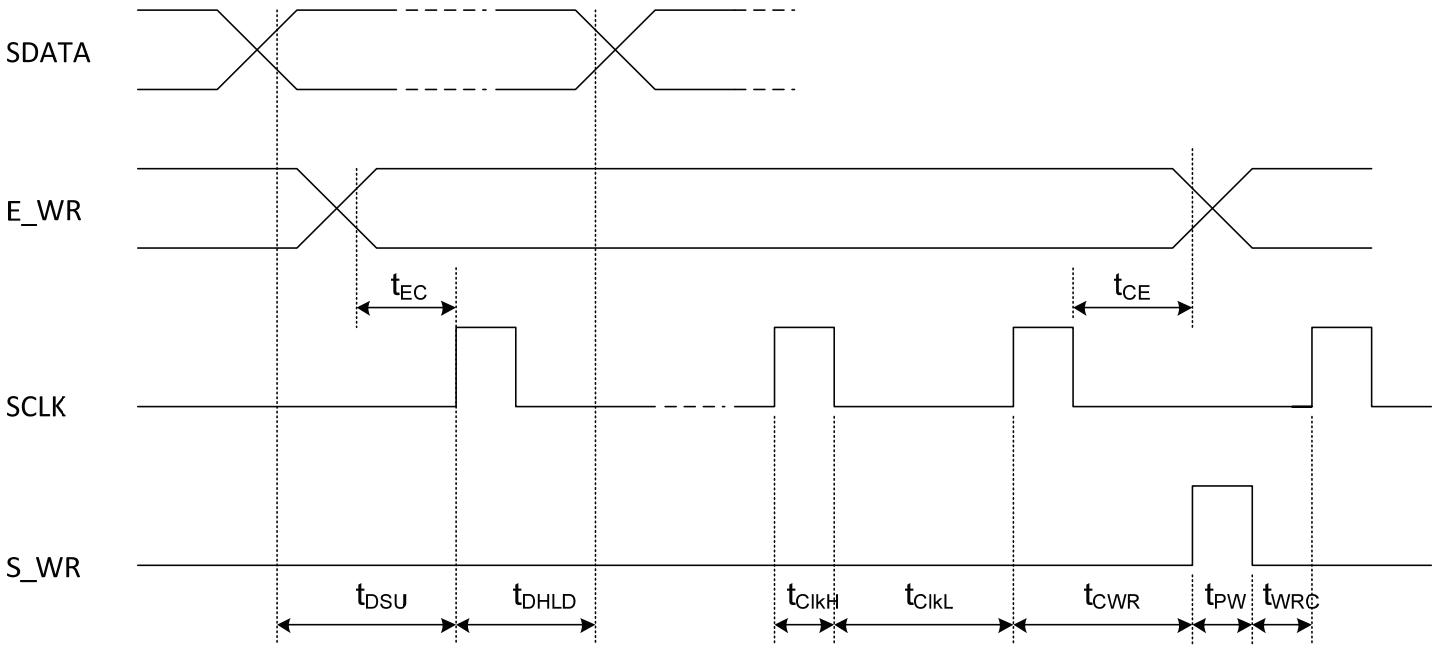
Interface Mode	$\overline{\text{ENH}}$	Reserved	Reserved	f_p output	Power Down	Counter load	MSEL output	f_c output	LD Disable
Serial*	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

Note: * Serial data clocked serially on SCLK rising edge while E_WR HIGH and captured in the double buffer on E_WR falling edge.

MSB (first in)

(last in) LSB

Figure 10. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 10. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserve*	Reserved.
Bit 1	Reserve*	Reserved.
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the reference counter output onto the D_{OUT} output.
Bit 7	LD Disable	Disables the LD pin for quieter operation.

Note: * Program to 0.

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_$\overline{U}$, and PD_$\overline{D}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_$\overline{D}$ pulses LOW. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_$\overline{U}$ pulses LOW. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

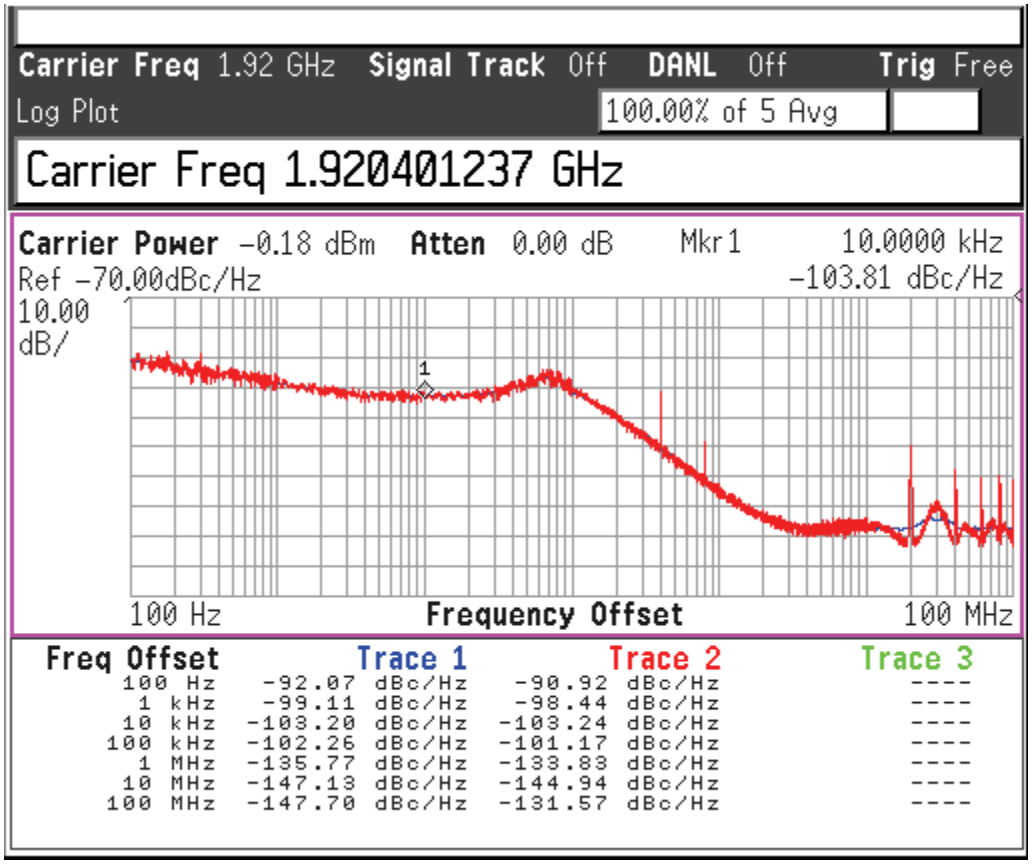
For the UP and DOWN mode, PD_$\overline{U}$ and PD_$\overline{D}$ drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to $V_{DD}/2\pi$.

PD_$\overline{U}$ pulses cause an increase in VCO frequency and PD_$\overline{D}$ pulses cause a decrease in VCO frequency, for a positive Kv VCO.

A lock detect output, LD is also provided, via the pin C_{EXT}. C_{EXT} is the logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$ waveforms, which is driven through a series 2 kΩ resistor. Connecting C_{EXT} to an external shunt capacitor provides low pass filtering of this signal. C_{EXT} also drives the input of an internal inverting comparator with an open drain output. Thus LD is an "AND" function of PD_$\overline{U}$ and PD_$\overline{D}$.

Figure 11. Typical Phase Noise

A typical phase noise plot is shown below. "Trace 1" is the smoothed average, and "Trace 2" is the raw data.



Test conditions: MASH-1-1 mode. F_{OUT} = 1.9204 GHz, $f_{COMPARISON}$ = 20 MHz, V_{DD} = 3.3V, temp = +25 °C, loop bandwidth = 50 kHz.

Figure 12. Package Drawing (dimensions are in millimeters)
68-lead CQFJ

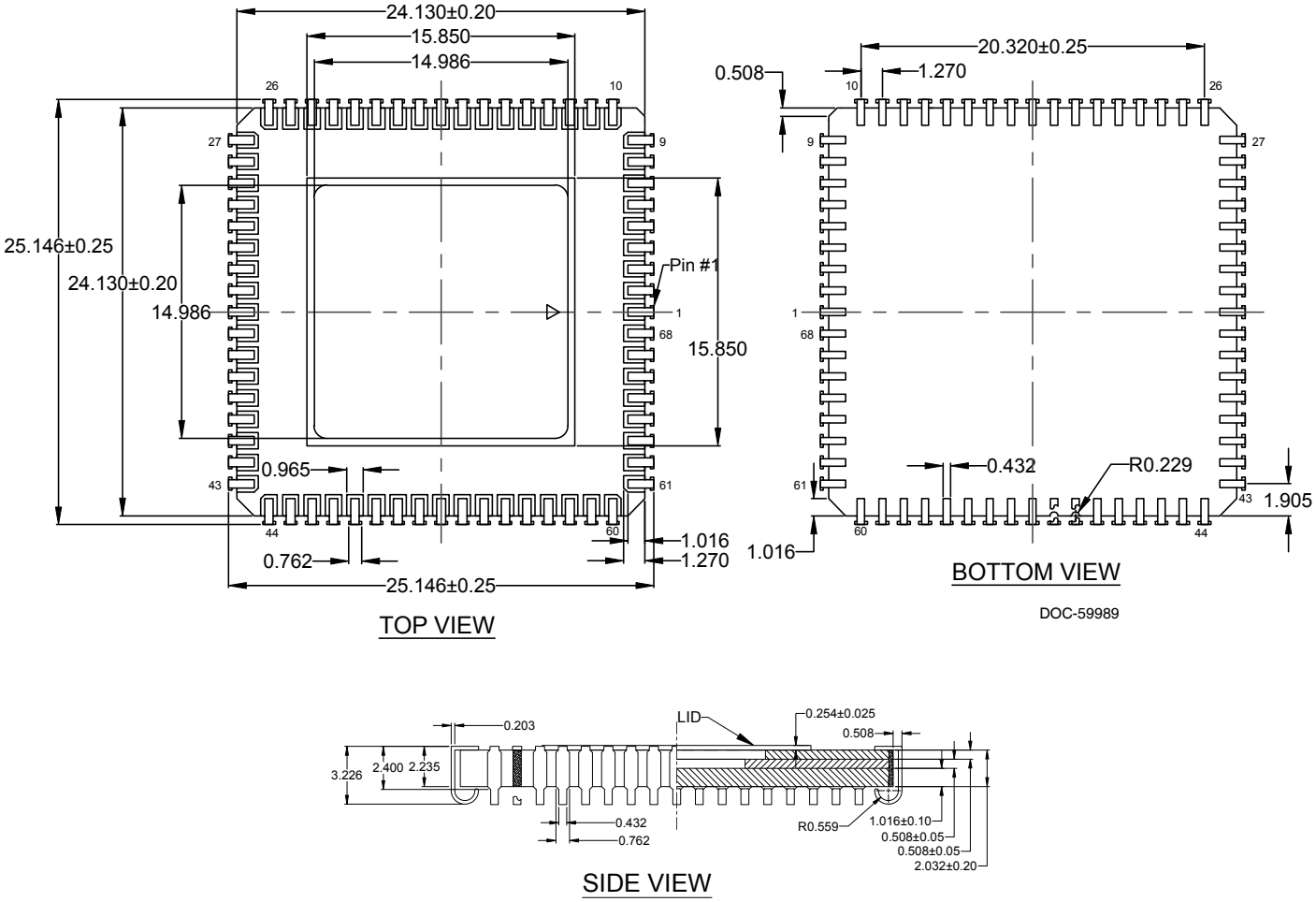


Figure 13. Top Marking Specifications

Not to scale PRT-25223

Line 1: Pin 1 indicator △, e2v and Peregrine logo
Line 2: Part number (XX will be specified by the purchase order)
Line 3: Date code (last two digits of the year and work week)
Line 4: Wafer lot # (as many characters as room allows)
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside marking on any of the Peregrine products.

Table 11. Ordering Information

Order Code	Description	Packaging	Shipping Method
97632-01[1]	Engineering samples	68-lead CQFJ	21 units / tray
97632-11	Flight units	68-lead CQFJ	21 units / tray
97632-00	Evaluation kit		1/Box

Note: * The 97632-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE97632-11 flight units. The PE97632-01 device provides the same functionality and footprint as the PE97632-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
e2v ~ http://www.teledyne-e2v.com ~ inquiries@e2v-us.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. ***Preliminary Specification:*** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).