SIEMENS

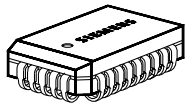
ISDN Exchange Power Controller (IEPC)

PEB 2025

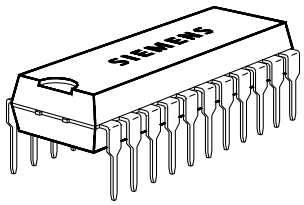
CMOS IC

Features

- Supplies power to up to four transmission lines
- CCITT recommendations compatible for power feed at the “S” interface
- Each line is individually powered and controlled
- Wide field of applications:
  - two- and four wire transmission lines
  - point-to-point configurations
  - point-to-multipoint configurations
- Maximum output current programmable up to 150 mA
- Programmable switch-off characteristic by overcurrent detection
- Automatic restart after removing overload conditions
- Status detectors for each line driver
- Microprocessor compatible interface
- Interrupt output for detection of any malfunction
- High voltage CMOS technology (60 V)



P-LCC-28-R



P-DIP-22

Type	Version	Ordering Code	Package
PEB 2025-N	V 1.5	Q67100-H6300	P-LCC-28-R (SMD)
PEB 2025-P	V 1.5	Q67100-H6241	P-DIP-22

The IEPC is an integrated power controller especially designed for feeding two- and four wire transmission lines. The IEPC is fully compatible to the CCITT recommendations on power feed at the “S”-interface. So the IEPC can be used in PABX/Central Office and in intelligent NT´s.

The IEPC supplies power up to four transmission lines. Each line is individually powered and controlled via microprocessor interface. An interrupt output signals any malfunction to the microprocessor.

The high voltage CMOS technology (60 V) ensures a wide field of applications:

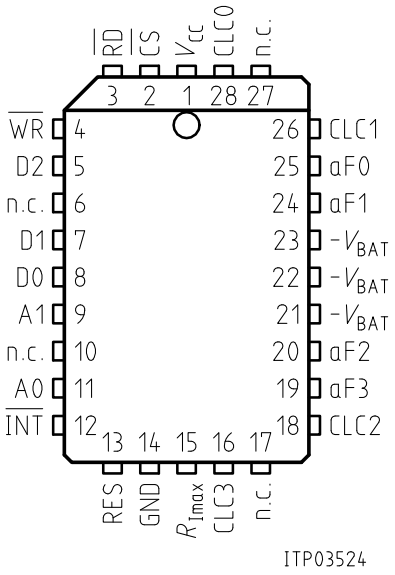
- two- and four wire transmission lines
- point-to-point configurations
- point-to-multipoint configurations etc.

Programmable output current and thermal shut down guards the IEPC against overloads.
The IEPC offers a special transient permitted overload state. Momentary overloads within a specified range e.g. by connecting a TE to a powered line, however, will not activate the current-limit-circuits of the power controller. If overload is detected, the line driver will turn off according to a time and current dependent turn off characteristic.
The IEPC offers an automatic restart-mode. In this case the IEPC tries to power up the line periodically, thus the feeding of a line will return automatically after the overload-conditions are removed.

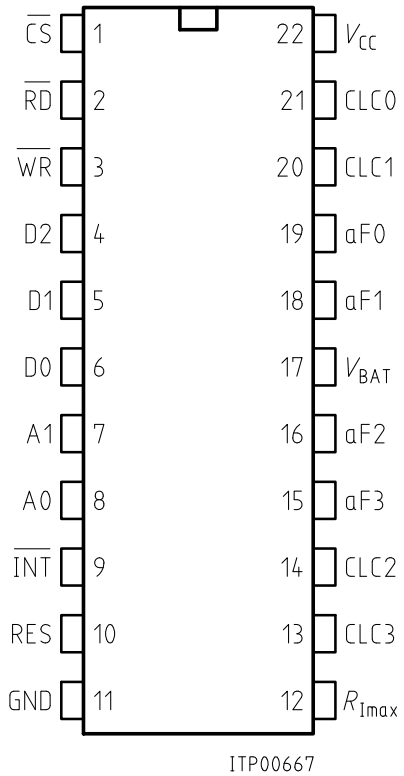
Pin Configurations

(top view)

P-LCC-28-R



P-DIP-22



Pin Definitions and Functions

Pin No. P-DIP-22	Pin No. P-LCC-28	Symbol	Input (I) Output (O)	Function
17	21, 22, 23	V_{BAT}	I	**Supply Voltage:** This pin has to be connected to the negative supply voltage. V_{BAT} supplies power to all line drivers.
22	1	V_{CC}	I	**Digital Supply Voltage:** + 5V
11	14	GND	I	**Ground:** Digital **Note:** GND has to be connected to ground battery (positive supply voltage)
19, 18, 16, 15	25, 24, 20, 19	aF0 - aF3	O	**a**-Line **F**eeding: aF_i are the line driver outputs
12	15	R_{Imax}	I	**Current Limit:** Using an external resistor connected between R_{Imax} and GND, the maximum limit is the same to all line drivers.
21, 20, 14, 13	28, 26, 18, 16	CLC0 - CLC3	I	**C**urrent **L**imit **C**haracteristic: By connecting external capacitors between CLC_i and GND, the time-dependent turn off-characteristics of the line drivers are defined.
1	2	$\overline{CS}$	I	**Chip Select:** A logic low on $\overline{CS}$ enables $\overline{RD}$ and $\overline{WR}$ communication between the processor and the IEPC.
3	4	$\overline{WR}$	I	**Write:** A logic low on this pin, while $\overline{CS}$ is low, enables the IEPC to accept command words from the processor.
2	3	$\overline{RD}$	I	**Read:** A low on this pin (while $\overline{CS}$ is low) enables the IEPC to release status onto the data bus for the processor.
6, 5, 4	8, 7, 5	D0 - D2	I/O	**Data Bus:** Control, status and command information are transferred via this bus between IEPC and processor.
8, 7	11, 9	A0, A1	I	**Address Bus:** These inputs select the internal registers while chip select is active.
10	13	RES	I	**Reset:** A logic high on the RES input sets the device into the initial state.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP-22	Pin No. P-LCC-28	Symbol	Input (I) Output (O)	Function
9	12	$\overline{\text{INT}}$	O	**Interrupt:** Open drain output. If any malfunction is detected by the IEPC, this interrupt-pin is activ low.
–	6, 10, 17, 27	N.C.		Not connected

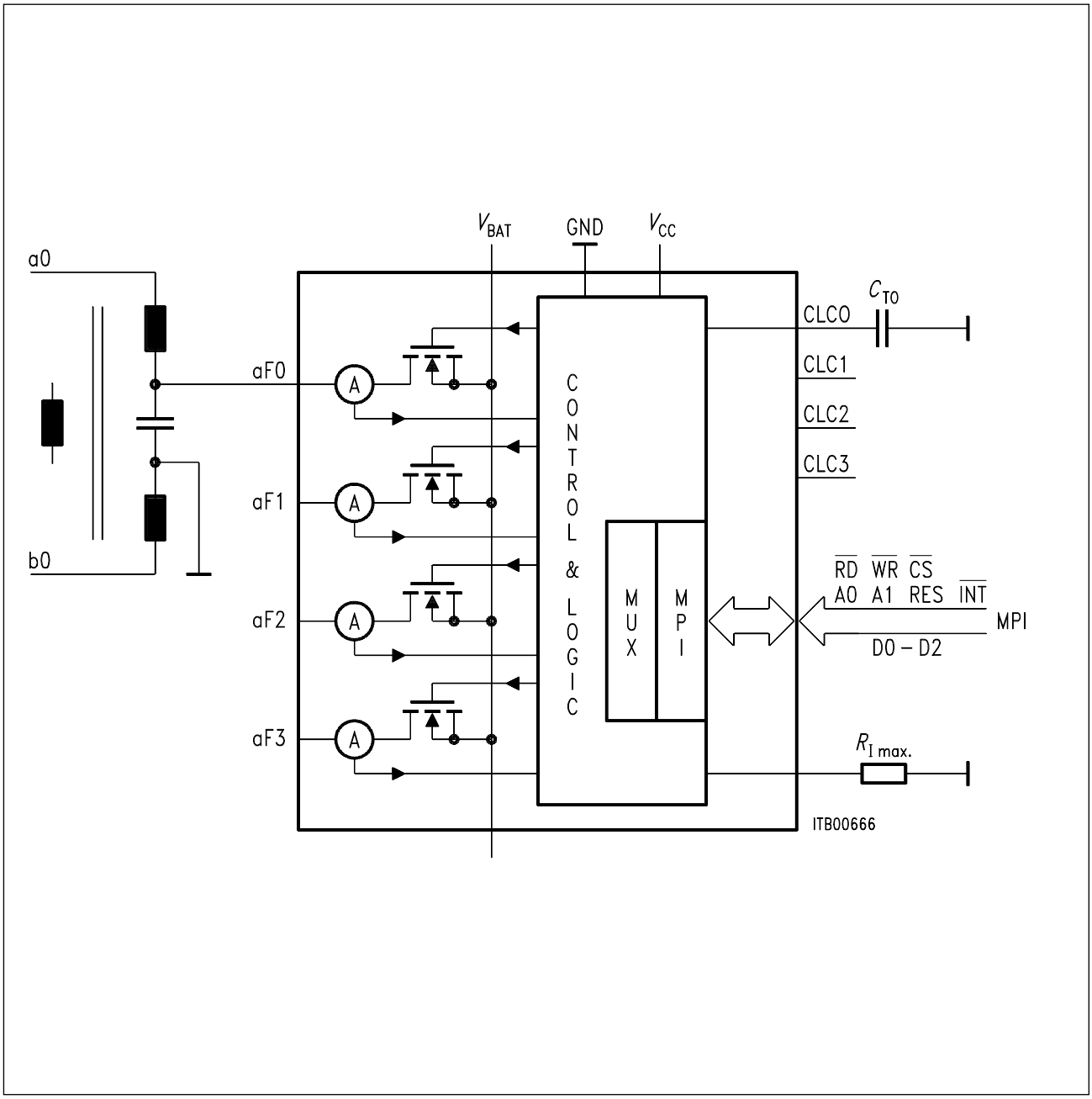


Figure 1
Functional Block Diagram

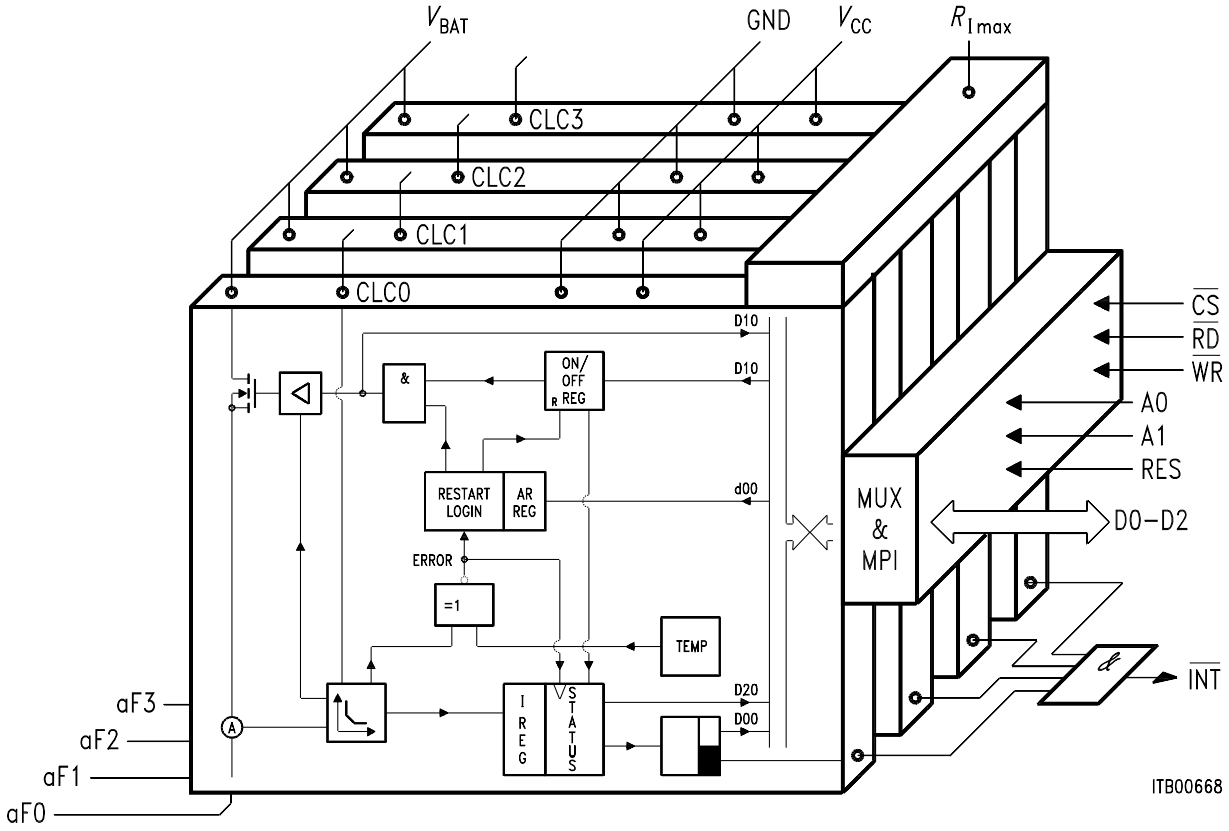


Figure 2
IEPC Architecture

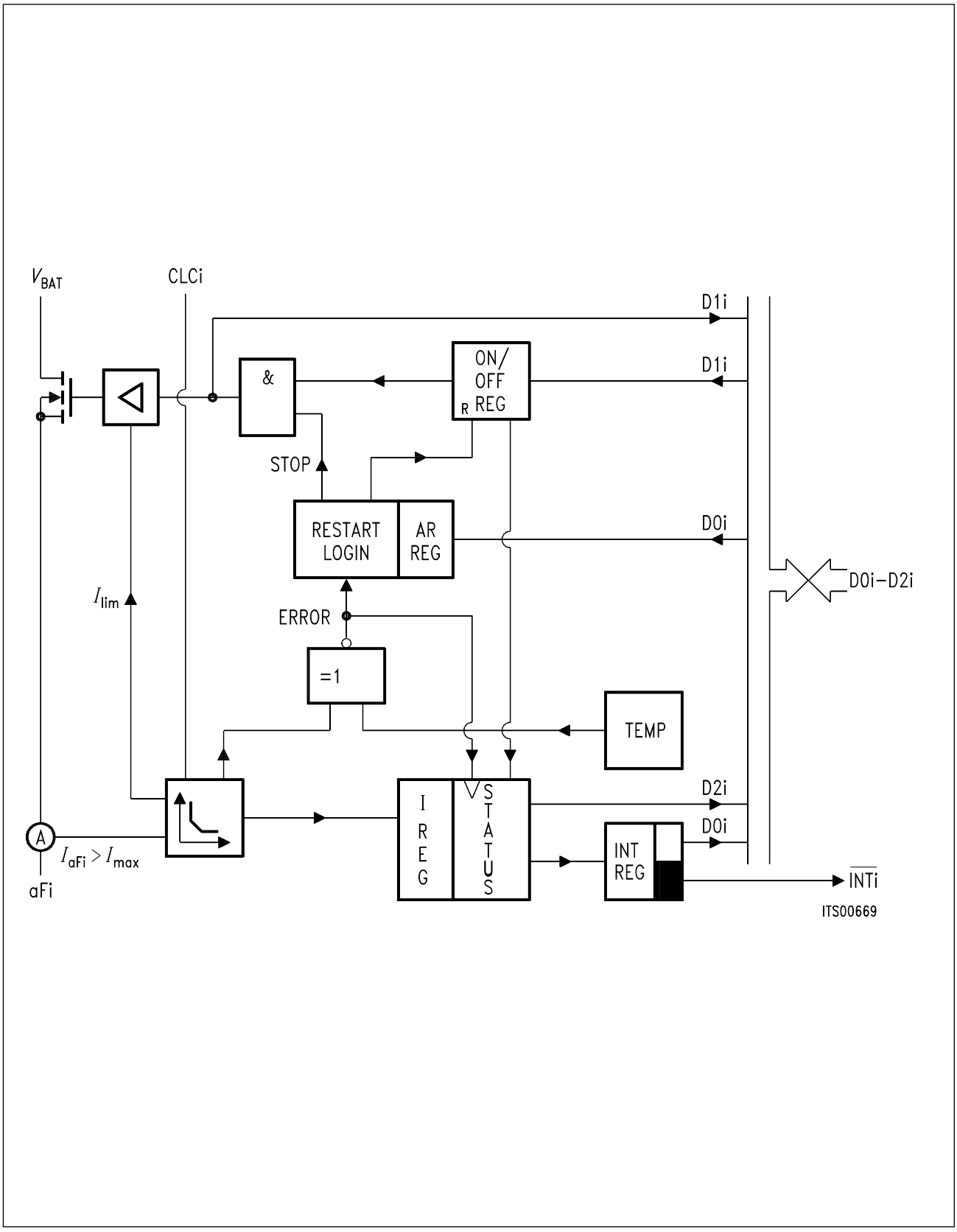


Figure 3
Functional Diagram of One Line Driver

Functional Description

Figure 2 shows the IEPC organization. The exchange power controller contains one line driver for each of the four transmission lines. A line oriented register architecture allows very simple software control.
Figure 3 shows the functional diagram of one of the four line drivers. The IEPC consists of a high voltage analog part and a low voltage digital part.
The ground battery (positive supply voltage) has to be connected to GND (pin 11).
When powering up the IEPC, the line drivers are switched off and all registers are cleared. The same initialized state can be achieved by an external high signal applied to the pin RES.

Analog Part

Power Switches

The negative pole of the supply, e.g. an exchange battery, has to be connected to the pin V_{BAT}. After an ON-command to line i, a high voltage MOS-FET will connect the negative supply voltage from V_{BAT} to aFi.

Current Control

The current of each negative wire (aFi) is controlled individually.
The maximum feeding current is programmed by an external resistor R_{I} connected between pin R_{Imax} and GND (see **figure 1**) and is same to all four lines.

aFi Line Control: Connecting an external capacitor C_{Ti} between CLCi and GND (see **figure 1**), the IEPC offers a special time and current dependent turn off characteristic. The IEPC will limit the aFi line current to protect the IEPC against over currents and to avoid discharging of the feeding source. **Figure 4** shows this **t**ransient **p**ermitted **o**verload (TPO) state.

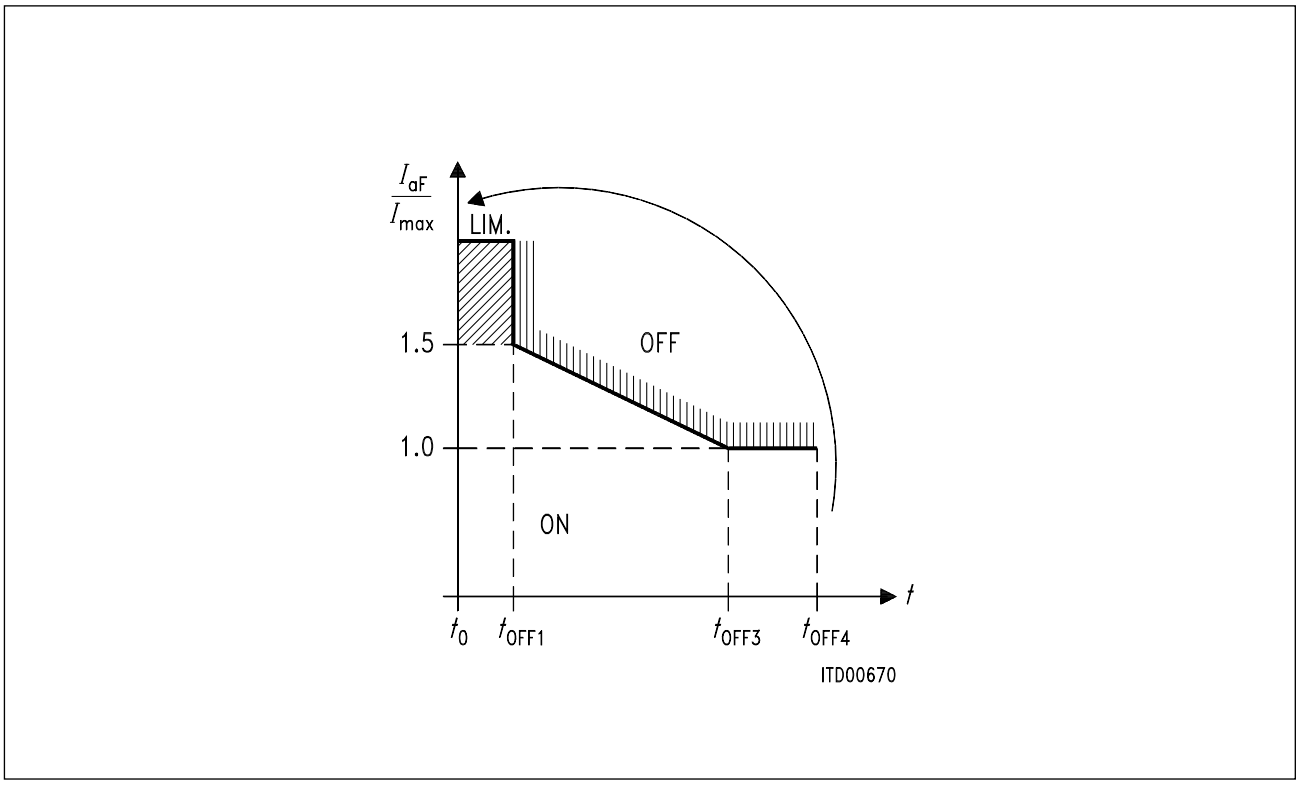


Figure 4
Diagram of the Transient Permitted Overload (TPO) State

During the first timestep (t_{OFF1}) since overload of the negative wire aFi was detected ($I_{aFi} \geq I_{max}$), the current will be limited. Within the next timestep (till t_{OFF3}) the current must drop from 1.5 I_{max} to I_{max}, otherwise the line driver turns off. After t_{OFF3} any current above I_{max} results turn off the line driver. After t_{OFF4}, if no turn off of the line driver has occured, the current limiting characteristics becomes active again and will be prepared for detection of further overload conditions.

Timestep t_{OFF1} is defined by charging the capacitor C_T with the current I_{CLC} which is specified in the AC characteristics.

t_{OFF3} and t_{OFF4} depend on t_{OFF1}:

$$t_{OFF3} \approx 15\ t_{OFF1} \qquad t_{OFF4} = t_{AR} \approx 50\ t_{OFF1}$$

Note:

If aFi has been switched off due to the time dependent current limiting circuit while C_{Ti} is charged, an ON command has no effect. To turn on the line driver C_{Ti} has to be discharged.

C_{Ti} will be discharged:

- by an OFF command
- if t_{OFF4} is reached
- in non-automatic restart mode if the line driver has been switched off due to an overload condition.

If overload is once detected, every exceeding of the current limits will turn off the line driver until t_{OFF4} is reached. The time dependent current limiting circuit will **not** be reseted if once overload is detected, even if the feeding current drops below I_{max} until t_{OFF4} is reached.

If pin CLC is connected to GND the time and current dependent turn off characteristic is disabled and the IEPC limits the driver current.

Automatic Restart

In connection with the time-dependent-current-limitation, the IEPC offers a programmable automatic restart mode (see digital part).
If overload is detected ($I_{aFi} \geq I_{max}$) at t_0, the IEPC starts charging the external capacitor C_{Ti}.

Automatic restart enabled: If the line driver has been switched off due to the time dependent turn off characteristic, C_{Ti} will **not** be discharged by the IEPC. If t_{OFF4} is reached the line driver restarts automatically. So the time difference between turn off and automatic restart is variable and depends on the moment of turn off.

Autorestart disabled: If t_{OFF4} is reached **or** if the line driver has been switched off due to the time dependent turn off characteristic, C_{Ti} will be discharged by the IEPC. During the discharge time of C_{Ti}, every restart of line i via microprocessor interface will be ignored by the IEPC.
(With C_{Ti} = 10 µF the maximum discharge time is 10 ms.)

Temperature Shut-Off

The temperature of each line driver is monitored separately. If the temperature of one line driver exceeds the shut-off temperature (approx. 120 °C), the transmission line will turn off. The shut-off temperature of the other three line drivers will be increased by approx. 25 °C.

Open Loop Detection

The IEPC offers an easy method to detect open loops. If the line driver aFi is in the OFF state a constant current source (approx. 100 µA) feeds the output aFi. In case of open loop (**figure 5**) the voltage at output aFi rises up to 3 V.

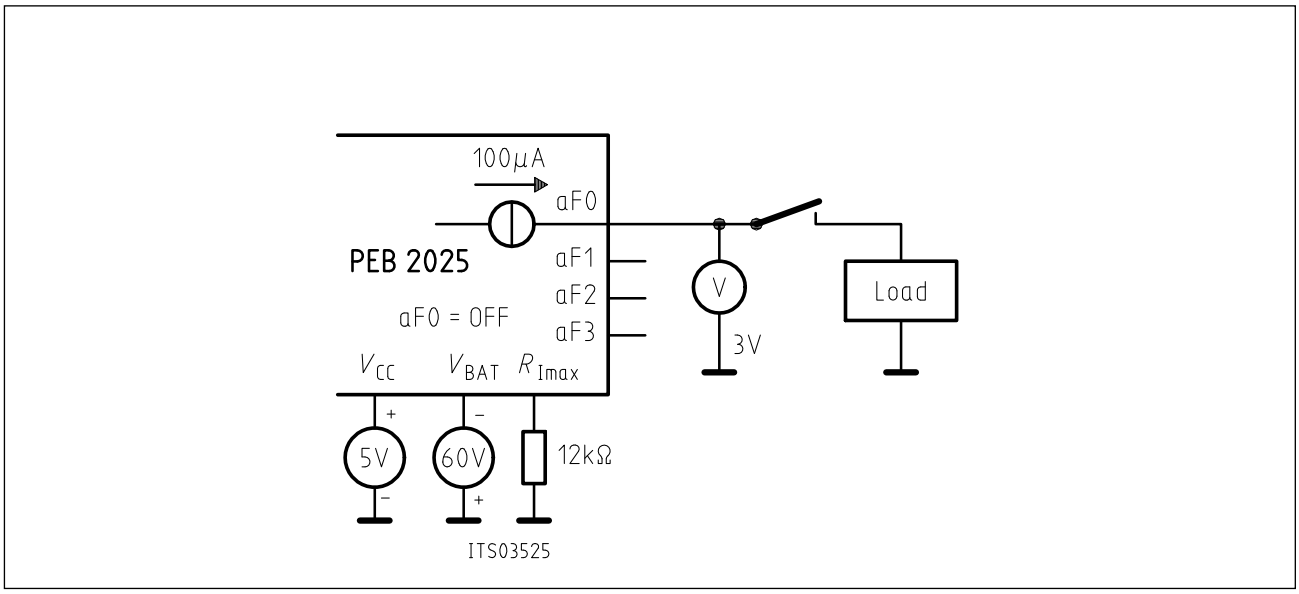


Figure 5
Open Loop Detection

Digital Part

The microprocessor interface (MPI) communicates with a processor which controles the IEPC. This MPI contains a 3-bit data bus, a 2-bit address bus, read-, write-, chip select- and reset lines.
If chip select is inactive (logic high) the data bus is in a high impedance state and no communication between the processor and IEPC is possible.
The IEPC contains a line oriented register architecture, i.e. one read and one write register for each line. A read or write cycle affects the addressed register, which is related to the corresponding line driver.

The write register consists of three control bits per line i:

D0: Automatic Restart-bit (AR)

D1: ON/OFF-bit (ON)

D2: must be 0

The read register consists of three status bits per line i:

D0: Interrupt-bit (INT)

D1: Actual ON/OFF Driver status-bit (AO)

D3: Current Overload-bit (CO)

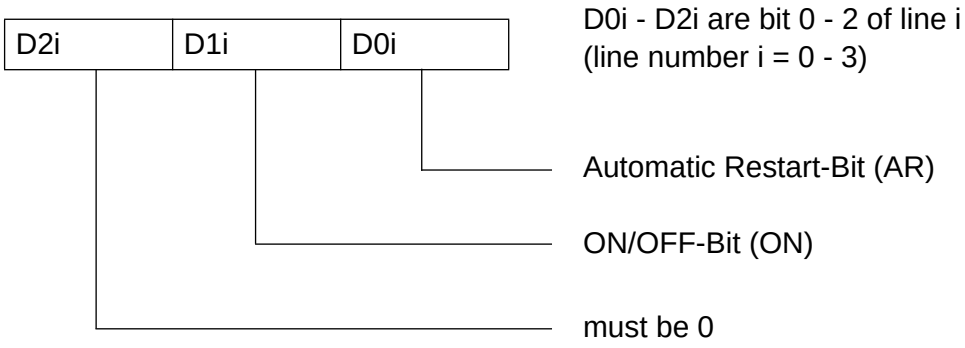
A logic high on the RES pin sets the device into an inital state: all registers of the IEPC are cleared (D0i - D2i are low).

Address Table

$\overline{CS}$	A1	A0	Selected Line
0	0	0	Line 0
0	0	1	Line 1
0	1	0	Line 2
0	1	1	Line 3
1	x	x	No access

Write Register

The write register is organized as shown below:



Automatic Restart Bit: Automatic restart mode is only possible in connection with the time-dependent-current limitation, i.e. an external capacitor must be connected between pin CLCi and GND. If D0i is high, automatic restart mode is enabled.

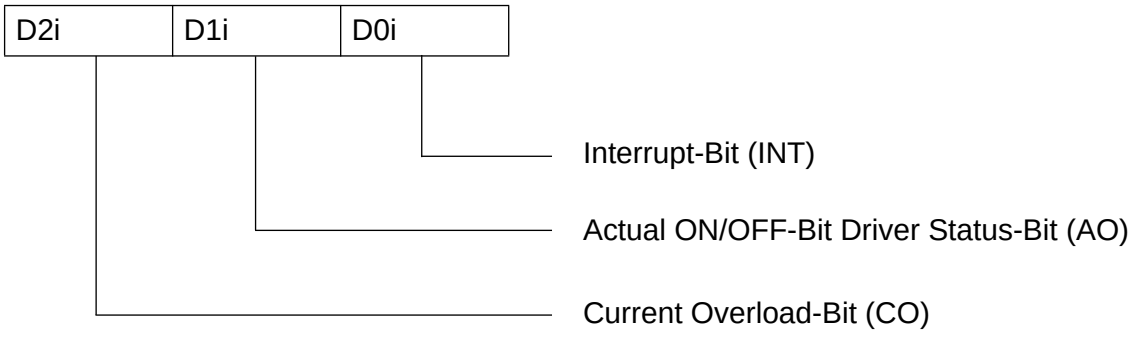
	D2i	D1i	D0i
AR enabled	0	x	1
AR disabled	0	x	0

ON/OFF-Bit: To turn a line driver on, D1i must be set to high, to turn it off, it must be set to low. An off command resets the time and current dependent turn off characteristic by discharging the external capacitor at pin CLCi.

	D2i	**D1i**	**D0i**
ON	0	1	x
OFF	0	0	x

Read Register

The read register is organized as shown below:



Interrupt-Bit: If malfunctions have been detected (current- or thermal overload) and the line driver of line i has been turned off the interrupt-bit will be set:

	D2i	**D1i**	**D0i**
Interrupt	x	x	1
Operational	x	x	0

The interrupts $\overline{INT0}$ - $\overline{INT3}$ are anded to the device output-signal $\overline{INT}$. Thus if any malfunction is detected an interrupt signal is sent to the microprocessor.

Actual ON/OFF Driver Status-Bit: D1i shows the actual status of the line driver of line i:

Driver	D2i	D1i	D0i
Driver ON	x	1	x
Driver OFF	x	0	x

Current Overload-Bit: If $I_{aFi} \geq I_{max}$ is detected and the line driver has been switched off the current overload bit will be set.

If CLCi is connected to GND, the current overload bit will **not** be set.

	D2i	D1i	D0i
Current overload	1	x	x
Operational	0	x	x

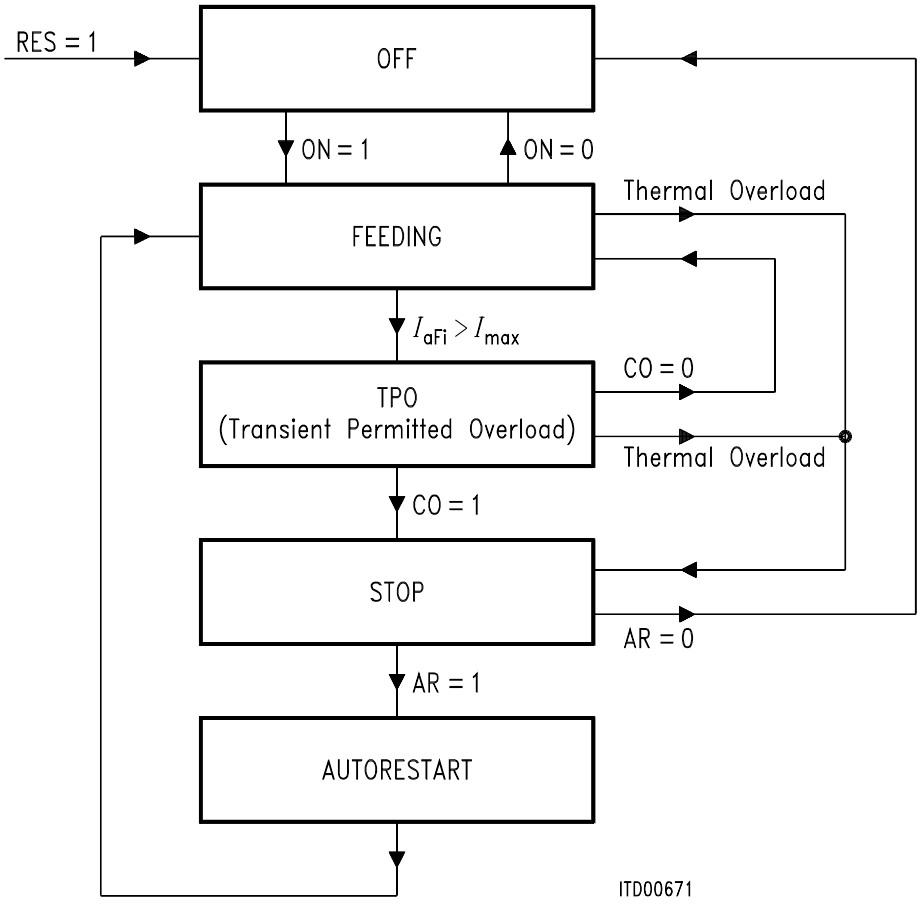


Figure 6
Line Driver State Diagram

State Diagram

Figure 6 shows the state diagram of one IEPC line driver.

A logic high on the RES input sets the device into the initial state. The line driver is switched off and all registers are cleared. The same initialized state is achieved by powering up the IEPC. After an ON-command (ON = 1) the line drivers will turn on and the IEPC is in the FEEDING-state. To return to the OFF-state the ON-bit must be cleared (ON = 0).

In the FEEDING-state the current I_{aFi} is controlled. If overcurrent is detected one of the following cases happens:

1. If an external capacitor C_{Ti} is connected between CLCi and GND and $I_{aFi} \geq I_{max}$ is detected the IEPC stays in the **T**ransient **P**ermitted **O**verload-state (TPO). Exceeding the time-current-limit the line driver turns off and the IEPC is in the STOP-state. The current overload-bit will be set (CO = 1) and C_{Ti} will be discharged by an resistor of the IEPC. Until C_{Ti} isn´t discharged completely, an ON command will be ignored. If no exceeding happens the line driver returns to the FEEDING-state.

2. If $I_{aFi} \geq I_{max}$ is detected and CLCi is connected to GND the IEPC limits the driver current. The current overload bit will not be set.

The temperature of each line driver is controlled separately. If the temperature of the line driver exceeds the shut-off temperature, the transmission line will turn off and the line driver is in the STOP-state. In this case the shut-off temperature of the other three line drivers will be increased.

There are two different ways to leave the STOP-state:

1. If the automatic restart bit is set (AR = 1) the IEPC returns after a delay time to the FEEDING-state automatically. The ON/OFF register will not be cleared.

2. If no automatic restart mode is selected (AR = 0) the IEPC returns to the OFF-state. In this case the ON/OFF register will be cleared.

As soon as the STOP-state is reached the IEPC sends an interrupt signal to the microprocessor (interrupt-pin is active low).

If the line driver is not in the terminal overload state, every rising edge of the read signal resets the interrupt bit INTi (D0i) of the selected line i. The current overload-bit C0i (D2i) will be reseted too.

If the line driver i is in the terminal overload state the rising edge of the read signal has no effect on the interrupt bit.

The internal interrupts $\overline{INT0}$ - $\overline{INT3}$ are anded to the open drain output pin $\overline{INT}$. So the interrupt pin stays activ low until all interrupt bits INT_i are reseted.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{BAT} referred to GND	V_{BAT}	– 70	0.3	V
V_{CC} referred to GND	V_{CC}	– 0.5	6	V
Voltage on pins aF0 - aF3	V_F	V_{BAT}	V_{CC}	V
Continuous current on pins aF0 - aF3 only one channel	I_F		200	mA
all channels at the same time; T_A = 25 ˚C			150	mA
all channels at the same time; T_A = 70 ˚C			130	mA
Reverse current on pins at aF0 - aF3	I_F	0	0	mA
Voltage on any other pins referred to GND	V_I	– 0.5	V_{CC} + 0.5	V
Power dissipation	P_D		1	W
Ambient temperature under bias	T_A	– 25	85	˚C
Storage temperature	T_{stg}	– 40	125	˚C
Thermal resistance system to case	$R_{th\ SA}$		50	K/W

Operating Range

Operating voltage referred to GND	V_{BAT}	– 60	– 12	V
Digital supply voltage referred to GND	V_{CC}	4.75	5.25	V
Ambient temperature	T_A	0	70	˚C

DC Characteristics

T_A = 0 to 70 ˚C; V_{BAT} = – 12 to – 60 V, V_{CC} = 5 V, GND = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply						
Supply current	I_{VBAT}			200	µA	a_{F0-3} = OFF
Digital supply current	I_{VCC}		5	10	mA	
Line Drivers						
Current control limit	I_{max}	60		90	mA	R_I = 12 kΩ
Current control limit	I_{max}	120		185	mA	R_I = 5.6 kΩ
Current limiting factor (I_{aFi})	I_{lim}/I_{max}	1.5		5		
Turn on resistance (V_{BAT} to aFi)	R_{DSon}		7	9	Ω	I_{aF} = 50 mA T_A = 25 ˚C
Logic						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	2.0			V	
L-output voltage	V_{OL}			0.45	V	I_O = 2 mA
H-output voltage	V_{OH}	2.4			V	I_O = – 1 mA

AC Characteristics

T_A = 25 ˚C; V_{BAT} = – 12 to – 60 V, V_{CC} = 5 V, GND = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Line Driver & Current Control						
Delay: ON-command to turn on line driver	t_{ON}			0.2	ms	for resistive loads
Delay: ON-command to turn off line driver	t_{OFF}			1	ms	for resistive loads
C_T charge current	I_{CLC}	100	120	140	µA	till t_{OFF1}
Current limiting time	t_{OFF1}	0.15	0.2	0.25	s	C_T = 10 µF
Current control recovery time	t_{OFF3}			3	s	C_T = 10 µF
Current control reset time	t_{OFF4}	7	10	15	s	C_T = 10 µF
Automatic restart period	t_{AR}	7	10	15	s	C_T = 10 µF

Switching Times

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
$\overline{RD}$ pulse width	t_{1R}	350			ns	
$\overline{WR}$ pulse width	t_{1W}	180			ns	
Address and $\overline{CS}$ setup time to $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	t_2	0			ns	
Address and $\overline{CS}$ hold time after $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	t_3	30			ns	
Data setup time to $\overline{WR}\uparrow$	t_4	60			ns	
Data hold time after $\overline{WR}\uparrow$	t_5	100			ns	
Data valid after $\overline{RD}\downarrow$	t_6			350	ns	
Data valid after $\overline{RD}\uparrow$	t_7	50			ns	
Data bus inactive after $\overline{RD}\uparrow$	t_8			120	ns	
Reset pulse width	t_{RES}	5			µs	

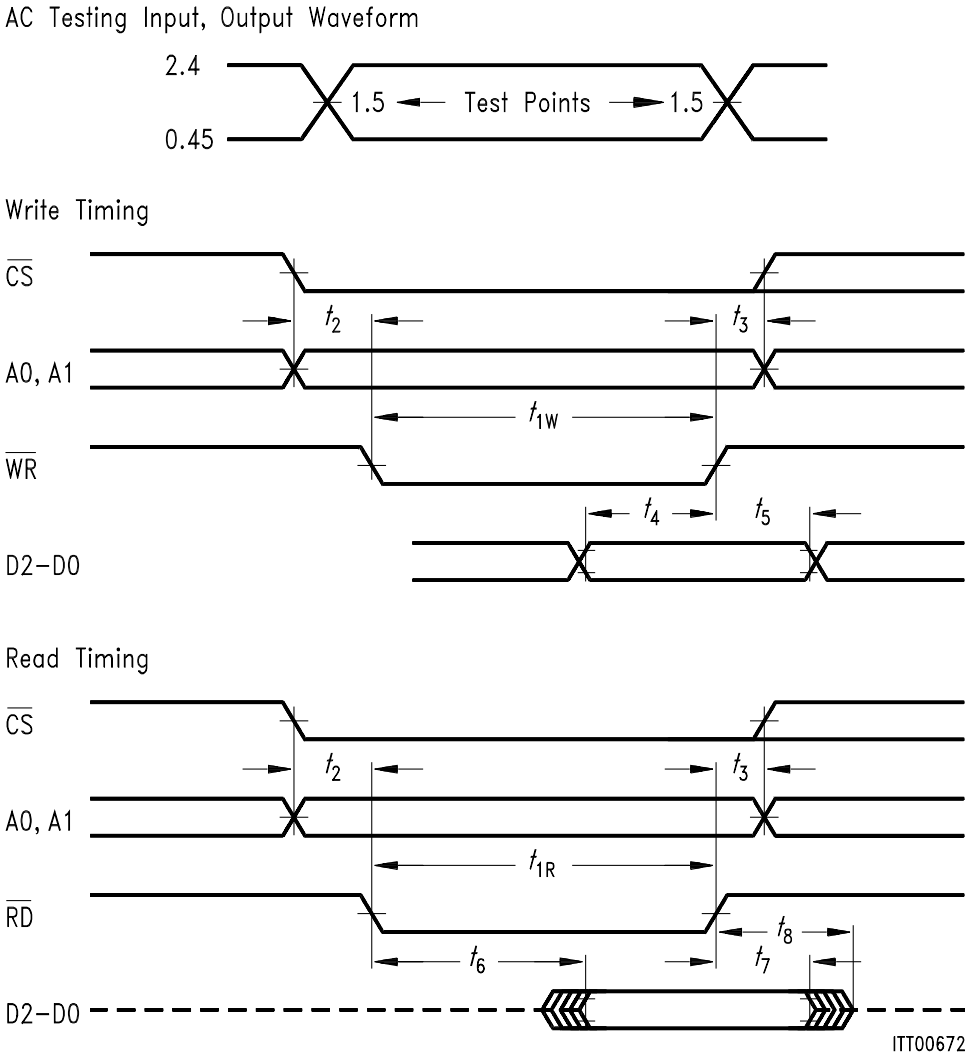


Figure 7
Waveforms

Protection Requirements

According to the absolute maximum ratings of the IEPC, the PEB 2025 has to be protected against overvoltage spikes comming in on aFi. This is done by the diodes D1 and D2 in **figure 8**. In some applications it could be necessary to protect the IEPC output aFi against reverse by using diode D3.

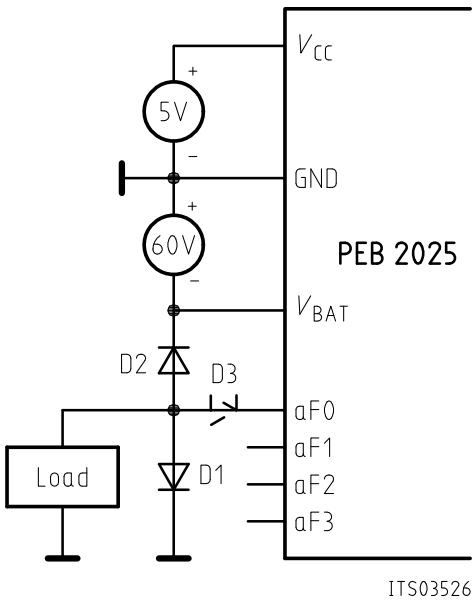
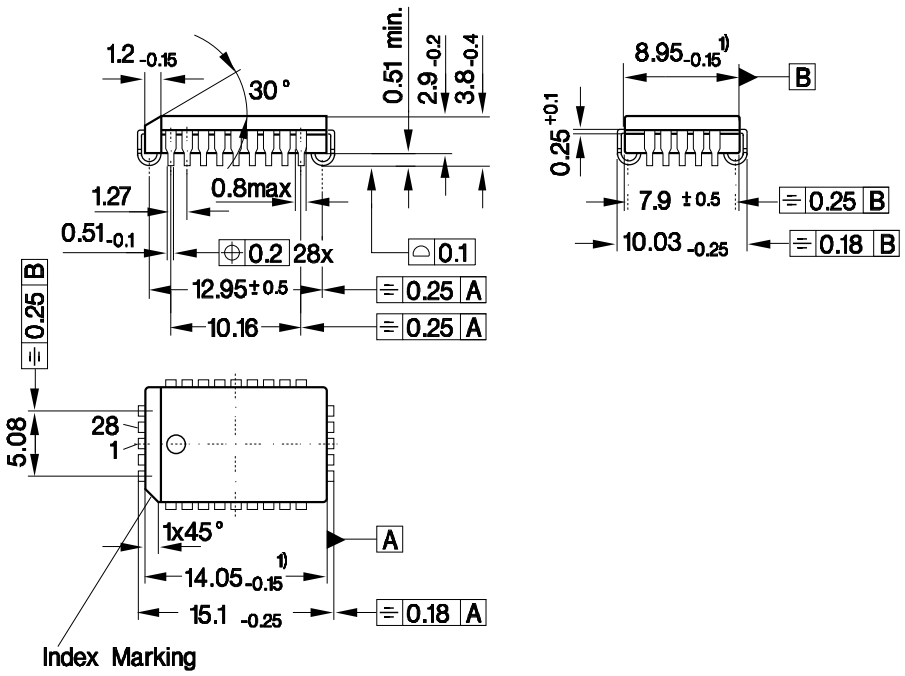


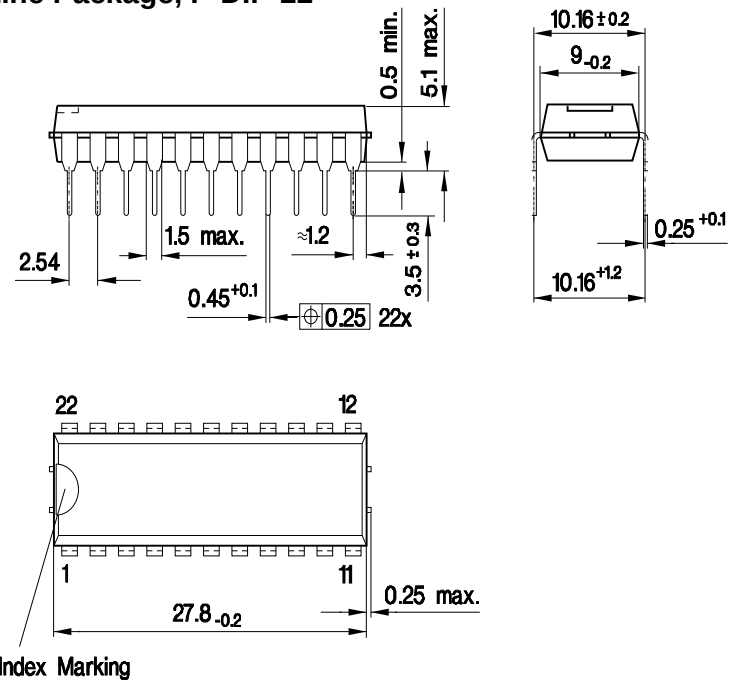
Figure 8
Protection against Overvoltages and Reverse Currents

Plastic Leaded Chip Carrier, P-LCC-28-R (SMD)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Plastic Dual In-Line Package, P-DIP-22



SMD = Surface Mounted Device

Dimension in mm