SIEMENS

ICs for Communications

Quadruple Transceiver for S/T Interface
QUAT-S

PEB 2084 Version 1.2

Data Sheet 07.95

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Ausgabe 07.95

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PEB 2084 **Revision History:**		**Current Version: Data Sheet 07.95**
Previous Releases:		Preliminary Technical Manual 2.94
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
11	10	Figure 1, IDO = Output and Input
9	12	Pin 40, IDO, resistor definition
20	22	Boundary scan, sequence of test pins (new)
29	33	Push-pull sensing
43	44	State diagram (DI $\rightarrow$ F3)
55	60	Maximum voltage on any pin
56	63	Power supply current

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1 Overview

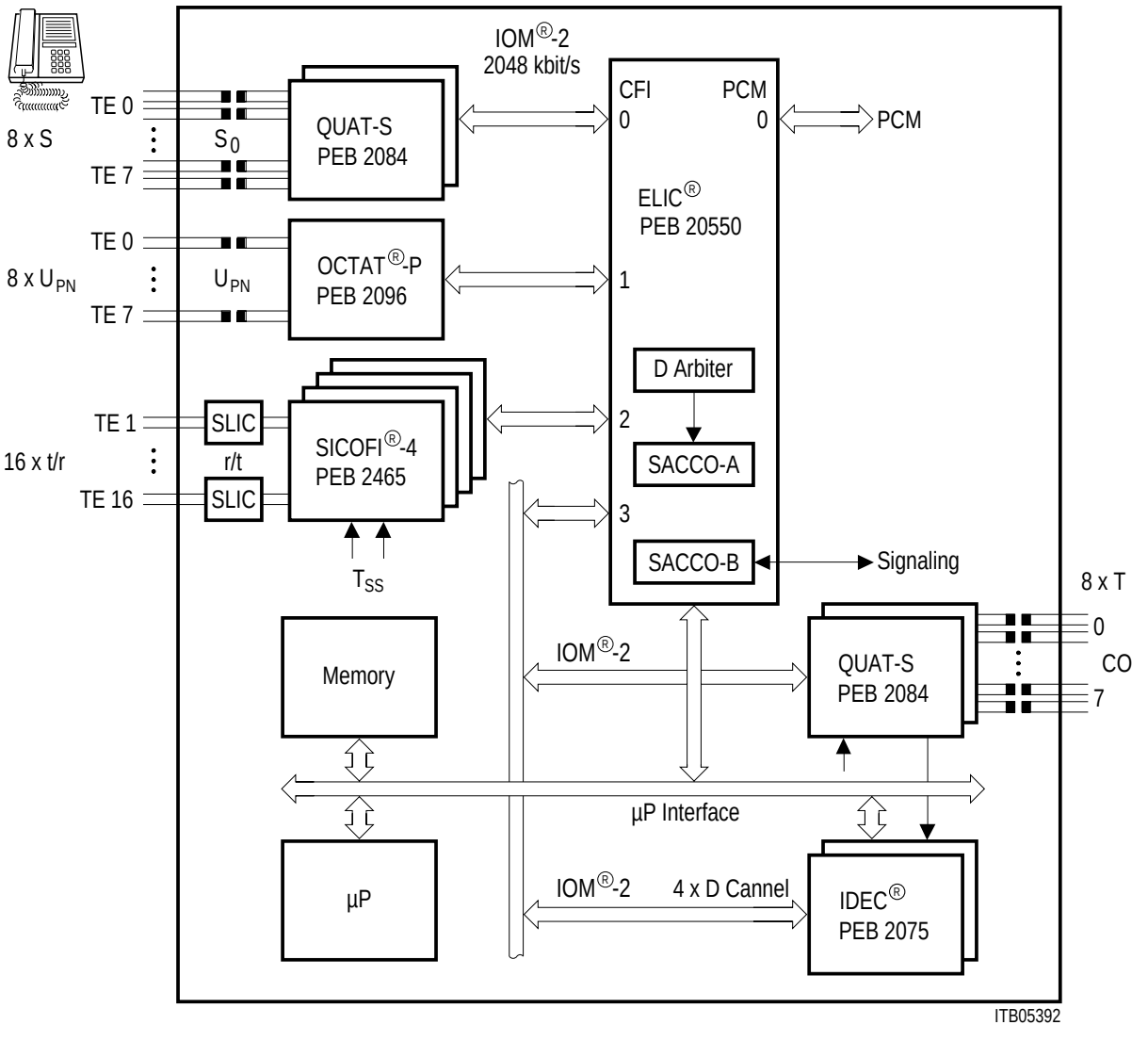
The PEB 2084, Quadruple Transceiver for S/T Interfaces (QUAT-S), implements four-wire S/T interfaces used to link voice/data digital terminals to PBX subscriber lines and PBX trunk lines to the public ISDN. The QUAT-S is an optimized device for PBX applications but can also be used in Hubs and Multiplexers. It can handle up to four S/T interfaces simultaneously. While each channel is independently useable as S or T interface.

The PEB 2084, QUAT-S, provides electrical and functional link between the analog S/T interface and the ISDN-Oriented Modular (IOM-2) interface. It handles the S/T interfaces fully according to CCITT I.430, ETSI 300.012, and ANSI T1.605 standards.

The PEB 2084, QUAT-S, is a CMOS device offered in a P-MQFP-44 package. It operates from a single 5 V power supply.

Other Siemens' integrated circuits for PBX applications are:

PEB 20550 Extended Line Card Interface Controller (ELIC)
PEB 2465 Signal-processing Codec Filter with 4 Channels (SICOFI-4)
PEB 2096 Octal Transceiver for U_{PN} Interfaces (OCTAT-P)
PEB 2075 ISDN D-Channel Controller (IDEC)



Example for an Integrated Analog / Digital PBX Application

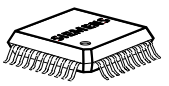
SIEMENS

Quadruple Transceiver for S/T Interface (QUAT-S)

PEB 2084

CMOS

1.1 Features



P-MQFP-44-2

- Four full duplex (B1 + B2 + D) S/T interface transceivers, each equipped with the following functions:
  - Analog S/T interfaces fully according to the CCITT I.430, ETSI 300.012 and ANSI T1.605 standards.
  - 192 kbit/s transmission rate
  - Receive timing recovery
  - Conversion between pseudo-ternary and binary codes
  - Conversion between S/T and IOM-2 frame structures
  - Activation / deactivation procedures, triggered by primitives received over the IOM-2 interface or by info received from the line (e.g. detection of INFO1)
  - Access to S and Q bits of S/T interface
  - Execution of test loops
  - Loop length up to 1.5 km (point-to-point)
  - Frame alignment in trunk applications with maximum wander of $\pm$ 50 µs
  - Logical S/T interface functions identical to PEB 2081, SBCX, for line card applications.
  - Analog S/T line transceivers identical to PEB 2081, SBCX.
- IOM-2 interface
- D-channel access control
- Support for JTAG boundary scan test
- 1µ CMOS technology with low power consumption
- + 5 V power supply
- P-MQFP-44 package

Type	Ordering Code	Package
PEB 2084 H	Q6701-H6481	P-MQFP-44-2 (SMD)

1.2 Logic Symbol

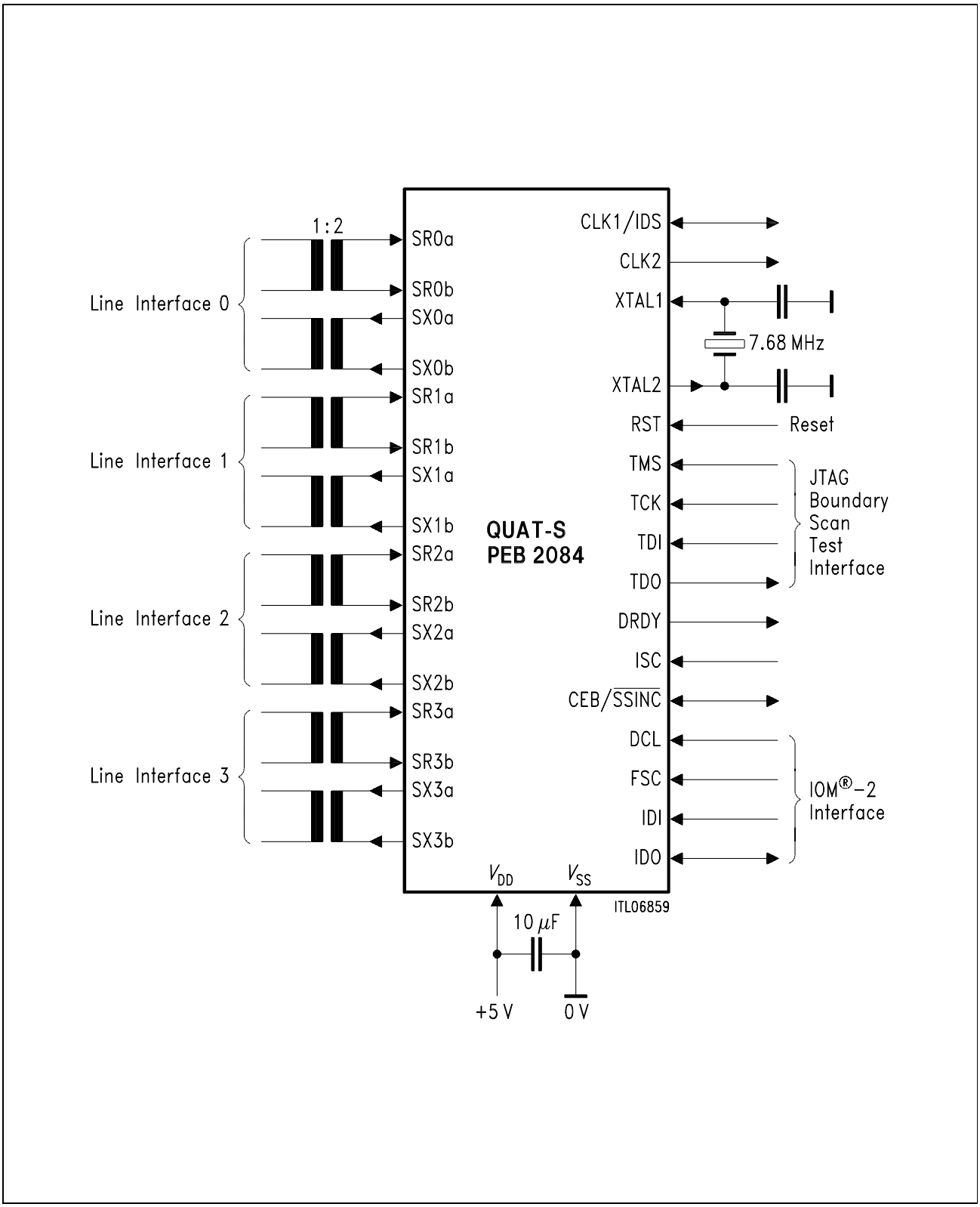
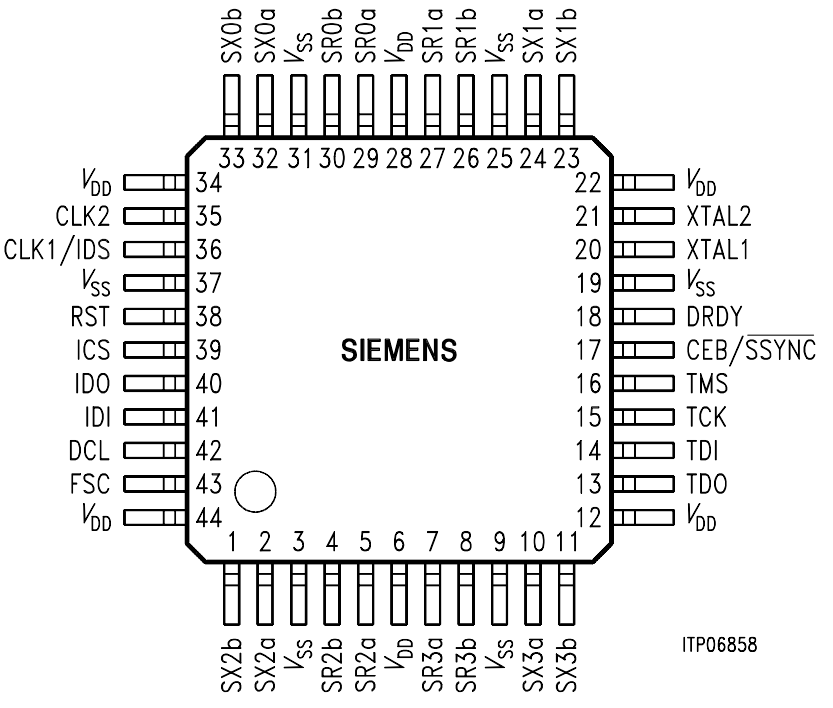


Figure 1
QUAT-S Logic Symbol

1.3 Pin Configuration

(top view)

P-MQFP-44-2



1.4 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
			S/T Interface a: positive, b: negative
29, 30	SR0a,b	I	No. 0: differential input
32, 33	SX0a,b	O	No. 0: differential output
27, 26	SR1a,b	I	No. 1: differential input
24, 23	SX1a,b	O	No. 1: differential output
5, 4	SR2a,b	I	No. 2: differential input
2, 1	SX2a,b	O	No. 2: differential output
7, 8	SR3a,b	I	No. 3: differential input
10, 11	SX3a,b	O	No. 3: differential output
			IOM®-2 Interface
43	FSC	I	Frame Synchronization Clock (8 kHz)
42	DCL	I	Data Clock
41	IDI	I	IOM Interface Data Input: Data Downstream in LT-S Data Upstream in LT-T
40	IDO	O/I	IOM Interface Data Output: Data Upstream in LT-S Data Downstream in LT-T Output open-drain: resistor to V_{DD} push-pull: resistor to V_{SS} resistor = 100 kΩ to 1 MΩ refer to push-pull sensing, **chapter 3.2**
39	ICS	I	IOM Interface Channel Select (pin-strapping) 0: channels 0 though 3 selected 1: channels 4 through 7 selected
			JTAG Boundary Scan Test Interface
16	TMS	I	Test Mode Select
15	TCK	I	Test Clock 6.25 MHz
14	TDI	I	Test Data Input
13	TDO	O	Test Data Output
20	XTAL1	I	Oscillator or 7.68 MHz clock input
21	XTAL2	O	Oscillator output

1.4 Pin Description (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
36	CLK1/ IDS	O/I	CLK1: Clock output 1.536 MHz synchronized to the trunk line (after reset in high impedance state, only activated by programming configuration register) IDS: IOM-Interface Data Rate Select during HW reset (pin-strapping) 0: double DCL (normal IOM-2 interface) 1: single DCL The value of the input is sampled by the falling edge of RST. Afterwards the pin may be used for CLK1 functions.
35	CLK2	O	7.68 MHz clock output
38	RST	I	Reset, active high
17	CEB / $\overline{\text{SSYNC}}$	I/O / I	CEB: Common echo bit for collision resolution in logical subscriber LT-S bus configurations (open drain output, external pull-up resistor required.) $\overline{\text{SSYNC}}$: Superframe synchronization input
18	DRDY	O	D-channel Ready signal to control HDLC hardware in LT-T mode (open-drain or push-pull operation identical to pin IDO)
6, 12, 22, 28, 34, 44	V_{DD}	I	+ 5 V power supply
3, 9, 19, 25, 31, 37	V_{SS}	I	Reference ground

2 Functional Description

The PEB 2084, QUAT-S, performs the layer-1 functions of the ISDN basic access for four S/T interfaces.

2.1 Device Architecture

The QUAT-S contains the following functional blocks: Refer to **figure 2**

- Four line transceivers with analog S/T interfaces
- One digital IOM-2 interface
- Frame structure converter between the IOM-2 interface and the S/T interfaces
- JTAG boundary scan test interface
- Clocking, reset and initialization block

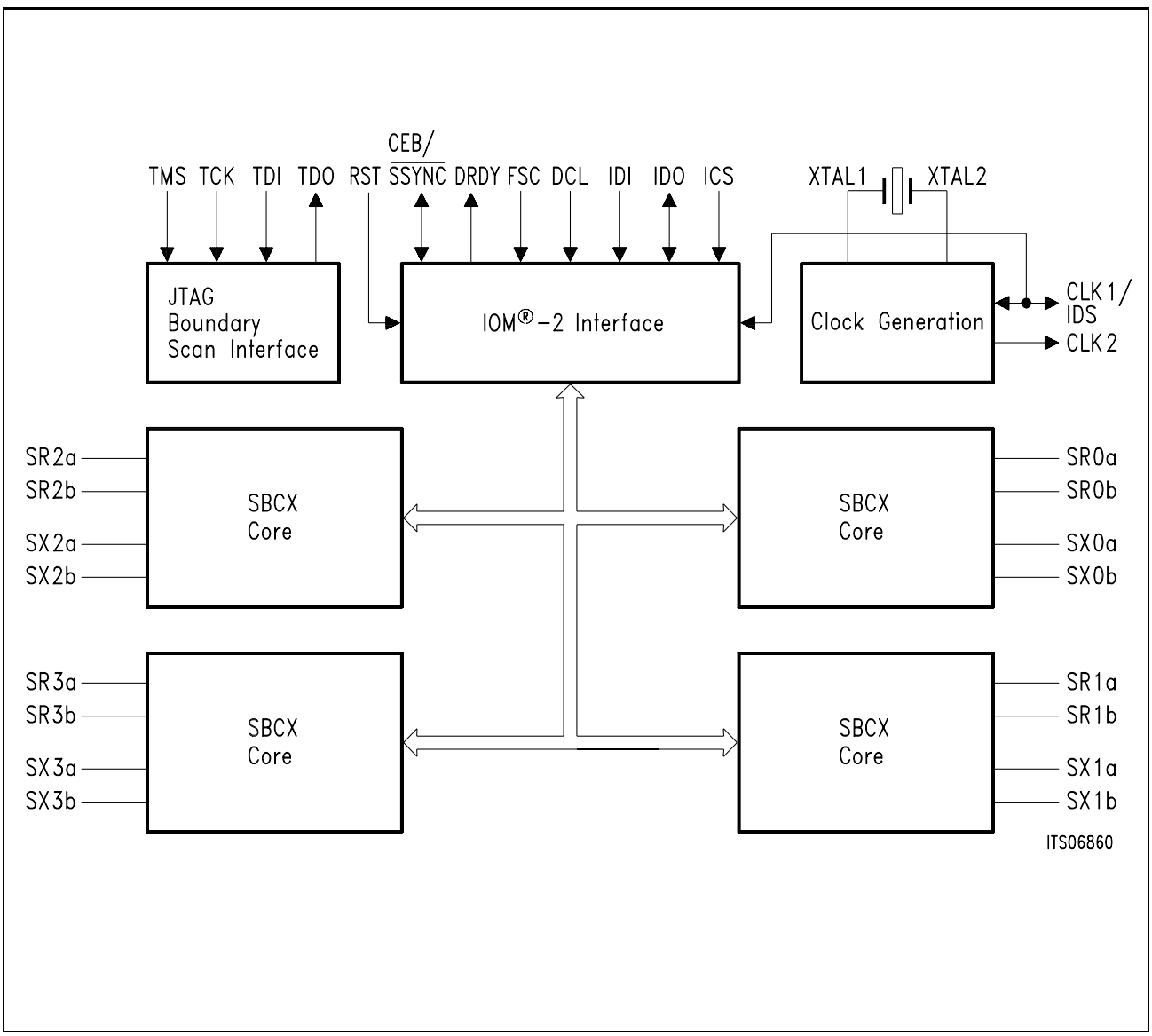


Figure 2
QUAT-S Device Architecture

2.2 Interfaces

PEB 2084, QUAT-S, provides four independent S/T interfaces, one IOM-2 interface and one JTAG boundary scan test interface.

2.2.1 S/T Interface

Frame Structure

One frame consists of 48 bits, at a nominal bit rate of 192 kbit/s. Thus each frame carries two octets of B1, two octets of B2 and 4 bits of D-channel, according to the B1+B2+D structure defined for the ISDN basic access (the total user data rate is 144 kbit/s). The beginning of the frame is marked with a F-bit using a code violation (no Mark inversion). The frame structures for data downstream (from network to subscriber) and for data upstream (from subscriber to network) are shown in **figure 3**.

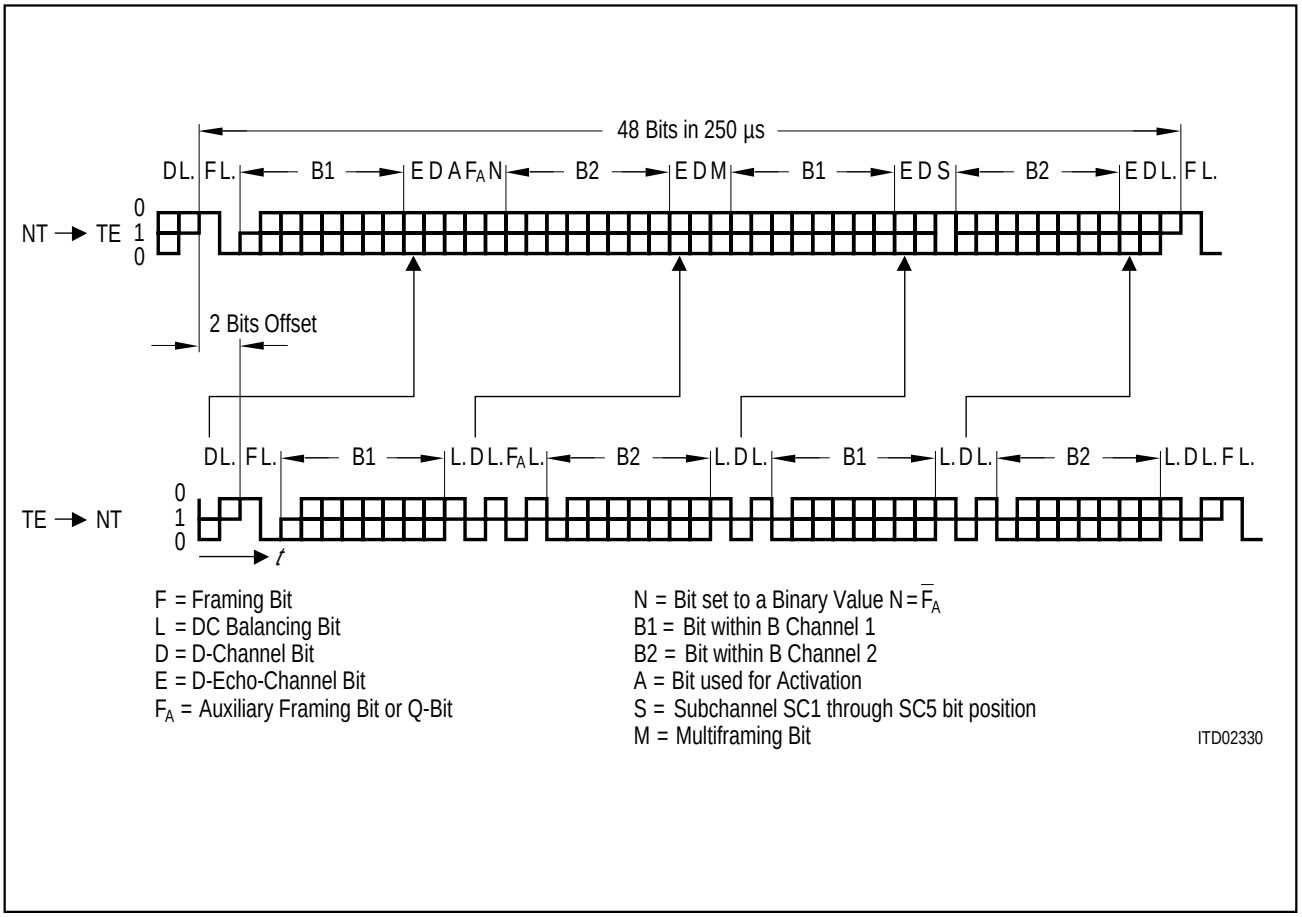


Figure 3
Frame Structure at Reference Points S and T (CCITT I.430)

The E-bit (= Echo bit to the D-channel bit) can be controlled via C/I channel and may be used to carry the “available” / “blocked” information sent by ELIC, PEB 20550. Refer to **chapter 3.3.3**.

Coding

The QUAT-S uses a pseudo-ternary coding technique on the S/T interface (with a 100% pulse width) according to CCITT I.430 recommendation. A binary ‘1’ corresponds to a neutral level (space = no current) on the S/T line, binary ‘0’s are coded as alternating positive and negative pulses (= marks), **figure 4**.

Code violation (CV) is caused by two successive pulses with the same polarity (= no mark inversion).

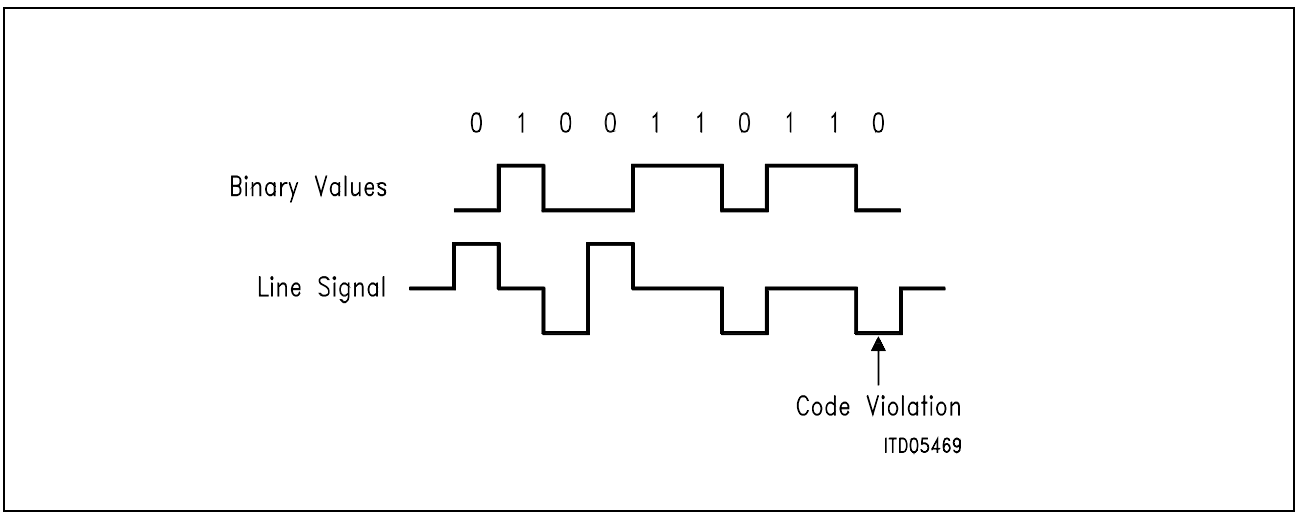


Figure 4
S/T Interface Line Code

For details refer to Technical Manual PEB 2081, SBCX.

Interface Configurations

The QUAT-S provides four S/T interfaces for different applications, see **figure 5**:

- Subscriber's connection to PBX (LT-S Mode) for different line configurations:
  - Point-to-point
  - Short passive bus
  - Extended passive bus
- PBX connection to CO trunk (LT-T Mode)

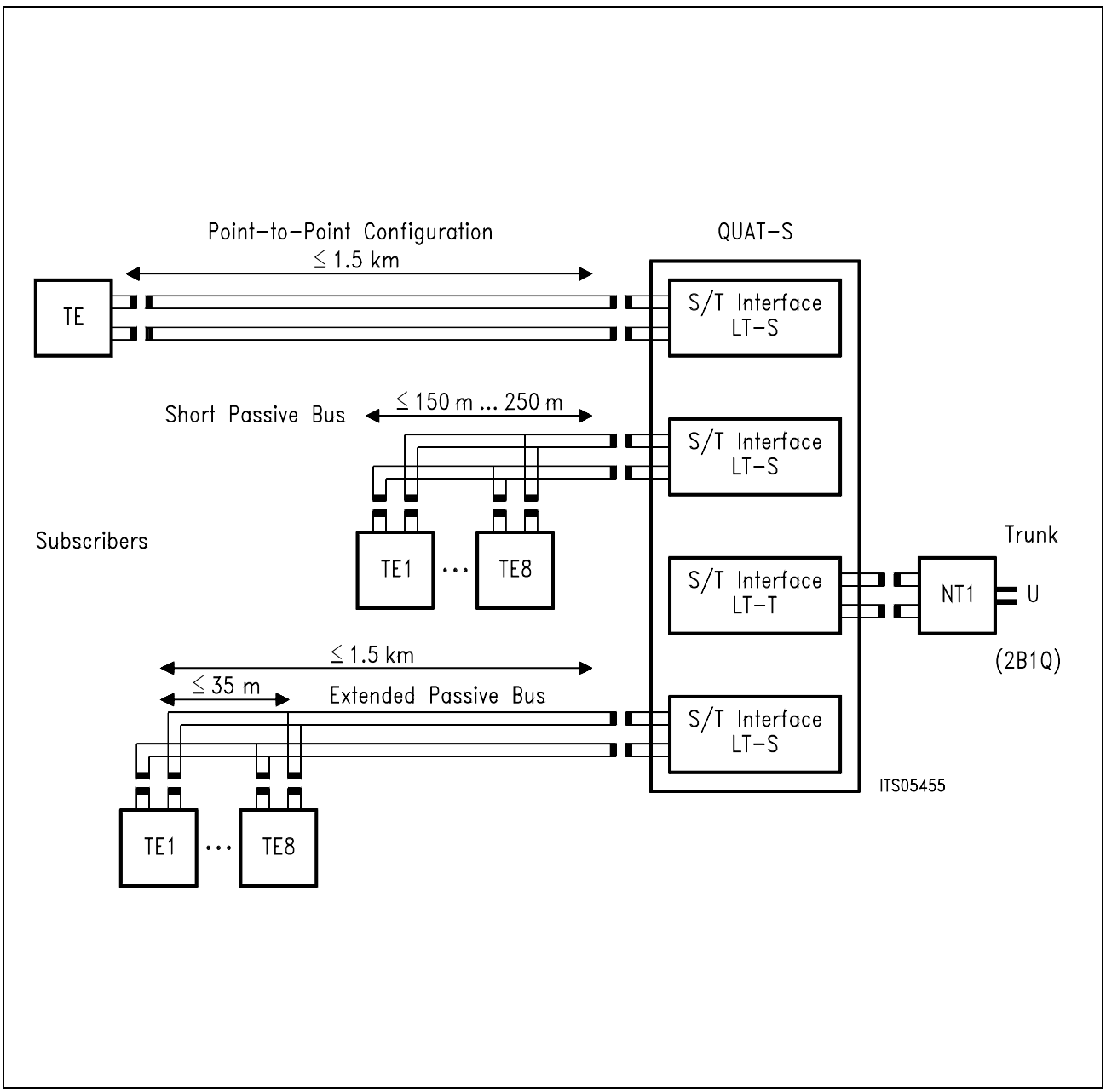


Figure 5
S/T Interface Configurations

The T interface is physically identical to the S interface.

2.2.2 IOM®-2 System Interface

The PEB 2084, QUAT-S, is equipped with a digital ISDN Oriented Modular (IOM-2) interface, for interconnection with other telecommunication ICs, such as IDEC (PEB 2075), EPIC (PEB 2055) and ELIC (PEB 20550). EPIC and ELIC represent the first switching stage towards the exchange system.

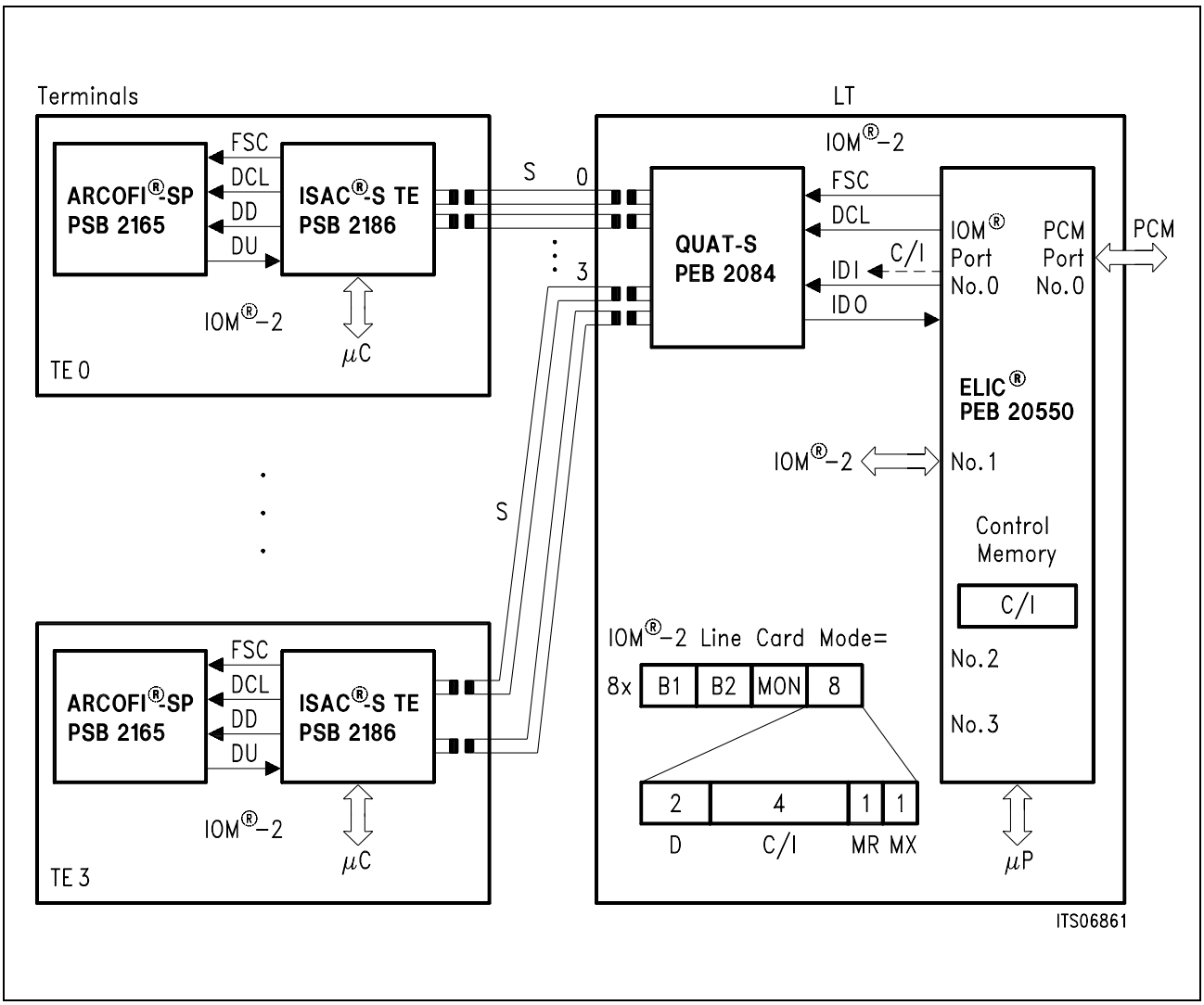


Figure 6
System Integration, IOM®-2 Interface

Interface Signals

The IOM-2 interface is a four-wire serial interface which comprises two data lines and two clock lines for synchronization. Refer to **figure 6**.

Data is carried over Data Upstream (DU) and Data Downstream (DD) lines. The downstream and upstream directions are always seen with respect to the exchange. Downstream refers to the information flow from the central exchange via PBX to the subscriber and upstream vice versa.

Thus, depending on the programmable QUAT-S mode, the data lines IDI and IDO get different meanings:

IDI	(IOM interface Data Input)	= Data Downstream	in LT-S
		= Data Upstream	in LT-T
IDO	(IOM-2 interface Data Output)	= Data Upstream	in LT-S
		= Data Downstream	in LT-T

The data is clocked by Data Clock (DCL) that operates at single or double data rate. The selection is done by pinstrapping (CLK1/IDS). The IOM frames are delimited by an 8 kHz Frame Synchronization Clock (FSC). The FSC rising edge indicates the start of an IOM-2 frame.

The IOM-2 interface specification describes open drain data lines with external pull-up resistors. However, if operation is logically point-to-point, tristate operation is possible as well.

Frame Structure

One IOM-2 frame typically contains 8 IOM channels (sub-frames). The ISDN user data rate is 144 kbit/s (B1 + B2 + D). The data is transmitted transparently synchronously and in phase in both directions over the IOM-2 interface using time division multiplexing within the 125 µs IOM-2 interface frame.

Refer to **figure 7**.

QUAT-S requires IOM-2 frame consisting of n complete ISDN channels (with 32 bits per channel); n = 4, 5, 6, … 16.

Nominal bit rate of data (IDI and IDO)	1024 kbit/s	… 4096 kbit/s
Nominal frequency of DCL	2048 kHz	… 8192 kHz
Selectable frequency of DCL	1024 kHz	… 4096 kHz
Nominal frequency of FSC	8 kHz	

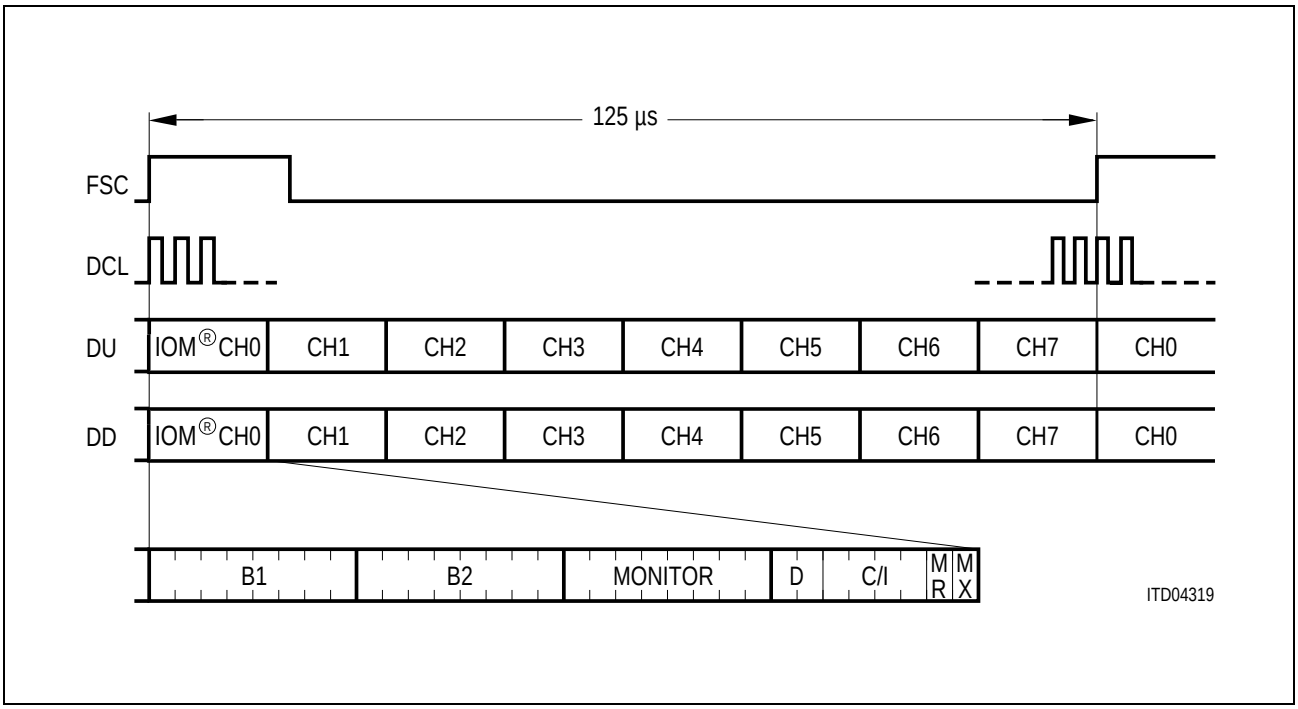


Figure 7
Multiplexed Frame Structure of the IOM-2 Interface in LT Mode with 2048 kbit/s Data Rate

Each IOM ISDN channel consists of a total of 32 bits, or four octets:
B1 (8 bits) + B2 (8 bits) + D (2 bits) plus 14 bits for intercommunication.

- Two 8-bit B1 and B2 channels for voice and data communication with a data rate of 64 kbit/s each,
- One 8-bit monitor channel for transferring maintenance information,
- One 2-bit D-channel for data transfer (e.g. signalling) with a data rate of 16 kbit/s
- Four command/indication (C/I) bits for controlling layer-1 functions.
- Two bits for handling the monitor channel: MR an MX (hand shake control).

8 bits	8 bits	8 bits	2	4 bits	1	1
B1 channel	B2 channel	Monitor channel	D ch.	Command/ Indication	MR	MX

The user data rate is 144 kbit/s (B1 + B2 + D).

Monitor Channels

The monitor channel is used to convey message oriented local functions such as software programming or access to internal registers via a layer-2 controller (ICC, ELIC,…). There is a defined handshake procedure between the monitor channel transmitter and the receiver in order to ensure a safe data transfer over the IOM-2 interface.

The monitor channel operates on an asynchronous basis. While data transfer on the bus takes place synchronized to the frame, the data flow is controlled by a handshake procedure using the monitor channel receive bit (MR) and the monitor channel transmit bit (MX). For example: data is placed onto the monitor channel and the MX bit is activated (active low). This data will be transmitted repeatedly once per 8 kHz frame until the transfer is acknowledged via the MR bit.

The monitor channel is in an idle condition when the MX bit is inactive in two or more consecutive frames (indication of End Of Message EOM).

The monitor channel is also used to convey S and Q maintenance bits information (S/Q channel).

The PEB 2084, QUAT-S, handles four monitor channels allocated to its four S/T interfaces. The implemented monitor protocol is according to the IOM Interface Specification, Rev. 2. For more details and an example refer to **chapter 3.3.2.**

D-Channels

The D-channels are switched transparently between the S/T interfaces and the IOM-2 interface. Depending on the data load on a line card, different PBX architectures can be implemented for D-channel handling in LT-S applications:

For decentral signalling, up to 32 subscribers can be served with only one special HDLC controller which is integrated in the PEB 20550, ELIC (SACCO-A).

For intensive data packet handling in LT-S mode (e.g. in PC networks) or in LT-T applications, additional HDLC controllers such as HSCX, IDEC, ESCC 2 or 8 or MUNICH 32 may be connected to the IOM-2 interface. If a D-channel collision resolution according to CCITT I.430 is required, the QUAT-S offers a strobe signal to control the connected HDLC (LAPD) controller.

For operational description refer to **chapter 3.3.3.**

C/I-Channels

A C/I-channel is used for communication between the PEB 2084, QUAT-S, and a processor via a layer-2 device, to control and monitor layer-1 functions (activation/deactivation and additional control functions). The layer-2 device monitors the layer-1 indication continuously and indicates a change if a new code is found to be valid in two consecutive IOM frames (double last look criterion).

The codes originated by layer-2 devices are called “Commands”, those originated by the PEB 2084, QUAT-S, are called “Indications”.

The PEB 2084, QUAT-S, handles four C/I-channels; one for each S/T transceiver.

For a list of the C/I codes and their use refer to **chapter 3.6**.

2.2.3 JTAG Boundary Scan Test Interface

The QUAT-S provides a boundary scan support for a cost effective board testing. It consists of:

- Complete boundary scan for 11 signals (pins) according to IEEE Std. 1149.1 specification
- Test access port controller (TAP)
- Four dedicated pins (TCK, TMS, TDI, TDO)
- One 32-bit IDCODE register
- Specific functions for SXna,b

Boundary Scan

The following QUAT-S pins are included in the boundary scan:
FSC, DCL, IDI, IDO, RST, ICS, CEB, DRDY, CLK1, CLK2 and XTAL1.

Depending on the pin functionality one or two boundary scan cells are provided.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	Input
Output	2	Output, enable

When the TAP controller is in the appropriate mode data is shifted into/ out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

The QUAT-S pins are included in the boundary scan in the following sequence:

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
1	43	FSC	I	1
2	42	DCL	I	1
3	41	IDI	I	1
4	40	IDO	O	2+1
5	39	ICS	I	1
6	38	RST	I	1
7	36	CLK1/IDS	O/I	2 + 1
8	35	CLK2	O	2
9	20	XTAL1	I	1
10	18	DRDY	O	2
11	17	CEB/$\overline{\text{SSYNC}}$	I/O	1 + 2

TAP Controller

The Test Access Port (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

Following the standard definition five instructions are executable.

TAP controller instructions:

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code
0100	Test Mode TM1	Single pulses (2 kHz) on SXna,b
0101	Test Mode TM2	Continuous pulses (96 kHz) on SXna,b
11XX	BYPASS	Bypass operation

Note: The instructions TM1 and TM2 require 7.68 MHz at XTAL1.

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state “update DR”, all output pins are updated with the falling edge of TCK. When it has entered state “capture DR” the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state “update DR”, all inputs are updated internally with the falling edge of TCK. When it has entered state “capture DR” the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

0001 (INTEST) is the default value of the instruction register.

SAMPLE / PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

Note: The input pin XTAL1 should not be evaluated.
The input frequency (7.68 MHz) is not synchronous to TCK (6.25 MHz) which may cause not predictable snap-shots on the pin XTAL1.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacture code (11 bits). The LSB is fixed to “1”.

Version	Device Code	Manufacture Code	Output
0001	0000 0000 0010 0000	0000 1000 001	1	→ TDO

Note: In the state “test logic reset” the code “0011” is loaded into the instruction code register.

Test Modes TM1 and TM2

Two different pulse types at the line interface SXna,b are selectable: 2 kHz single pulses or 96 kHz continuous pulses, **figure 8.**

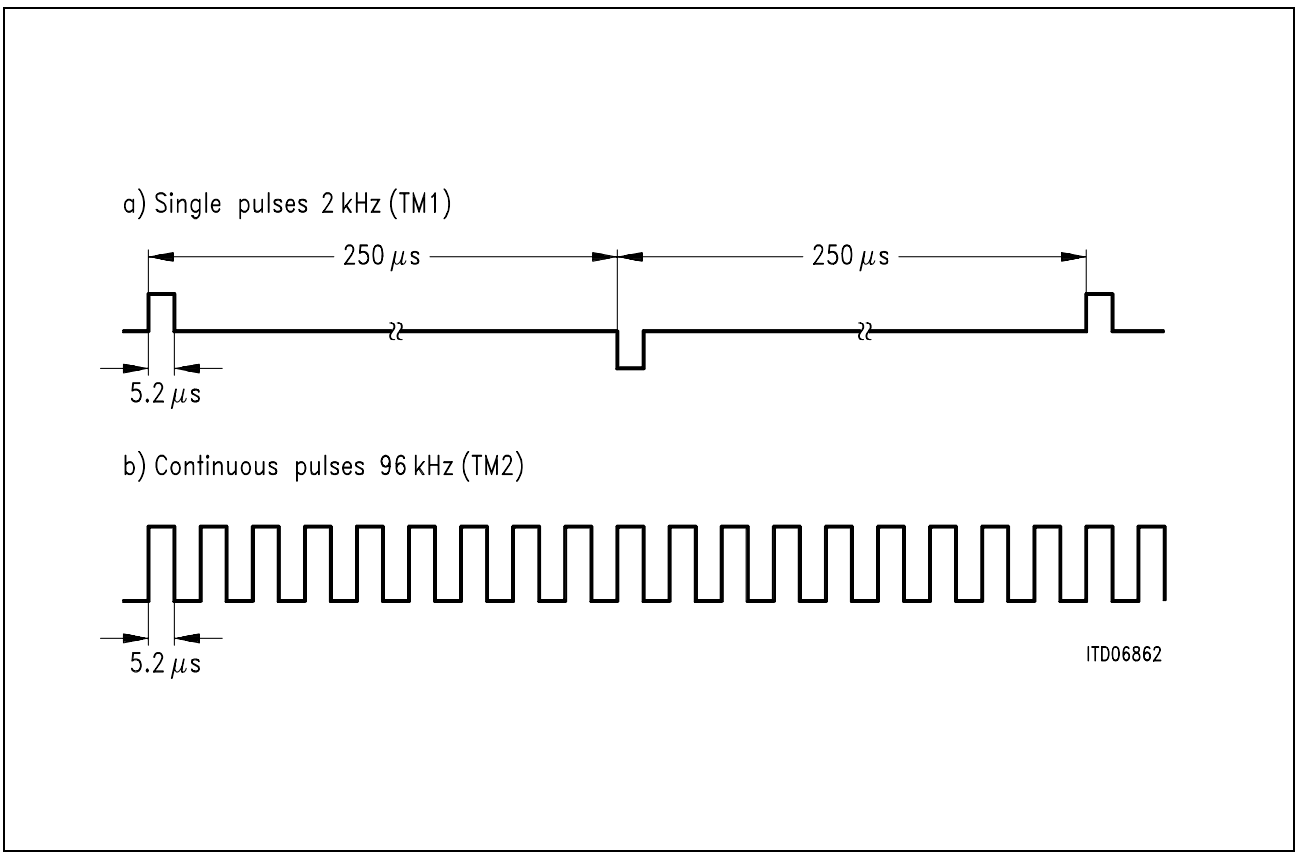


Figure 8
Test Pulse Wave Forms

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

2.3 Individual Functions

2.3.1 Transceiver, Analog Connections

The receiver input stages consist of a differential amplifier, followed by a peak detector and a set of comparators. Additional noise immunity is achieved by digital oversampling after the comparators, meaning that the sampling of the received bit is controlled digitally and dependent on the mode (CONFIGURATION Register).
The peak detector requires at most 2 µs to reach the peak value while storing the peak level for at least 250 µs. The data detection thresholds are chosen to 35 % of the peak voltage to increase the performance in extended passive bus configurations. However they are never lower than 85 mV. The level detector monitors the line input signals to detect whether an information is present. In LT-S analog loop-back mode the level detector monitors its own loop signal and an incoming signal is not recognized.

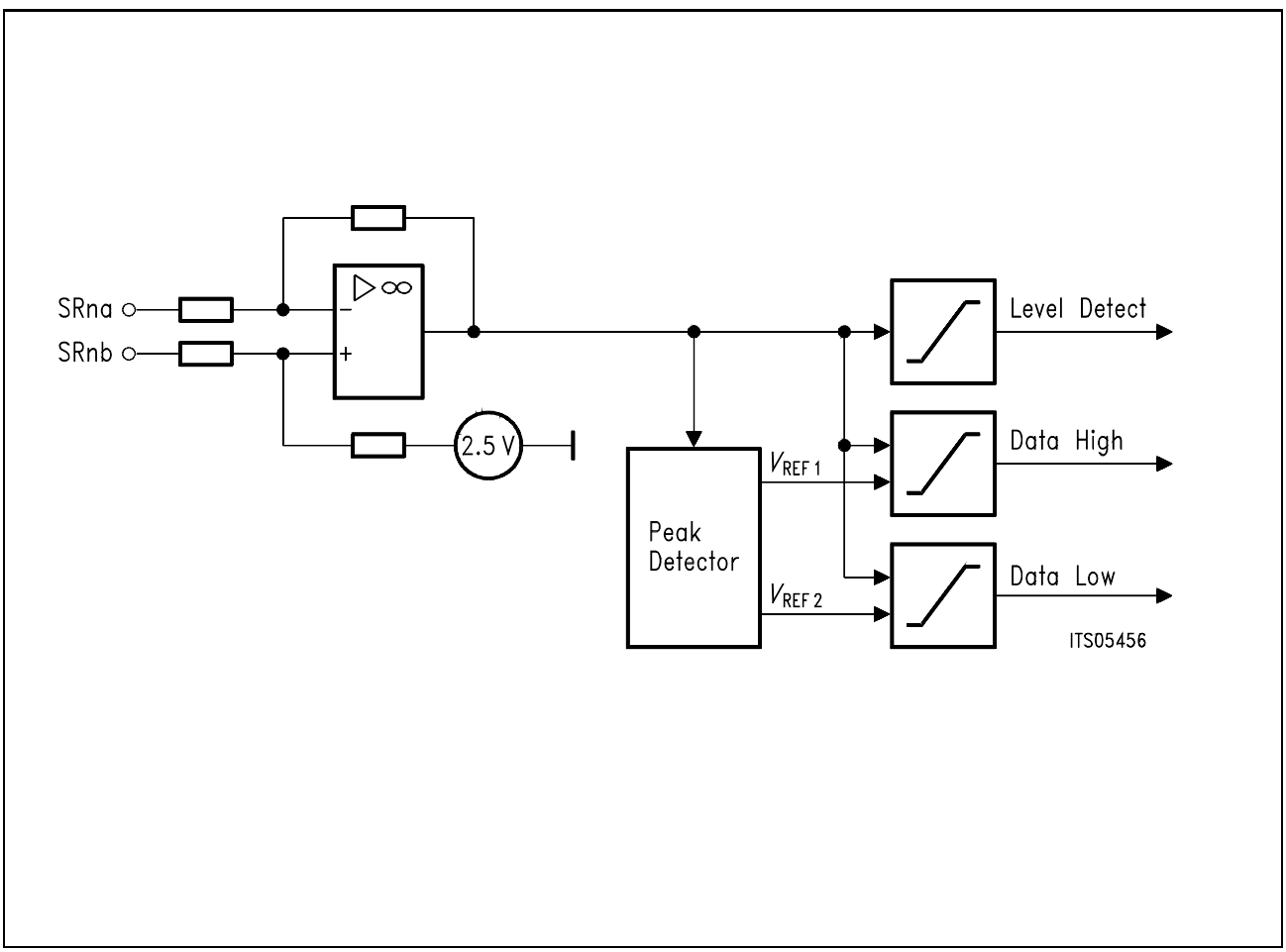


Figure 9
Receiver Functional Blocks

The transmitter stage consists of two identical current limited voltage sources, one for each polarity of output pulses, in order to achieve a ternary pulse shaping. A voltage of 2.1 V is delivered between SXna and SXnb, which yields a current of 7.5 mA over 280 Ω.

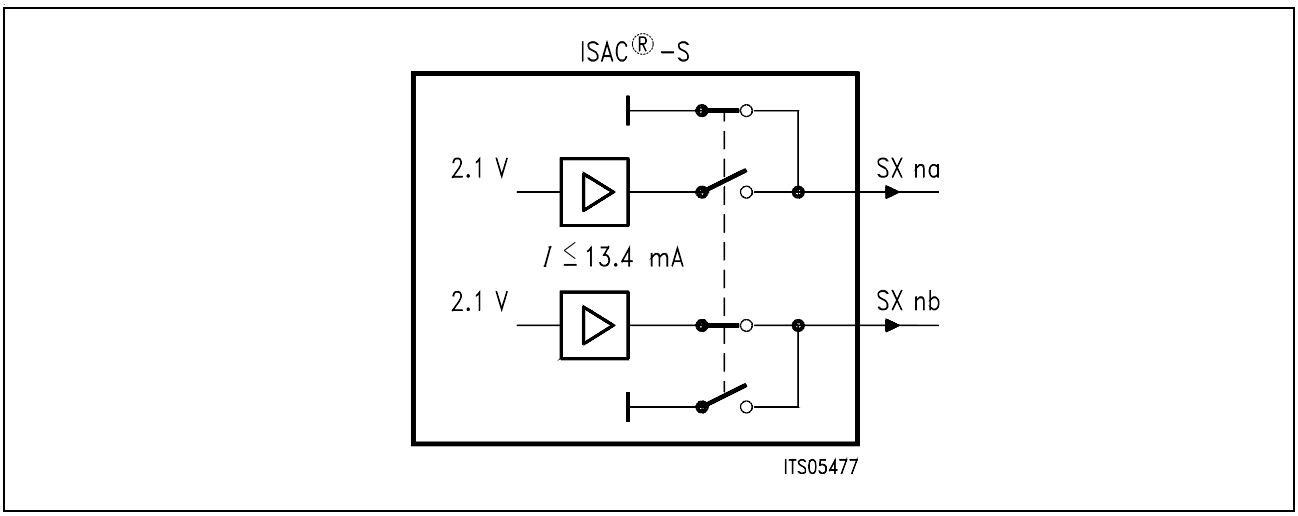


Figure 10
Transmitter Functional Block

External transformers of the ratio 2:1 are needed in receive and transmit directions to provide for isolation and transform voltage levels according to CCITT recommendations I.430. The QUAT-S also needs external circuitry for impedance matching, overvoltage protection and electromagnetic compatibility (EMC) for its connection to the 4-wire S/T interface.

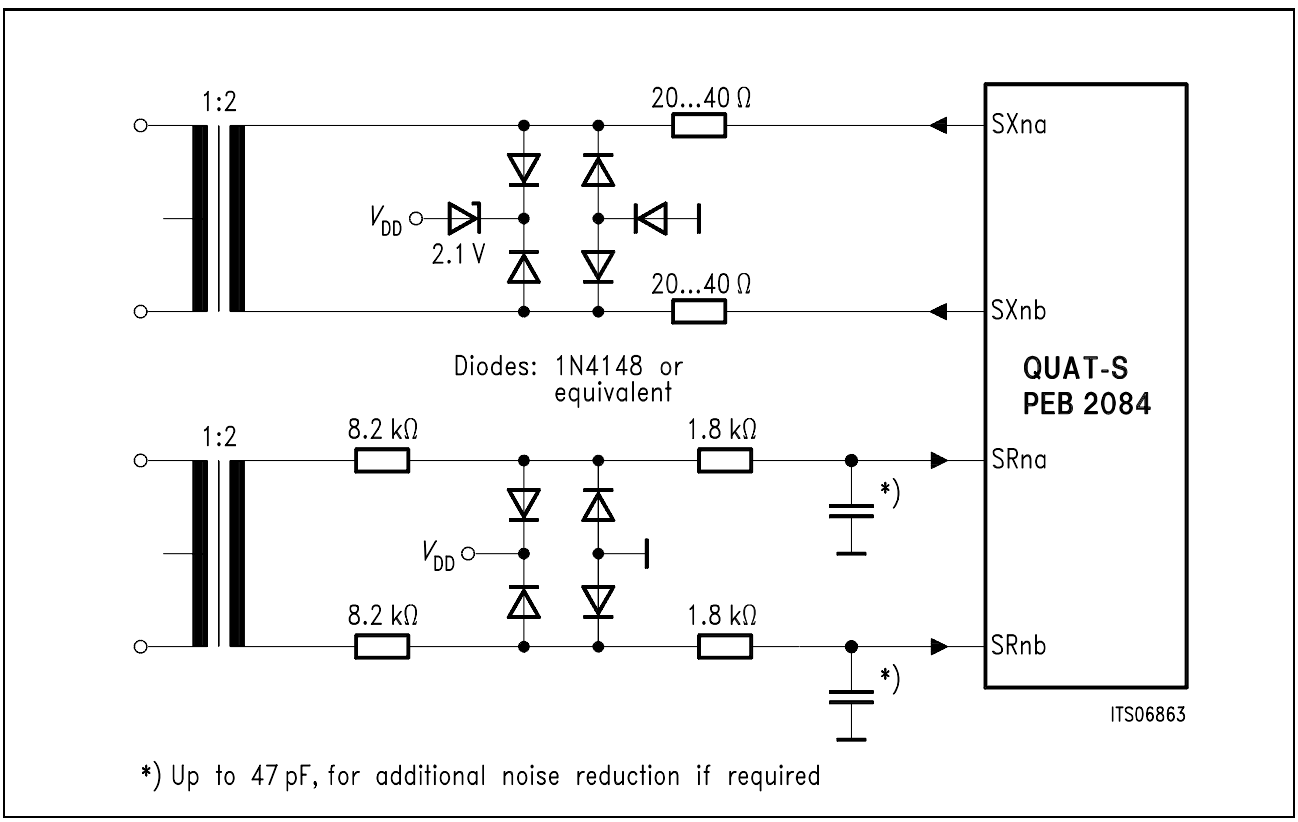


Figure 11
QUAT-S External Circuitry

Note: The actual values of the external resistors depend on the selected transformer.
The resistor values are optimal for an ideal transformer (R_{Cu} = 0).
Line termination (R_T) is applied to the last TE on the S bus only.

The transmitter of the QUAT-S is identical to that of SBCX, hence the line interface circuitry should be the same. The external resistors (20 … 40 Ω) are required in order to adjust the output voltage to the pulse mask (nominal 750 mV according to CCITT I.430) on the one hand and in order to meet the output impedance of a minimum of 20 Ω (transmission of a binary one according to CCITT I.430) on the other hand.
The QUAT-S has a symmetrical receiver.

Useful hints on how to design the external interface circuitry are contained in the application note “S/T interface circuitry using the PEB 2080, SBC, or PEB 2085, ISAC-S” from 12.89.

2.3.2 Timing Recovery

LT-S Mode (Configuration Register: Mode = 0)

In the LT-S mode the QUAT-S is the clock master to all connected TEs.

The transmit PLL (XPLL) synchronizes the 192 kHz transmit bit clock to the IOM-2 clock FSC (8 kHz) derived from the oscillator clock. When the oscillator clock is synchronous to FSC (fixed divider ratio of 960 from 7.68 MHz clock) the XPLL will not perform any tracking after having locked the phase, i.e. the input jitter on clocks XTAL and FSC will not be increased, **see figure 12.**

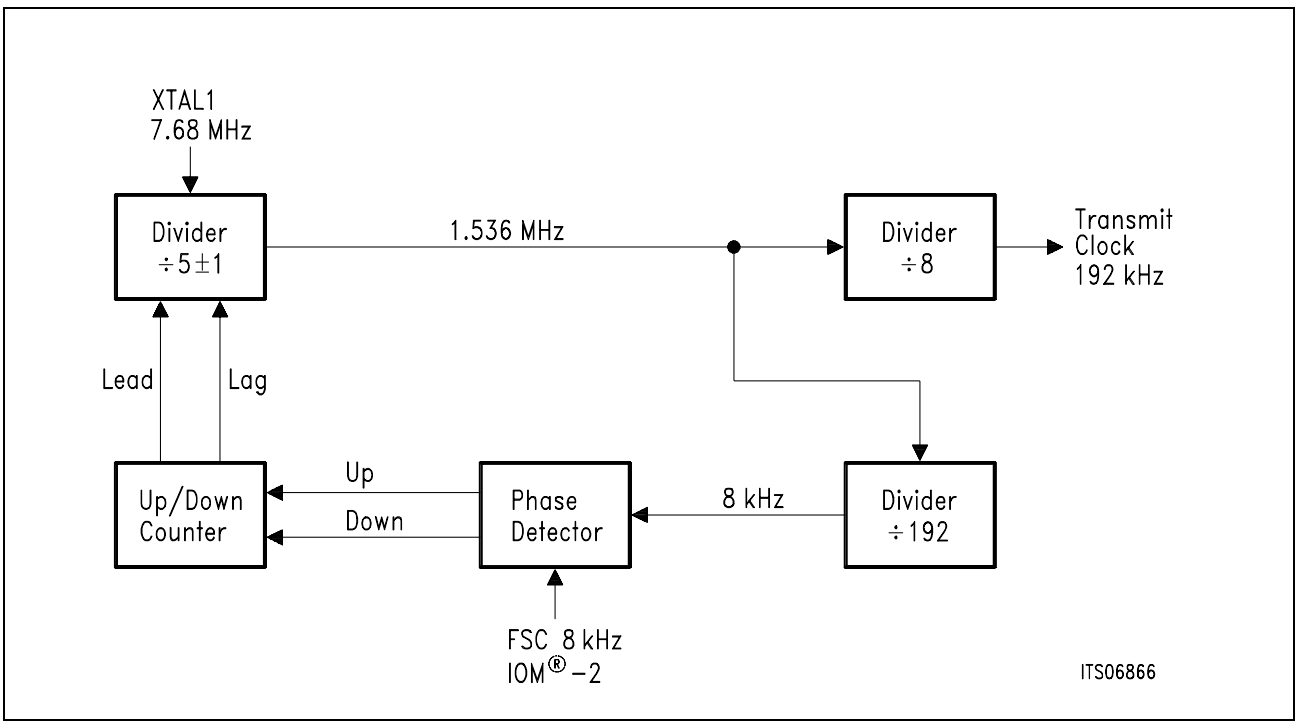


Figure 12
Block Diagram of XPLL

In the receive direction two cases have to be distinguished depending on the bus configuration:

– **Short passive bus configuration** (Configuration Register: C/W = 1)

The 192 kHz receive bit clock is identical to the transmit bit clock. The sampling instant for the receive bits is shifted by 4.6 µs with respect to the transmit bit clock. According to CCITT I.430 the receive frame shall be shifted (delayed) by two bits with respect to the transmit frame.

– **Point-to-point or extended passive bus configurations**
(Configuration Register: C/W = 0)

The 192 kHz receive bit clock is recovered (via PLL) from the receive data stream on the S interface. According to CCITT I.430 the receive frame can be shifted by 2 to 8 bits with respect to the transmit frame. However other shifts are allowed by the QUAT-S as well; including 0.

LT-T Mode (Configuration Register: Mode = 1)

In LT-T applications the QUAT-S is a clock slave to the central office clock, which is always the master. Thus a PBX clock system must be locked up with the CO clock system.

The 192 kHz receive bit clock is recovered (via PLL) from the receive data stream on the T interface.

2.3.3 Receive Signal Oversampling

The receive signal is sampled several times (oversampling) inside the receive clock period, and a majority logic is used to reduce the bit error rate in severe conditions.

As illustrated in **figure 13**, each received bit is sampled 29 times at 7.68 MHz clock intervals inside the estimated bit window. The samples obtained are compared against a threshold of 50 % with respect to the signal stored by the peak detector. If at least 16 samples have an amplitude exceeding the set threshold, a logical “0” is considered to be detected; otherwise a logical “1” (no signal) is considered to be detected.

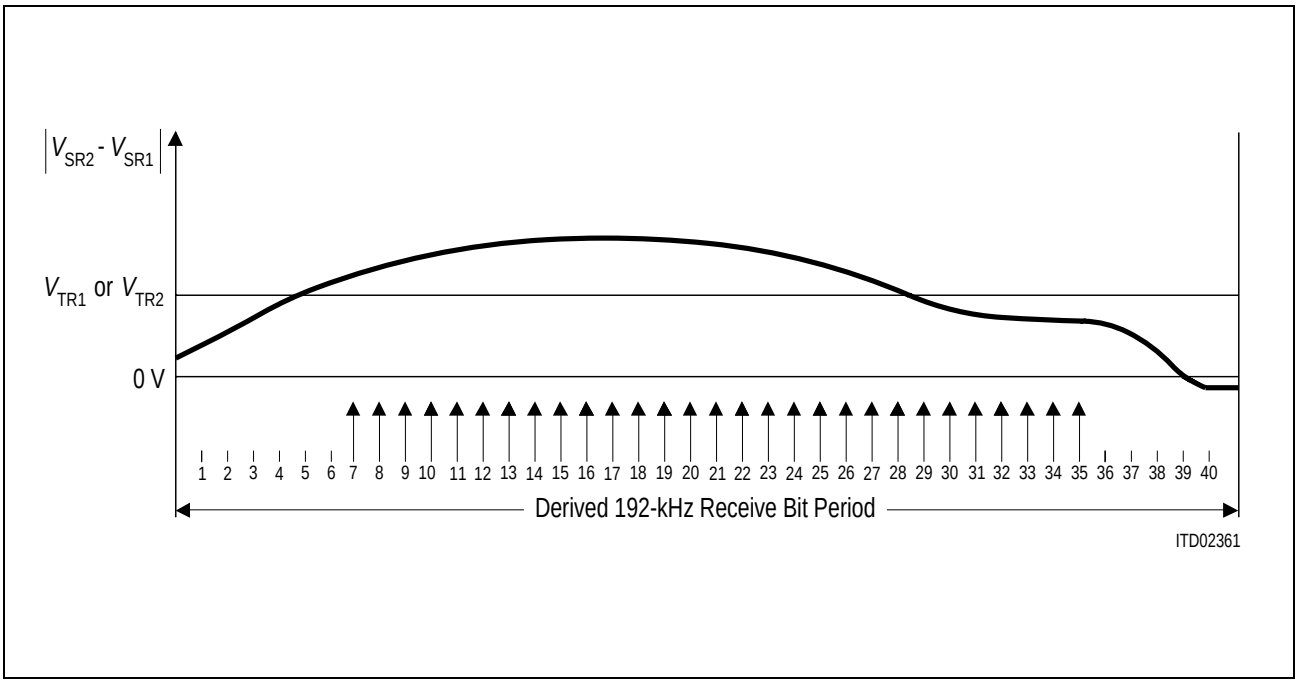


Figure 13
Receive Signal Oversampling on S and T Interfaces

The PLL also provides a synchronous 1.536 MHz clock (adaptive timing recovery), which can be used to synchronize the PCM clocks of the PEB 20550, ELIC, by means of a XTAL controlled PLL circuit. Refer to **figure 14.**

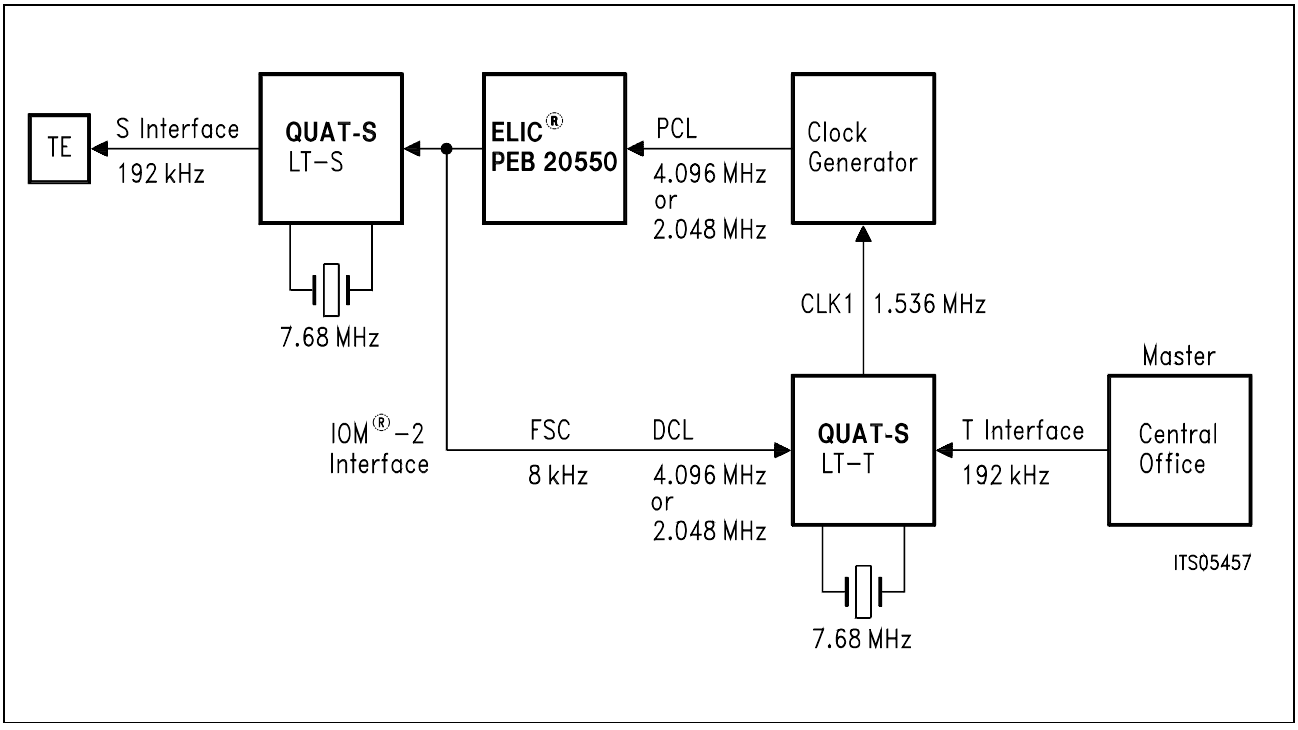


Figure 14
Clock System in LT-S and LT-T Modes

Since the ELIC generates the IOM-2 clocks (FSC, DCL) for all connected layer-1 and layer-2 devices, the loop is closed. If several layer-1 devices are operated in LT-T mode, only one device (one channel in a QUAT-S) may be selected (Configuration Register, bit RCLK) to deliver the reference clock.

The receive PLL performs tracking every 250 µs after detecting a phase difference between the F/L transition of the receive signal and the recovered clock. A phase adjustment is done by adding or subtracting 65 ns to or from the 1.536 MHz clock cycle.

Elastic Buffer

The two interfaces (IOM-2 and S/T) of the QUAT-S require a buffer to compensate for the differences in bit rate between the two interfaces as well as the different round trip delays of various wiring configurations. The QUAT-S enables intermediate storage of 3 × B1, 3 × B2 and 6 D-bits for phase difference and wander absorption.

Moreover, the buffer is designed as a wander-tolerant system, required in LT-T modes where the QUAT-S is a slave to both interfaces and the data clocks of the two interfaces have a time dependent phase relationship. The elastic buffer of the QUAT-S compensates for a maximum phase wander of 50 µs peak-to-peak and a slip detector indicates when this limit is exceeded. Setting the C/W-bit in the Configuration Register gives a warning when a slip of 25 µs is exceeded. An indication (Slip detected) is released in the C/I channel. However the data may be lost.

The phase relationship between the IOM-2 interface and the S/T interface is arbitrary in this case.

The transmit frame is shifted (delayed) by two bits with respect to the receive frame.

2.3.4 Activation / Deactivation

An incorporated finite state machine controls the activation and deactivation procedures and communicates with the layer-2 unit via the IOM-2 C/I channel. Each of the four C/I channels is allocated to its corresponding S/T line interface. Refer to **chapter 3.6.**

2.3.5 S/T Interface Frame Structures Synchronization

The QUAT-S supports two different kinds of frame structures:

a) A Multi-Frame consisting of 20 consecutive S/T frames.
b) A Super-Frame consisting of 2 × n (n = 1, 2, …) consecutive S/T frames.

Both frames provide an extra layer-1 capacity for information transmission in both application modes: LT-T and LT-S (refer to **chapter 3.6**, access to S and Q channels).

2.3.5.1 Multi-Frame Generation with a short FSC

The QUAT-S synchronizes to a multi-frame structure according to CCITT recommendation I.430.

In **LT-S** application mode the S interface multi-frame (20 × 250 µs = 5 ms period) can be generated by a master device (e.g. ELIC) by inserting a short FSC pulse.

An external strobe on the pin CEB/$\overline{\text{SSYNC}}$ can be used for simple terminal synchronization.

A short FSC pulse has a width of one DCL clock whereas a normal FSC pulse has a width of at least two DCL clocks. The QUAT-S samples the FSC input with the second falling edge of DCL clock in the very first bit positions of the frame. If the sampled bit is zero the S/T interface transmit frame, including multi-frame, is reset.

The frame relationship between IOM-2 interface (FSC) and S/T interface is shown in the following figures.

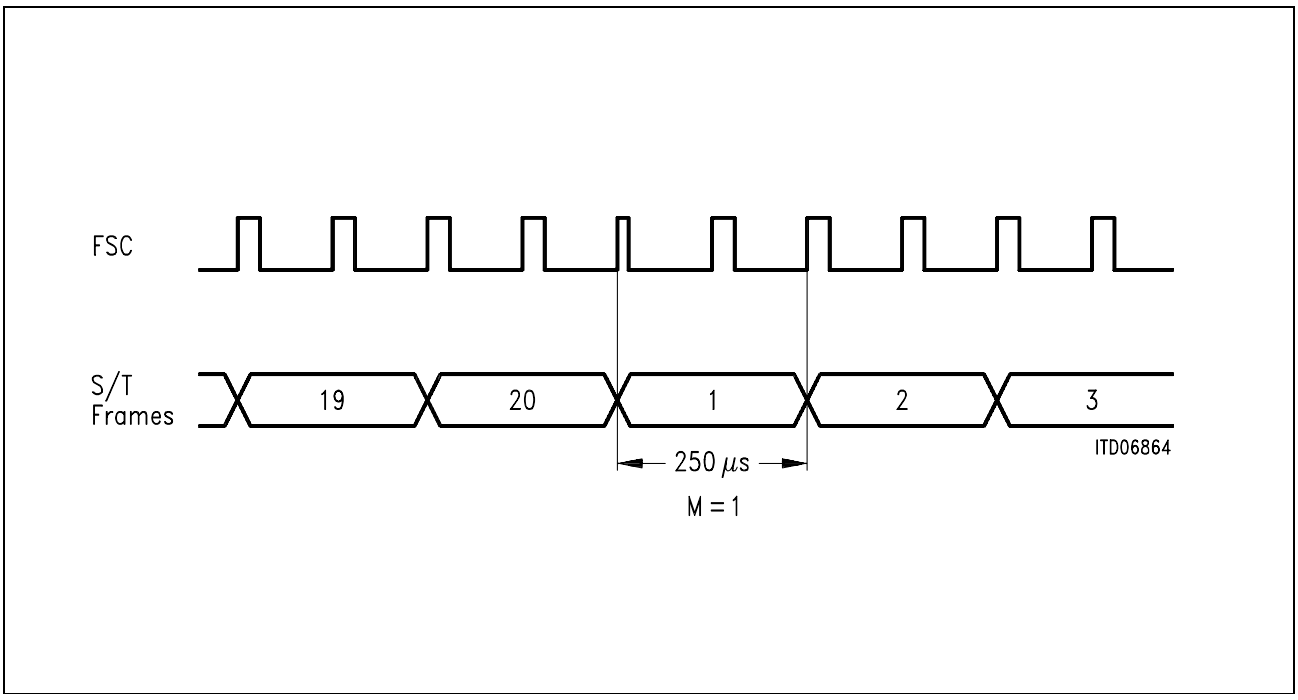


Figure 15
Multi-Frame Generation with a Short FSC

2.3.5.2 Super-Frame (M-bit) Generation using $\overline{\text{SSYNC}}$ (for DECT)

A zero pulse on the $\overline{\text{SSYNC}}$ input pin forces the QUAT-S to send M = 1 synchronously on all four S/T interfaces. (Useful with MFD = 1 only.)

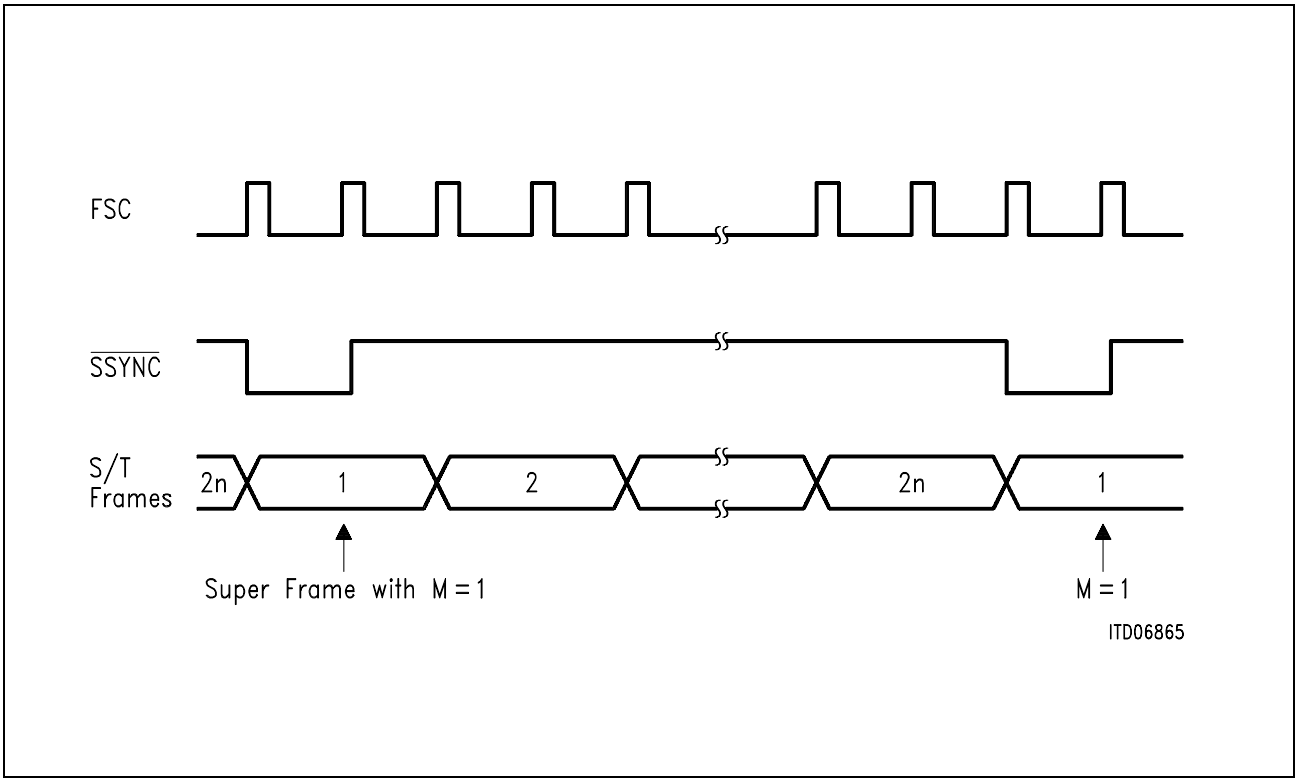


Figure 16
M-bit Generation Using $\overline{\text{SSYNC}}$

In **LT-T mode** the QUAT-S synchronizes to the received F_A-bit inversions and M-bits. When the synchronization is not achieved or lost, it mirrors the received F_A-bits.

Multi-frame synchronization is achieved after two complete multi-frames have been detected with reference to F_A/N-bit and M-bit positions. Multi-frame synchronization is lost after two or more bit errors in F_A/N-bit and M-bit positions have been detected in consequence, i.e. without a complete valid multi-frame in between.

The multi-frame synchronization can be disabled by programming the Configuration Register:
MFD = 1.

3 Operational Description

All procedures required for data transmission over the S/T interface are implemented. These comprise the S/T interface frame and multiframe synchronization, activation/deactivation procedure, and timing requirements such as bit rate and jitter. For a correct functionality of the QUAT-S the following operational precautions must be taken:

3.1 Reset

At power up, a reset pulse (RST) should be applied to bring the line interfaces of the PEB 2084, QUAT-S, to the state “reset”. No clocks are required during that procedure.

After that the PEB 2084, QUAT-S, may be operated according to the state diagram, each line interface controlled via the corresponding C/I channel.

3.2 Push – Pull Sensing on Pin IDO

The QUAT-S senses whether an external pull-up resistor (100 kΩ to 1 MΩ) is connected to the pin IDO. The sensing is done after reset within the following two IOM frames in the monitor channel.

The pin is pulled low for one bit and then switched to tristate. If the voltage level at IDP0 rises in the next bit to “High”, QUAT-S interprets this behaviour as an external pull up being connected to the pin and remains as open collector. If the level stays at “Low” QUAT-S switches to push-pull. However, actions of other device on this line or crosstalk from other lines during the sensing procedure may falsify the result. (A pull down resistor of 100 kΩ to 1 MΩ may improve the correctness of the sensing). This feature is useful if multiple transmitters are connected to the same IOM-2 interface, e.g. QUAT-S with an IDEC.

3.3 IOM®-2 Interface

3.3.1 ISDN Channels Allocation

The allocation between S/T line interfaces and the IOM-2 ISDN channels is according to their numbers with an offset of four or zero. The offset can be selected via pin ICS by pin strapping, i.e.
for ICS = 0 the SRX0a,b is allocated to IOM channel 0, and so on,
for ICS = 1 the SRX0a,b is allocated to IOM channel 4, and so on.

For detailed electrical definition refer to the **chapter 5** and the IOM Interface Specification, Rev. 2.

As described in **chapter 2.2.2**, each basic ISDN channel consists of five different communication channels: two voice channels, one monitor channel (incl. MR and MX bits), one D-channel and one command/indication (C/I) channel.

3.3.2 Monitor Channel

Before starting a data transmission to the QUAT-S, a microprocessor must verify that the transmitter of the QUAT-S is inactive, i.e. that a previous transmission has been terminated.

The QUAT-S has a monitor transmitter time out function of minimum 4 ms implemented. This prevents the monitor message to be transmitted continuously if the monitor data won't be acknowledged by the receiver.

First the Identification Register of the QUAT-S may be read. Two bytes are transmitted to the QUAT-S and as a result of the read operation two bytes are returned to the controller. In case of a write operation the data is only acknowledged and no data is returned from the QUAT-S to the controller.

The first byte of the data transmitted to the QUAT-S always indicates the type of the desired monitor operation (i.e. read or write to the internal registers).

The example shows the typical register access of the ELIC and gives a feeling about the important bits.

The ELIC uses a 16-Byte FIFO for transmission and reception of the monitor data. Therefore the user doesn't need to provide routines for the handshake protocol.

An example for a communication between a µP, an ELIC and the QUAT-S is shown in **figures 17 and 18.**

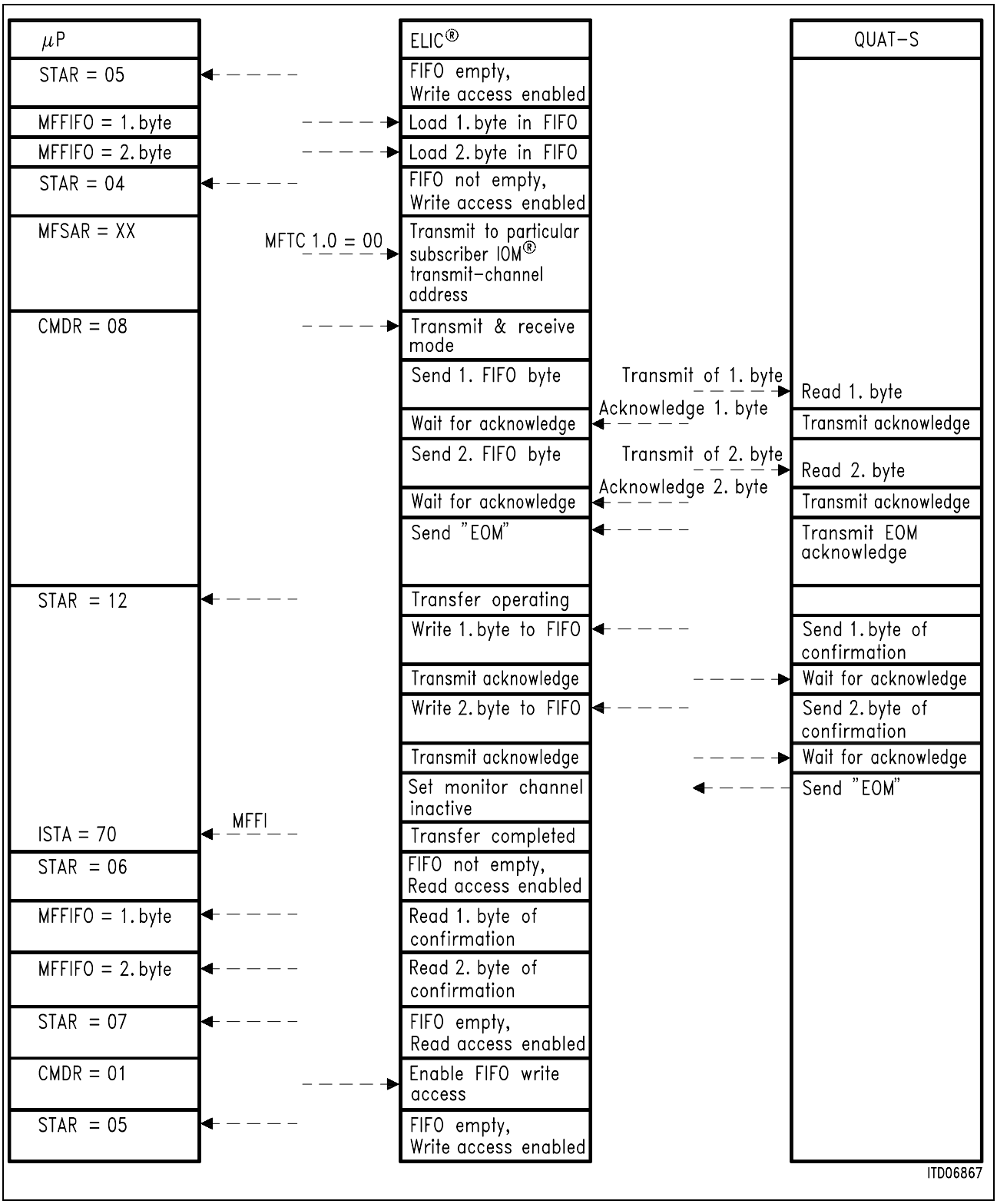


Figure 17
Monitor Channel Handling: µP ↔ ELIC ↔ QUAT-S

A detailed description of the hand-shake procedure using MX and MR bits is shown in **figure 18.**

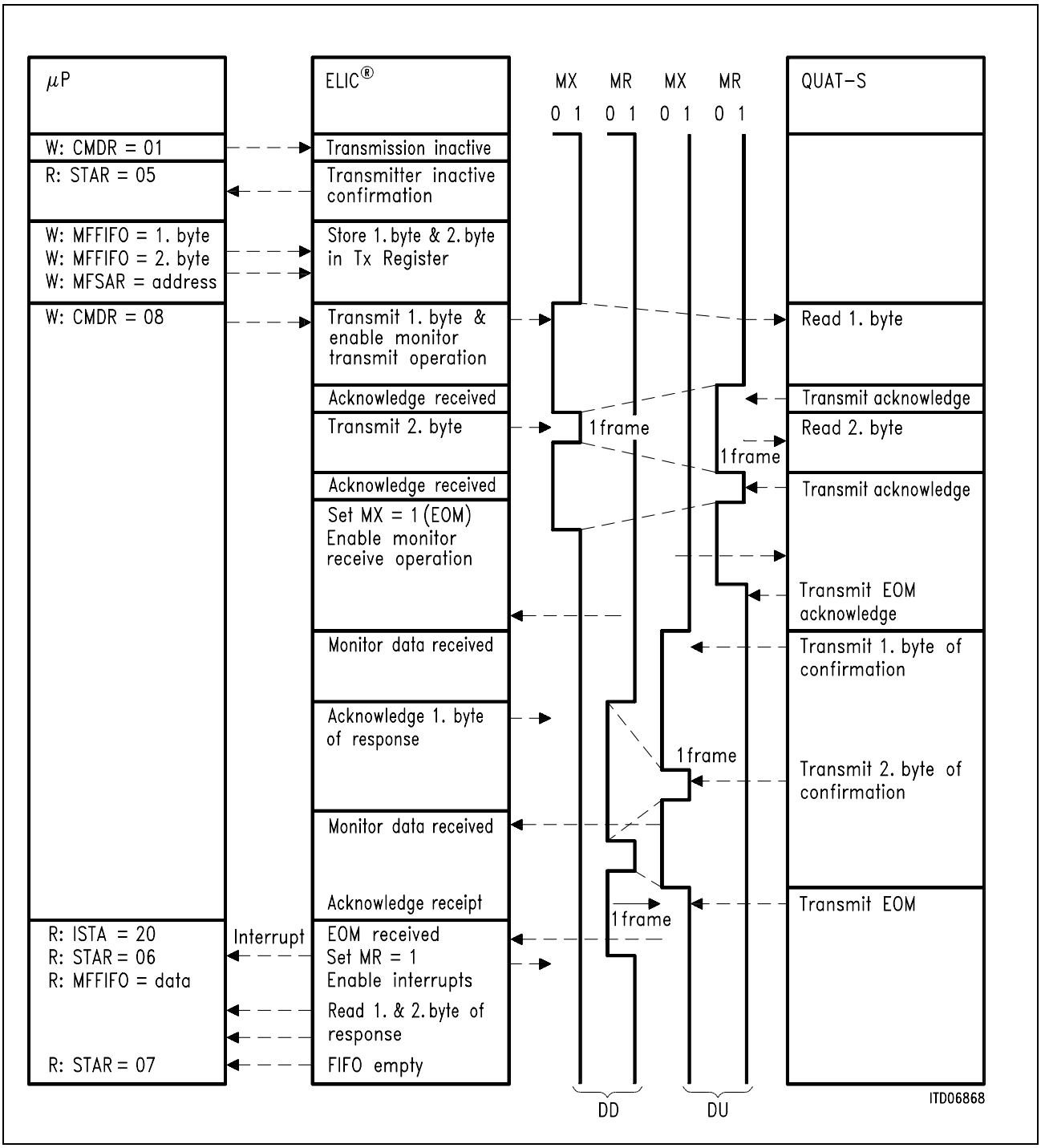


Figure 18
Monitor Channel Handling: Hand-shake by the Use of MX and MR Bits (LT-S Mode)

QUAT-S in LT-S Mode	Data Downstream:	MX-bit at ELIC → MR-bit at QUAT-S
	Data Upstream:	MX-bit at QUAT-S → MR-bit at ELIC
QUAT-S in LT-T Mode	Data Downstream:	MX-bit at QUAT-S → MR-bit at ELIC
	Data Upstream:	MX-bit at ELIC → MR-bit at QUAT-S

3.3.3 D-Channel Handling

Decentral D-channel handling in a PBX depends on QUAT-S application mode: LT-S or LT-T.

LT-S Mode. Configuration Register, MODE = 0.

It is used in PBX applications with only one signalling controller (HDLC) used for up to 32 ISDN subscribers in order to minimize system costs. A terminal is allowed to send data only if the signalling controller is ready to receive data. The D-channel access can be controlled via a central D-channel arbiter unit integrated in the PEB 20550, ELIC, or according to CCITT I.430 via an arbitration logic in the QUAT-S.

D-Channel Arbitration via ELIC. Auxiliary Register, DCM(1:0) = 11.

ELIC, PEB 20550, informs the QUAT-S whether the signalling controller (SACCO-A) is ready to receive data. It sends commands (C/I) to individual QUAT-S channels:

C/I = $\overline{1100}_H$ (e.g. 1000_H) indicates that the D-channel is “available” and can be used.

C/I = 1100_H indicates that the D-channel currently can not be used (is “blocked”) as the signalling controller is allocated to an other terminal.

The QUAT-S controls the connected terminal transmitters (e.g. ISAC-S, SBCX, ISAC-S TE) via its S interfaces accordingly. It translates the information “available” or “blocked” by setting the E-bit on the S interface.

E = D indicates to the terminal that its HDLC controller can send data.

E = $\overline{D}$ indicates that the HDLC controller may not send data or has to abort sending data.

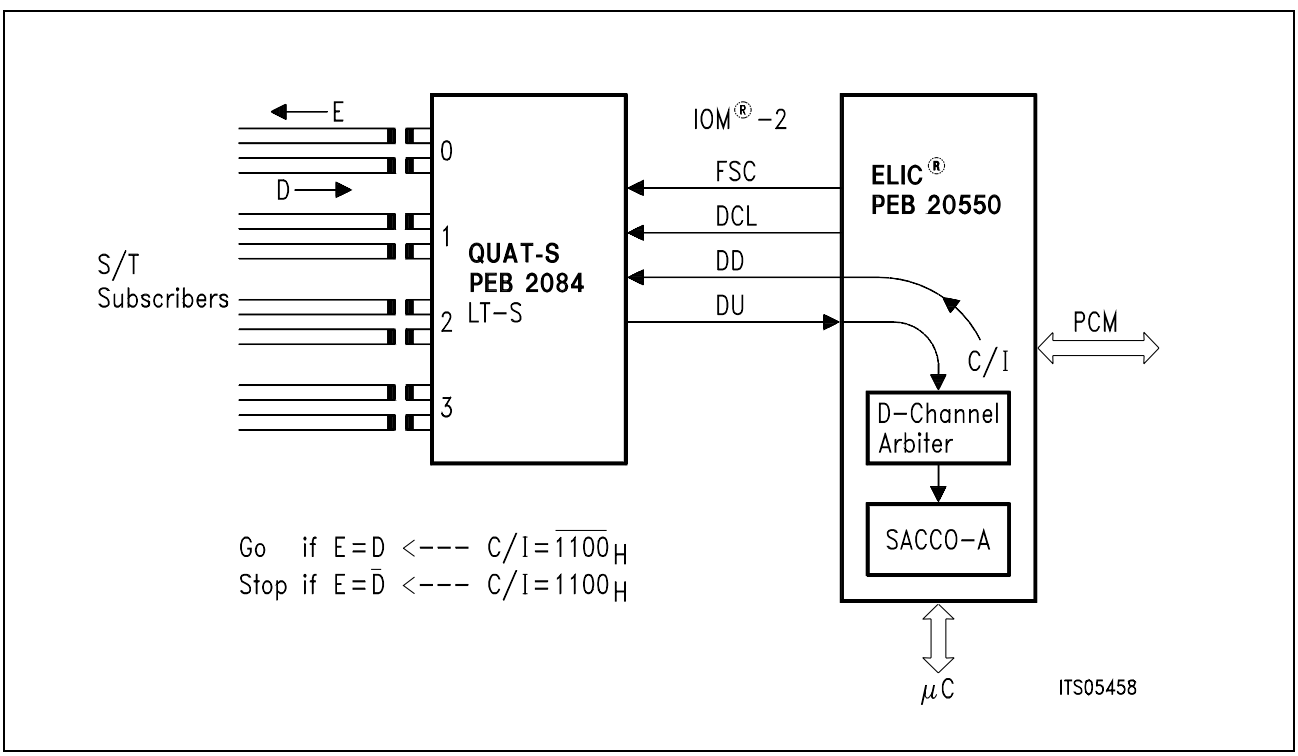


Figure 19
QUAT-S in LT-S Mode with a D-Channel Access via ELIC D-Channel Arbiter

The codes (C/I = $\overline{1100}_H$ and 1100_H) can only be used when the QUAT-S is in the state G3 activated (during INFO 4 transmission). Refer to **chapter 3.6.**

For a detailed description of the D-Channel Arbiter refer to “ELIC, PEB 20550, Technical Manual 9.93”, page 54, chapter 2.2.8.

D-Channel Access According to CCITT I.430 (Star Configuration)

The D-channel access is arbitrated among the terminals themselves, if the QUAT-S Auxiliary Register is programmed to DCM(1:0) = 10.

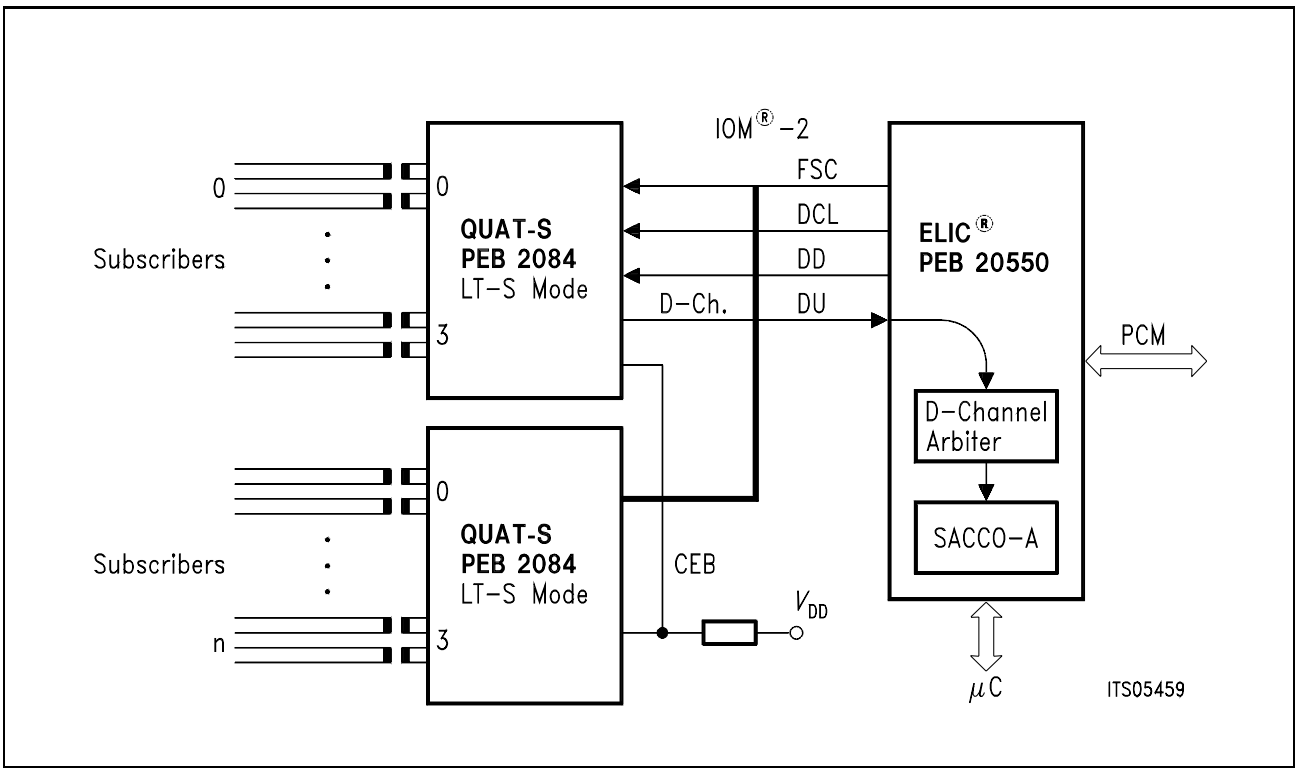


Figure 20
QUAT-S in LT-S Mode Supporting Arbitration According to CCITT I.430

The D-channel access control is established as a logical passive bus structure. All received D-channels are ANDed and the resulting value (internally connected to the pin CEB) is sent back as Echo bit on all involved S/T interfaces.

If more QUAT-S work in parallel the CEB pins (open drain output) are wired via an external pull-up resistor to V_{DD}.

The “short passive bus”, a system of multiple TE’s accessing a single D-channel, is extended to multiple physical S lines still representing a single logical “short passive bus”. It is a system with multiple B-channels using a single D-channel.

Only the winning D-channel reaches the ELIC. The other D-channels remain blocked until a TE encounters 8 (10) E-bits equal to the D-bit in a row.

The ELIC D-channel arbiter doesn't work in this application as an arbiter (all channels are permanently sent the C/I command "available" = 1000_H), it only detects the winning D-channel on the IOM interface and controls the connected LABD controller (SACCO-A).

LT-T Mode Configuration Register, bit 0: MODE = 1

D-channel collision resolution is always controlled according to CCITT I.430.

Four-Channel LT-T Applications

The pin DRDY conveys control information synchronous to the D-channel timeslots to control PEB 2075, IDEC, if the Auxiliary Register, bits DCM(1:0) = 10.
Stop when DRDY = "0", Go when DRDY = "1".

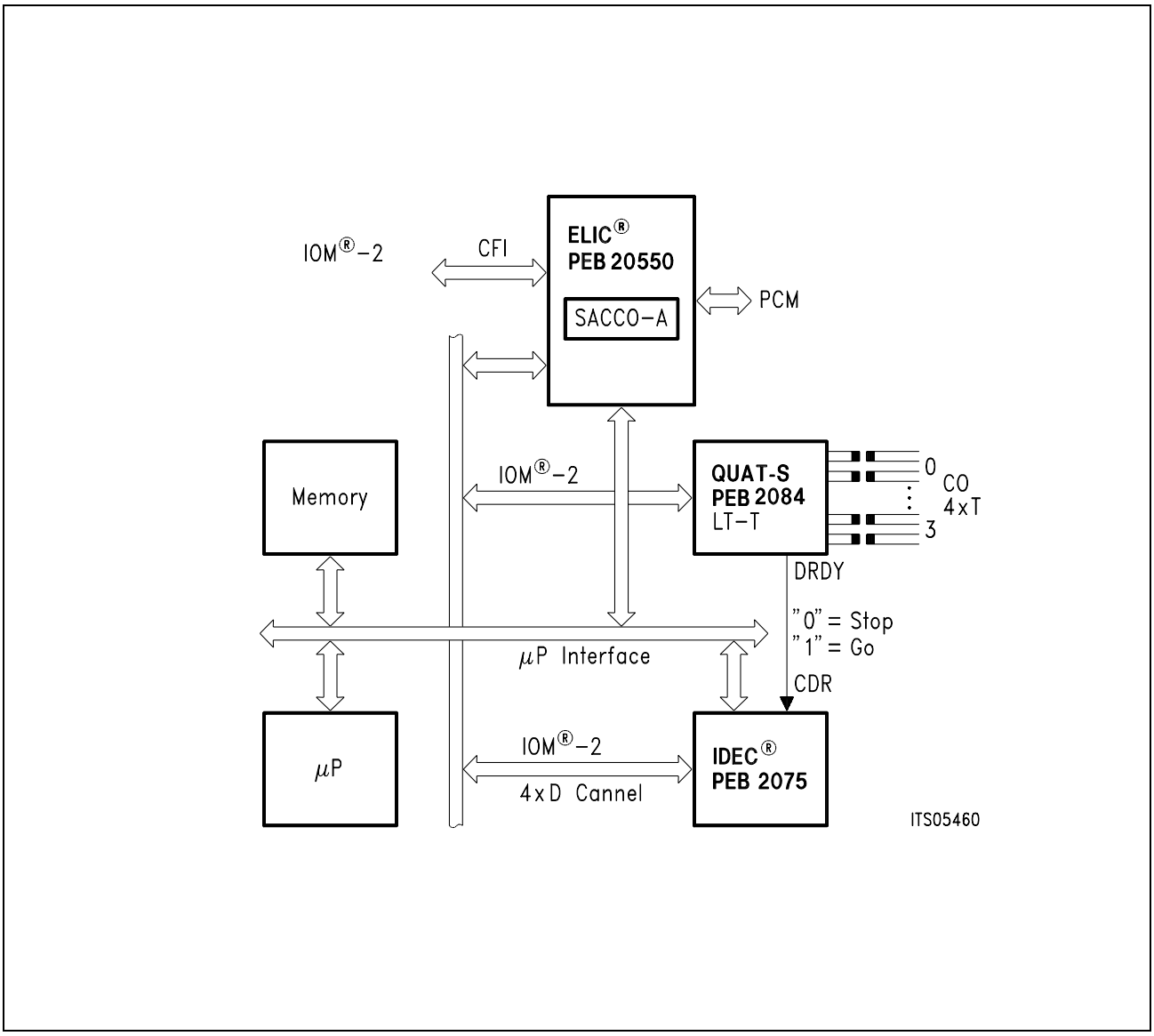


Figure 21
QUAT-S in LT-T Mode with IDEC for Four-Channel Applications

Single-Channel LT-T Applications

QUAT-S can also be used in a mixed mode, e.g. by programming three channels in LT-S mode and one channel in LT-T mode. The Auxiliary Register of only one channel can be programmed to DCM(1:0) = 11 and the Configuration Register pin RCLK to 1.

Whereas the subscriber D-channels are handled by the D-channel arbiter and SACCO-A in ELIC (as described in chapter LT-S Mode), the trunk D-channel is handled by the QUAT-S arbitration logic and SACCO-B in ELIC.

If the Echo bit differs from the D-bit then QUAT-S stops SACCO-B: DRDY = “1”, else SACCO-B may send data: DRDY = “0”. Pin DRDY conveys control information asynchronous to the D-channel timeslot.

This mode is applicable to single channel LT-T applications only.

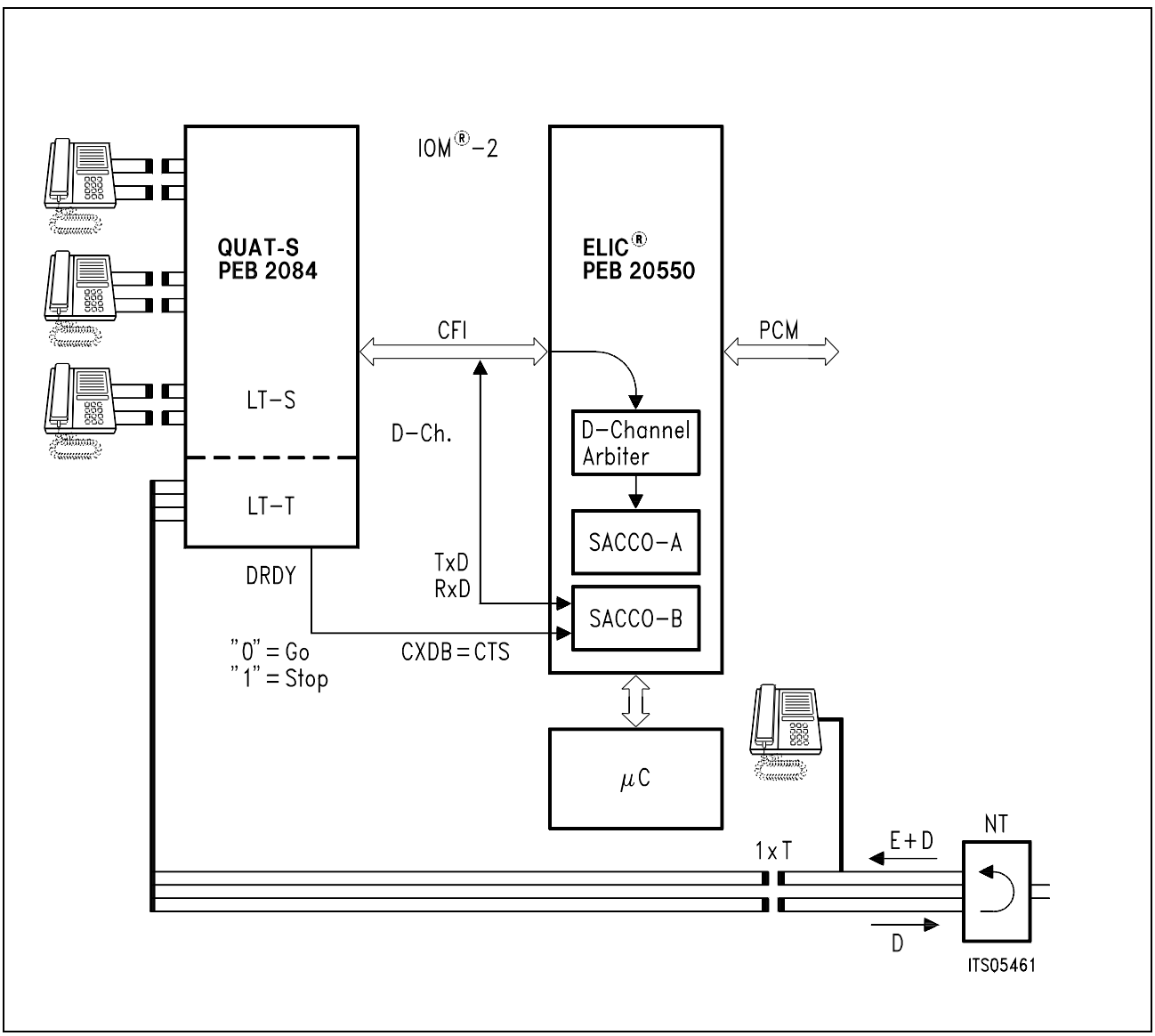


Figure 22
QUAT-S with SACCO-B for Single-Channel LT-T Applications

Clock generation for the above application is shown in **figure 14.**

3.3.4 Command/Indicate Channel

The exchange of control information in the C/I channel is state oriented. This means that a code in the C/I channel is repeated in every IOM frame until a next change is necessary. A new code must be found in two consecutive IOM frames to be considered as valid (double last look criterion).

C/I commands trigger QUAT-S layer-1 state machine in accordance with CCITT I.430.

For a list of the C/I codes and their use refer to **chapter 3.6.**

3.4 Activation and Deactivation

An internal finite state machine of the PEB 2084, QUAT-S, controls the activation/deactivation procedures, switching of loops and transmission of special pulse patterns. Such actions can be initiated by primitives (INFOS) on the S/T interface or by control codes (C/I) sent over the IOM-2 interface.

The IOM-2 interface should be kept active in both application modes, LT-S and LT-T, for the QUAT-S is always ready to transmit and receive messages.

Depending on the application mode and the transfer direction the QUAT-S state machines support about 20 different codes in conditional and unconditional states:

LT-S mode C/I codes data downstream = Commands: reset, test mode, activate req.,..
data upstream = Indications: not sync., code violation, timer out,..
States: deactivated, activated, pending, lost framing, test mode.
The state diagram is shown in **figure 23.**

LT-T mode C/I codes for data upstream = Commands: reset, test, activate request,..
data downstream = Indications: command x acknowledged,..
Conditional states: power up, pending deactivation, synchronized, slip detected,..
The state diagram is shown in **figure 24.**
Unconditional states can be entered from any conditional state and should be left with the command TIM: loop closed, test mode, reset state,..
The state diagram is shown in **figure 25.**

The activation and deactivation procedures implemented in the PEB 2084, QUAT-S, correspond with those implemented in the PEB 2081, SBCX.

3.4.1 LT-S Mode

Command / Indication Codes

Commands (downstream) LT-S mode	Abbreviation	Code	Remark
Deactivate request	DR	0000	(x)
Reset	RES	0001	(x)
Test mode 1	TM1	0010	Transmission of pseudo-ternary pulses at 2 kHz frequency (x)
Test mode 2	TM2	0011	Transmission of pseudo-ternary pulses at 96 kHz frequency (x)
Activate request	AR	1000	
Activate indication	AI	1100	Transmission of transparent INFO acc. to state diagram with inverted D-channel mirrored back in E-channel
Activate request loop	ARL	1010	Activation request for loop 2
Deactivate confirmation	DC	1111	Deactivation acknowledgment, quiescent state

(x) unconditional commands

Indications (upstream) LT-S mode	Abbreviation	Code	Remark
Timing	TIM	0000	
Resynchronizing	RSY	0100	Receiver is not synchronous
Activate request	AR	1000	INFO 1 received
Code violation received	CVR	1011	After each multi-frame the receipt of at least one illegal code violation is indicated four times. This function must be enabled by setting the RCVE-bit in the configuration register.
Activate indication	AI	1100	Synchronous receiver
Deactivate indication	DI	1111	Timer (32 ms) expired or INFO 0 received after deactivation request

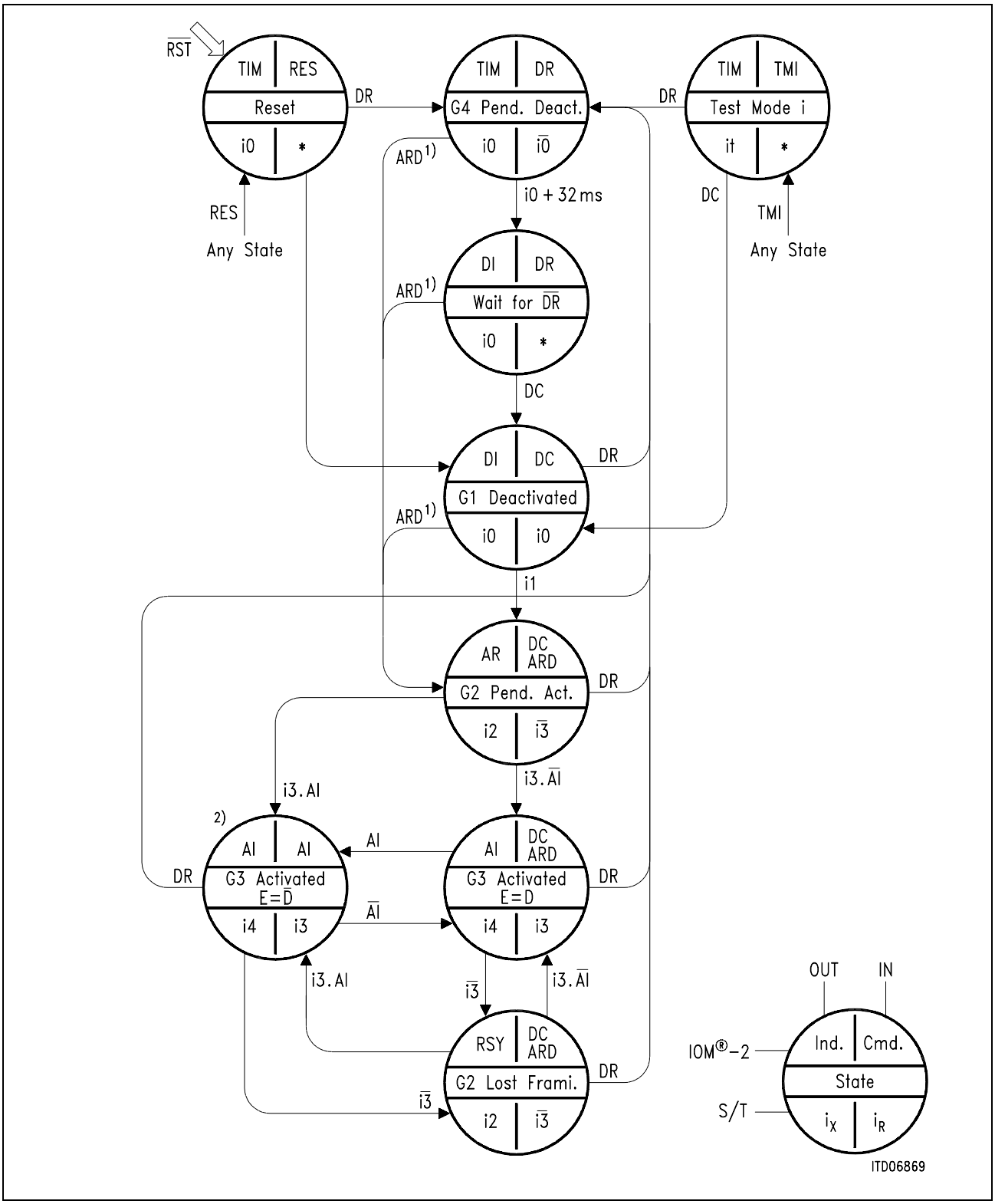


Figure 23
QUAT-S State Diagram of LT-S Mode

Note: 1) ARD stands for AR or ARL
2) only if DCM (1:0) = 11

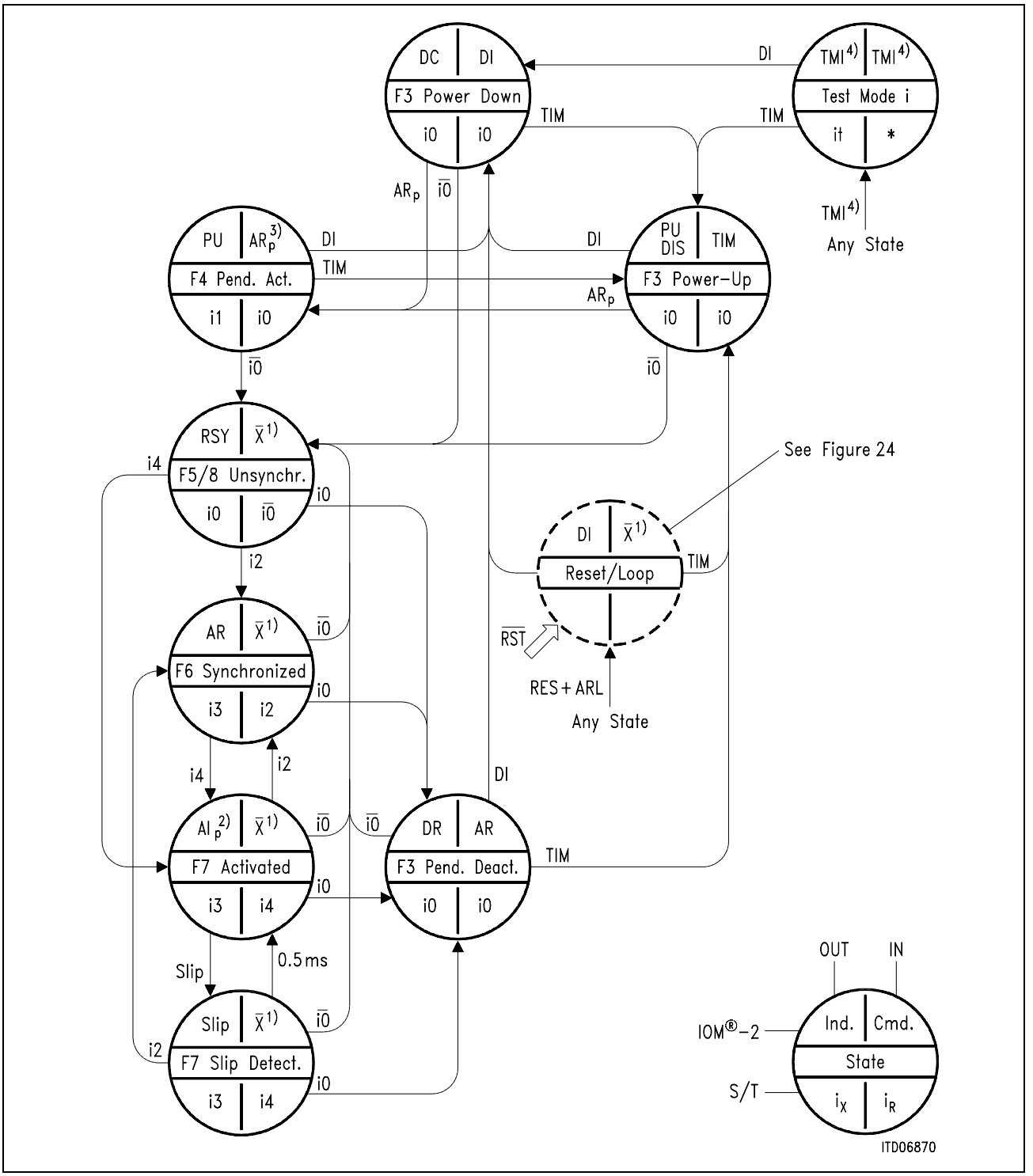


Figure 24
QUAT-S State Diagram in the LT-T Mode, Conditional States

Note: 1) × = $\overline{TM1}$ and $\overline{TM2}$ and $\overline{RES}$ and $\overline{ARL}$
2) AI_p stand for AI8 or AI10
3) AR_p TMI stands for AR8 or AR10
4) TMI stands for TM1 or TM2

LT-S Mode States

- G1 deactivated
  The line interface is not transmitting. There is no signal detected on the S interface, and no activation command is received in the C/I channel.
- G2 pending activation
  As a result of an INFO 1 detected on the S line or an ARD command, the line interface begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.
- G3 activated
  Normal state where INFO 4 is transmitted to the S interface. The line interface remains in this state as long as neither a deactivation nor a test mode is requested, nor the receiver looses synchronism. When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter keeps on sending INFO 4.
- G2 lost framing
  This state is reached when the line interface has lost synchronism in the state G3 activated.
- G4 pending deactivation
  This state is triggered by a deactivation request DR. It is an unstable state: indication DI (state “G4 wait for DR.”) is issued by the QUAT-S when: either INFO 0 is received, or an internal timer of 32 ms expires.
- G4 wait for $\overline{\text{DR}}$
  Final state after a deactivation request. The line interface remains in this state until a response to DI (in other words DC) is issued.
- Test mode 1
  Single alternating pulses are sent on the S interface (2 kHz repetition rate).
- Test mode 2
  Continuous alternating pulses are sent on the S interface (96 kHz).

3.4.2 LT-T Mode

Command / Indication Codes, Conditional States

Commands (upstream) LT-T Mode	Abbreviation	Code	Remark
Timing	TIM	0000	Line interface is powered up
Reset	RS	0001	(x)
Test mode 1	TM1	0010	Transmission of pseudo-ternary pulses at 2 kHz frequency (x)
Test mode 2	TM2	0011	Transmission of pseudo-ternary pulses at 96 kHz frequency (x)
Activate request, priority 8	AR8	1000	Activation command, D channel priority is 8
Activate request, priority 10	AR10	1001	Activation command, D channel priority is 10
Active request loop	ARL	1010	Activation of loop 3 (x)
Deactivate indication	DI	1111	Line interface is powered down

(x) unconditional commands

Indications (downstream) LT-T Mode	Abbreviation	Code	Remark
Deactivate request	DR	0000	Deactivation request via S/T interface
Reset	RES	0001	Reset acknowledge
Test mode 1	TM1	0010	TM1 acknowledge
Test mode 2	TM2	0011	TM2 acknowledge
Slip detected	SLIP	0011	Wander is larger than 50 µs peak-to-peak (or 25 µs peak-to-peak if programmed, refer to the C/W-bit of the Configuration Register)
Resynchronization during level detect	RSY	0100	Signal received, receiver not synchronous
Power up	PU	0111	Line interface is powered up
Activate request	AR	1000	INFO 2 received
Activate request loop	ARL	1010	Loop 3 closed
Code violation received	CVR	1011	After each multiframe the receipt of at least one illegal code violation is indicated four times. This function must be enabled by setting the RCVE-bit in the configuration register.
Activate indication loop	AIL	1110	Loop 3 activated
Activate indication with priority class 8	AI8	1100	INFO 4 received, D-channel priority is 8 or 9
Activate indication with priority class 10	AI10	1101	INFO 4 received, D-channel priority is 10 or 11
Deactivate confirmation	DC	1111	Line interface is powered down

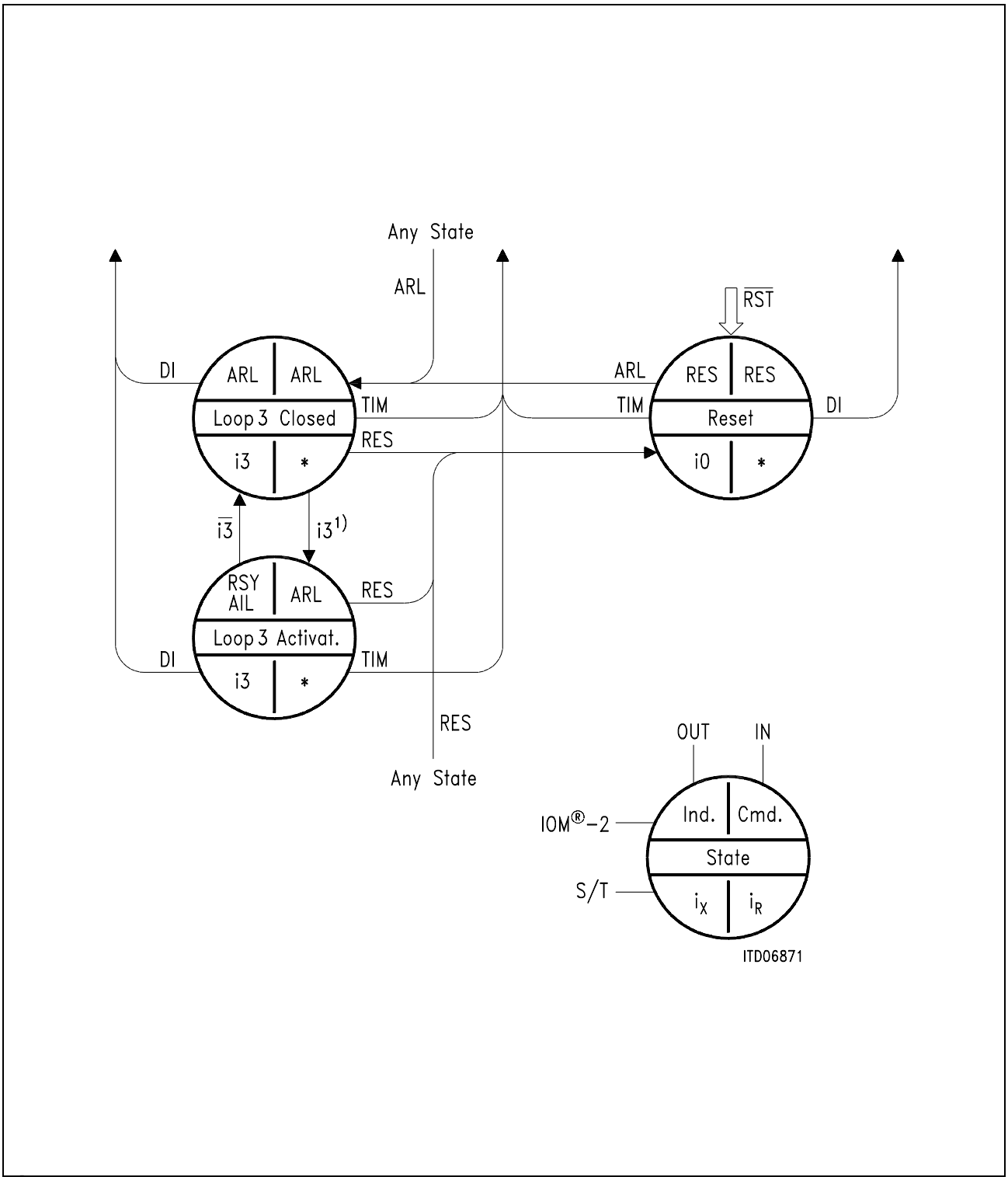


Figure 25
QUAT-S State Diagram in the LT-T Mode, Unconditional States (Transitions)

Note: 1) In state loop 3 activated, i3 is the internal signal, the external signal is i0.

LT-T Mode, Conditional States

- F3 power down
  This is the deactivated state of the physical protocol. The receive line awake unit is active.
- F3 power up
  This state is similar to “F3 power down”. The state is invoked by a C/I command TIM = “0000” (or DI static low). After the subsequent activation of the clocks the “Power Up” message is output.
- F3 pending deactivation
  The line interface reaches this state after receiving INFO 0 (from states F5 to F8). From this state an activation is only possible from the line (transition “F3 pend. deact.” to “F5 unsynchronized”). The power down state may be reached only after receiving DI.
- F4 pending activation
  Activation has been requested from the terminal, INFO 1 is transmitted, INFO 0 is still received, “Power Up” is transmitted in the C/I channel. This state is stable: timer T3 (I.430) is to be implemented in software.
- F5/8 unsynchronized
  At the reception of any signal from the NT, the QUAT-S ceases to transmit INFO 1, adapts its receiver circuit, and awaits identification of INFO 2 or INFO 4. This state is also reached after the line interface has lost synchronism in the states F6 or F7 respectively.
- F6 synchronized
  When the QUAT-S receives an activation signal (INFO 2), it responds with INFO 3 and waits for normal frames (INFO 4).
- F7 activated
  This is the normal active state with the layer-1 protocol activated in both directions. From state “F6 synchronized”, state F7 is reached almost 0.5 ms after reception of INFO 4.
- F7 slip detected
  When a slip is detected between the T interface clocking system and the IOM-2 interface clocks (phase wander greater than 50 µs, data may be disturbed, or 25 µs if programmed in the configuration register) the line interface enters this state, synchronizing again the internal buffer. After 0.5 ms this state is left again.

LT-T Mode, Unconditional States

The unconditional states should be left with the command TIM.

- Loop 3 closed
  On Activate Request Loop command, INFO 3 is sent by the line transmitter internally to the line receiver (INFO 0 is transmitted to the line). The receiver is not yet synchronized.
- Loop 3 activated
  The receiver is synchronized on INFO 3 which is looped back internally from the transmitter. Data may be sent. The indication “AIL” is output to indicate the activated state. When the S/T line awake detector, which is switched to the line, detects an incoming signal, this is indicated by “RSY”.
- Test mode 1
  Single alternating pulses are sent on the T interface (2 kHz repetition rate).
- Test mode 2
  Continuous alternating pulses are sent on the T interface (96 kHz).
- Reset state
  A hardware or software reset (RES) forces the line interface to an idle state where the analog components are disabled (transmission of INFO 0) and the T line awake detector is inactive. Thus activation from the NT is not possible.

3.4.3 Example of Activation/Deactivation

An activation and deactivation procedure between a QUAT-S and an ISAC-S or SBCX in TE mode over the S/T interface line is shown in **figure 26**. It illustrates how the state machines of the respective modes interwork to facilitate activation and deactivation. In this case activation was initiated by an AR request at the terminal side and deactivation by a DR command at the LT side. Activation could also be initialized at the LT side using an AR request.

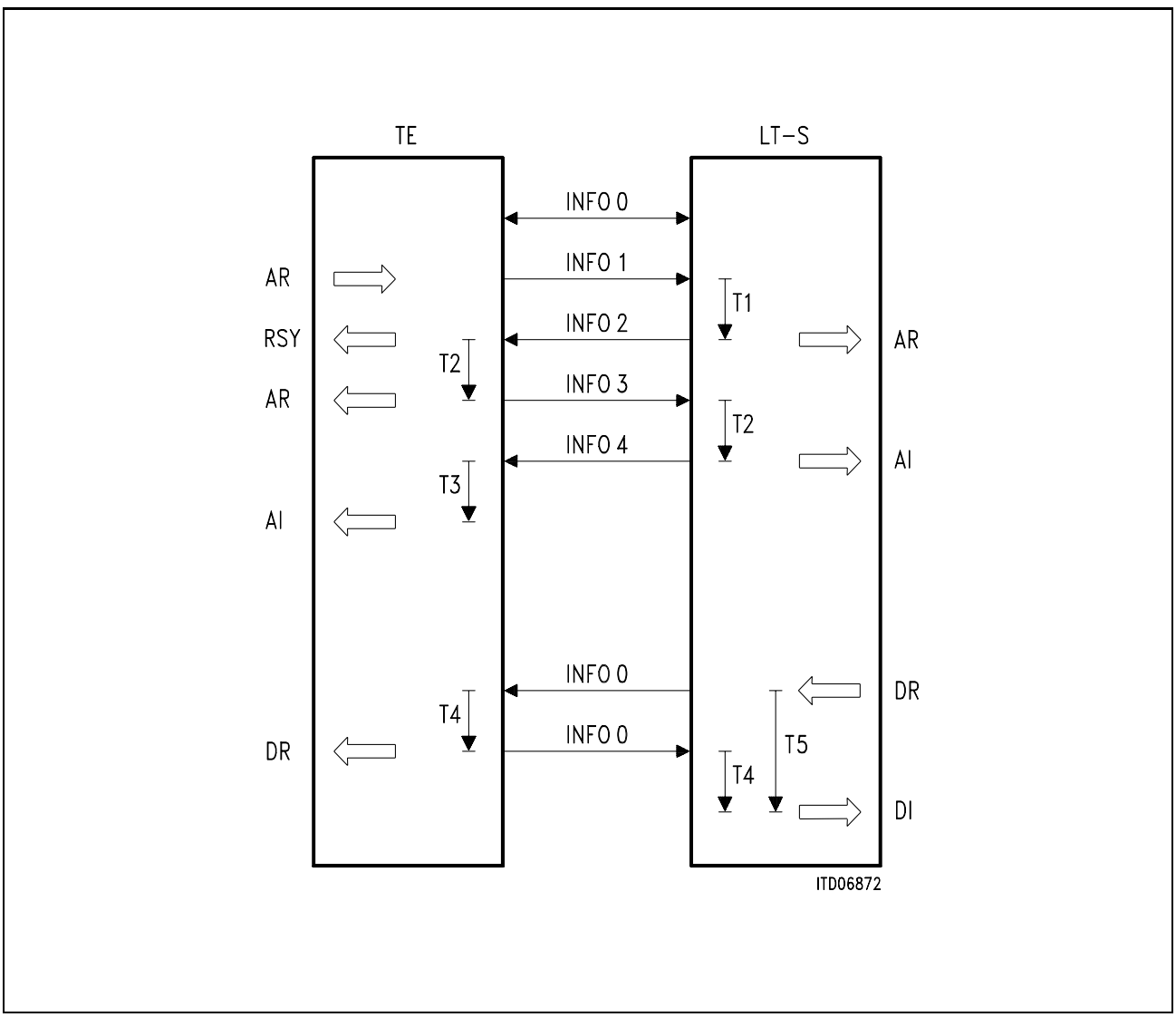


Figure 26
Example of S/T Interface Activation and Deactivation

Note: T1: 4 ms time for INFO 1 detection
T2: ≤ 1 ms time for synchronization
T3: 500 ms time for INFO 4 detection (2 subsequent frames)
T4: 16 ms time for INFO 0 detection
T5: 32 ms timer

3.5 Diagnostic Functions, Test Loop-backs

Different test loops for B1, B2 and D-channels can be closed in the QUAT-S:

- Transparent analog loops (the data are also sent forward).
- Non transparent analog loops (the forward data path is blocked).
- External transparent analog loop for board test.

The loops may be closed in both operational modes, in LT-S and in LT-T, via the C/I command ARL which may be applied (continuously) in the states “G4 pending deactivation”, “G4 wait for $\overline{DR}$” and “G1 deactivated”.

Loop transparency can be achieved by setting the LP-bit in the Configuration Register.

An example is shown in **figure 27.**

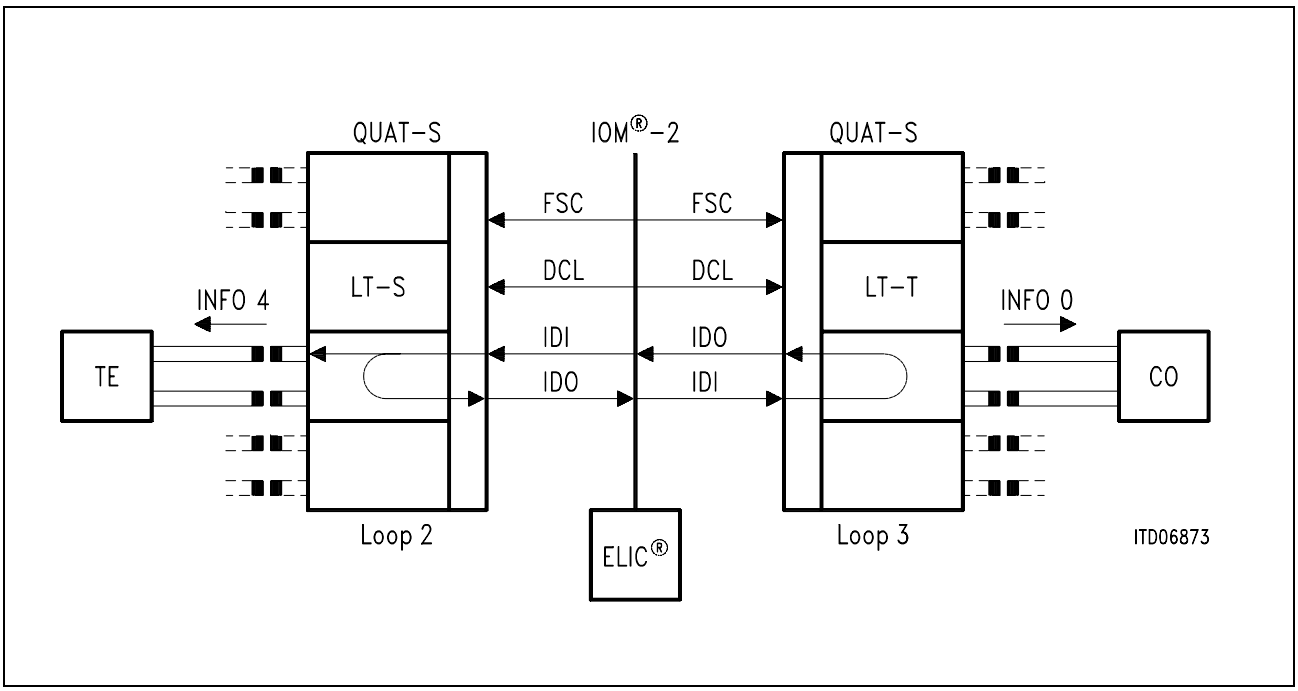


Figure 27
An Example for QUAT-S in LT-S Mode with a Transparent Loop (Loop 2) and in LT-T Mode with a Non Transparent Loop (Loop 3)

Loop 2 and 3 are activated over the IOM-2 interface with Activate Request Loop (ARL).

3.6 S and Q Channel Access

According to CCITT recommendation I.430 a multi-frame (= 20 consecutive S/T frames) provides an additional communication channel between TE and LT or LT and CO via S and Q bits. Refer to **figure 28.**

Two S channels (S1 and S2) can be used by the QUAT-S for communication in data downstream direction.

The Q channel bits are defined to be the bits in the F_A bit position and are used for communication in data upstream direction.

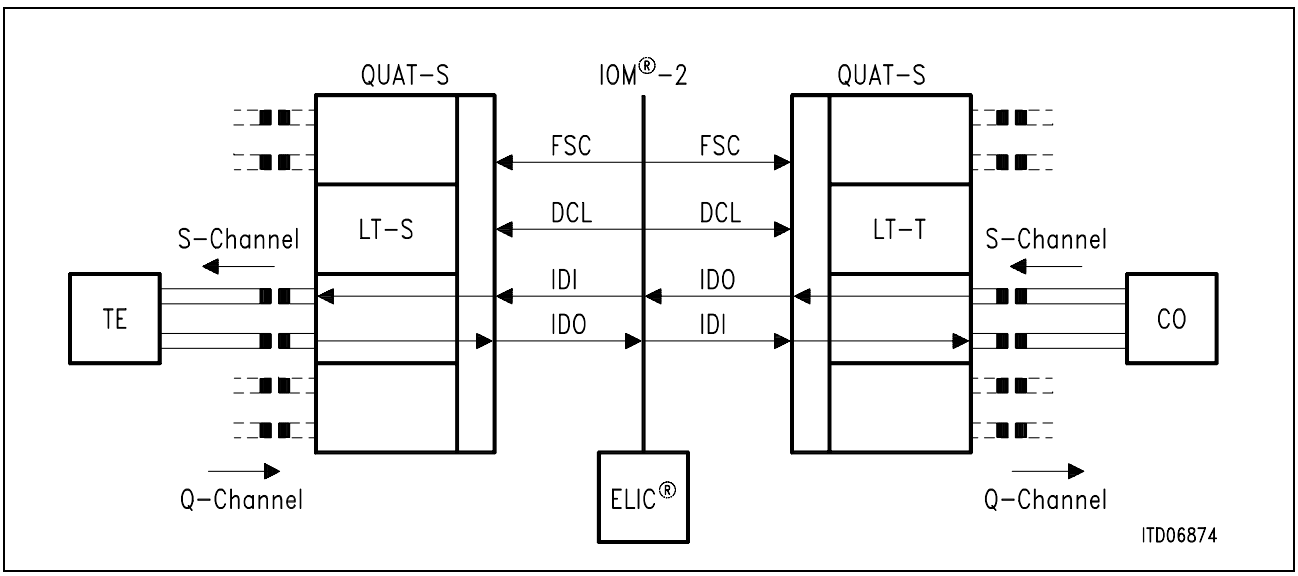


Figure 28
Direction of S and Q Channels in Different Application Modes

The following table shows the S and Q bit positions within the multi-frame (20 S/T frames).

Frame Number	LT to TE or CO to LT	TE to LT or LT to CO
1 2	S11 S21	Q1 ZERO
6 7	S12 S22	Q2 ZERO
11 12	S13 S23	Q3 ZERO
16 17	S14 S24	Q4 ZERO
1 …	S11 …	Q1 …

All other S and Q bit positions within the remaining 12 frames of the multi-frame carry the value ZERO.

The S and Q bits are accessed by the ELIC or EPIC via IOM-2 interface monitor channel. The bits are handled in byte format packed in the lower nibble. The upper nibble is used as identifier for the message type. The bit structure used by the QUAT-S is outlined in the following table.

Identifier	Downstream Data	Upstream Data
0 0 0 1	S11 S12 S13 S14	
0 0 1 0	S21 S22 S23 S24	
0 0 0 1		Q1 Q2 Q3 Q4

QUAT-S has implemented a 3×4 bit RAM as buffer for the S and Q bits. The 4-bit RAM cells can be addressed separately.
The data are handled by the QUAT-S in either non auto mode or in transparent mode.

In the transparent mode the S data are transferred in downstream direction as a real time data stream of 1.600 bit/s (8 bits in 5 ms = 20×250 µs), the Q data are transferred in upstream direction as a real time data stream of 800 bit/s (4 bits in 5 ms).

In non auto mode the received S and Q channels are checked for code changes and, if a change is detected, the new four bits are transferred. In transmit direction each of the 4-bit message is repeated until a new word is written into the buffer (e.g. into the MFFIFO in ELIC).

3.7 Default-Use of Pin CEB/$\overline{\text{SSYNC}}$

The PEB 2084, QUAT-S, uses the input signal at pin CEB/$\overline{\text{SSYNC}}$ as an external multiframe synchronization input in any case except if DCM(1:0) is set to “10” in any of the four channels. The external multiframe synchronization input signal is expected to be low for 125 µs and high for 2n + 1 times 125 µs thus defining an S/T interface multiframe of n + 1 frames. The edges of the external multiframe synchronization input signal have to be in coincidence with the rising edges of FSC. Each low at this input will generate one frame with M-bit as binary ONEs at the S/T interface output. When setting bit MFD (configuration register) to “1”, this function enables the generation of arbitrary multiframes, which may be useful to synchronize digital cellular wireless communications equipment.

While using $\overline{\text{SSYNC}}$ for M-bit generation the short FSC signal is not allowed as it would reset the Super-Frame generated by $\overline{\text{SSYNC}}$. If not used, the $\overline{\text{SSYNC}}$ input must be connected via a pull-up resistor to V_{DD}.

4 Registers Description

As the QUAT-S contains four PEB 2081, SBCX, cores, it contains four complete register sets. All registers programming is done via the four IOM monitor channels.

Access to the registers of the QUAT-S are treated as local functions and therefore are marked with the code “1000” in the first four bits of the message:

Monitor message:

Code = 1 0 0 0	Internal address	D7 D6 D5 D4	D3 D2 D1 D0

Register Read

An internal register is read by setting the internal address to zero (0_H) and indicating the address of the specific register in the bits D(3:0). The bits D(7:4) are set to zero.

E.g. “80_H 01_H” is the read command for the register 1_H, the Configuration Register.

Code = 1 0 0 0	0 0 0 0	0 0 0 0	register addr. = 01_H

The response message from QUAT-S comprises two bytes, the first showing the address after the local function code, the second showing the register data.

E.g. “81_H (D7:0)” is the response to a read command on address 1_H, where D(7:0) is the content of the Configuration Register.

Code = 1 0 0 0	register addr.= 01_H	D7 D6 D5 D4	D3 D2 D1 D0

Register Write

An internal register is written by setting the internal address to the address of the specific register. The register will then be loaded with the value of D(7:0),
e.g. “81_H $5D_H$” programs the Configuration Register (addr. 1_H) with the value $5D_H$.

Code = 1 0 0 0	register addr.	D7 D6 D5 D4	D3 D2 D1 D0

4.1 Identification Register

Read, Address: 0_H

	bit 7							bit 0
Format:	0	1	0	0	0	1	0	0

After the read command “80_H 00_H” according to the procedure described above the QUAT-S transmits the response “80_H 44_H”.

The returned value 44_H of the Identification Register is specific for the PEB 2084, QUAT-S.

4.2 Configuration Register

Read/Write, Address: 1_H

	bit 7							bit 0
Format:	MFD	RCLK	0	LP	SQM	RCVE	C/W	MODE

Initial value: 00_H

Bit-name	Description
MFD	**Multi-Frame Disable (write):** 0: All multi-frame functions active. 1: Multi-frame generation (LT-S) or synchronization (LT-T) prohibited. No SQ monitor messages released. **Multi-Frame Detected (read):** 0: No multi-frame synchronization achieved. 1: Multi-frame synchronization (LT-T) achieved.
RCLK	**Receive Clock** 0: No output signal at pin CLK1/IDS (if all QUAT-S channels are programmed to 0 at this bit location, the output pin CLK1 is tristated) 1: The 1.536 MHz clock synchronized to the receiver (LT-T) is output at the pin CLK1(Due to an internal short-circuit safety logic, a 1 is only processed if the other three channels are set to 0 at this bit location.) **Note:** The pin CLK1/IDS is used to pin-strap the DCL data clock ratio during HW reset phase 10: Double clock 11: Single clock
LP	**Loop** LT-S mode 0: Transparent analog loop 1: Non transparent analog loop LT-T mode 0: Non transparent analog loop 1: External transparent loop
SQM	**SQ channel handling Mode selection** 0: Non auto mode only S1 and Q channels 1: Transparent mode S1, S2 and Q channels

Bit-name	Description
RCVE	**Receive Code Violation Indication (C/I) Enable** 0: Normal operation 1: A code violation detector is implemented to support the Far-end-code-violation (FECV) function according to ANSI T1.605. After each multi-frame the receipt of at least one illegal code violation is indicated by the occurrence of four times the CI code 1011 (CVR).
C/W	**Configuration / Wander detection** LT-S mode: Configuration 0: Point-to-point or extended passive bus configuration (adaptive timing recovery). 1: short passive bus configuration (fixed timing recovery) LT-T mode: Wander detection (warning on slip detection in C/I, data may be lost!) 0: “SLIP” after 50 µs wander 1: “SLIP” after 25 µs wander
MODE	**Mode select** 0: LT-S mode selected 1: LT-T mode selected

4.3 Loopback Register

Read/Write, Address: 2_H

	bit 7							bit 0
Format:	0	SB2	SB1	0	0	0	1	0

Initial value: 02_H

Bit-name	Description
SB2	Loopback B2 channel at the S/T interface
SB1	Loopback B1 channel at the S/T interface

Note: Register bits not described may exist in hardware due to the use of the PEB 2081, SBCX, core. Writing those bits other than the default value will cause unexpected behavior of the device.

4.4 Auxiliary Register

Read/Write, Address: 4_H

	bit 7							bit 0
Format:	CI3	CI2	CI1	CI0	TOD	0	DCM1	DCM0

Initial value: CI(3:0), 0_H

Bit-name	Description
CI(3:0)	**C/I codes as in C/I channel** The indication can be read via monitor channel CI (3:0).
TOD	**Time-Out Disable** 0: Monitor timeout (minimum 5 ms) 1: The time-out function of the monitor transmitter can be disabled to ease manual software debugging.
DCM(1:0)	**D-channel mode:** Specific D channel associated functions including the pins DRDY and CEB/$\overline{\text{SSYNC}}$: 00: Transparent D-channel, pins DRDY and CEB/$\overline{\text{SSYNC}}$ tristated. 10: LT-T mode: D-channel collision resolution according to CCITT I.430. Pin DRDY conveys control information synchronous to D-channel timeslots to control PEB 2075, IDEC (0: stop; 1: go). LT-S mode: D-channel access control by establishing a logical passive bus structure, where the received D-channel is ANDed with the other channels selected over pin CEB and the resulting value is sent back as Echo bit. 11: LT-T mode: D-channel collision resolution according to CCITT I.430. Pin DRDY conveys asynchronous control information to control SACCO-B in the ELIC, PEB 20550. This mode is only applicable for a single channel LT-T application (0: go; 1: stop). LT-S mode: D-channel access control via the central D-channel arbiter unit of the PEB 20550, ELIC. Dependent on the command, each channel mirrors the received D-channel into the Echo channel inverted command 1100_H) or unchanged ($\overline{1000}_H$). 01: Not applicable

Note: Register bits not described may exist in hardware due to the use of PEB 2081, SBCX, core. Writing those bits other than the default value will cause unexpected behavior of the device.

4.5 Other Registers

Other registers are implemented at address locations 3_H, 5_H, and 8_H. Access to those monitor addresses may cause unexpected behavior of the device.

5 Electrical Characteristics

All characteristics given are valid under the following conditions unless otherwise indicated:
T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

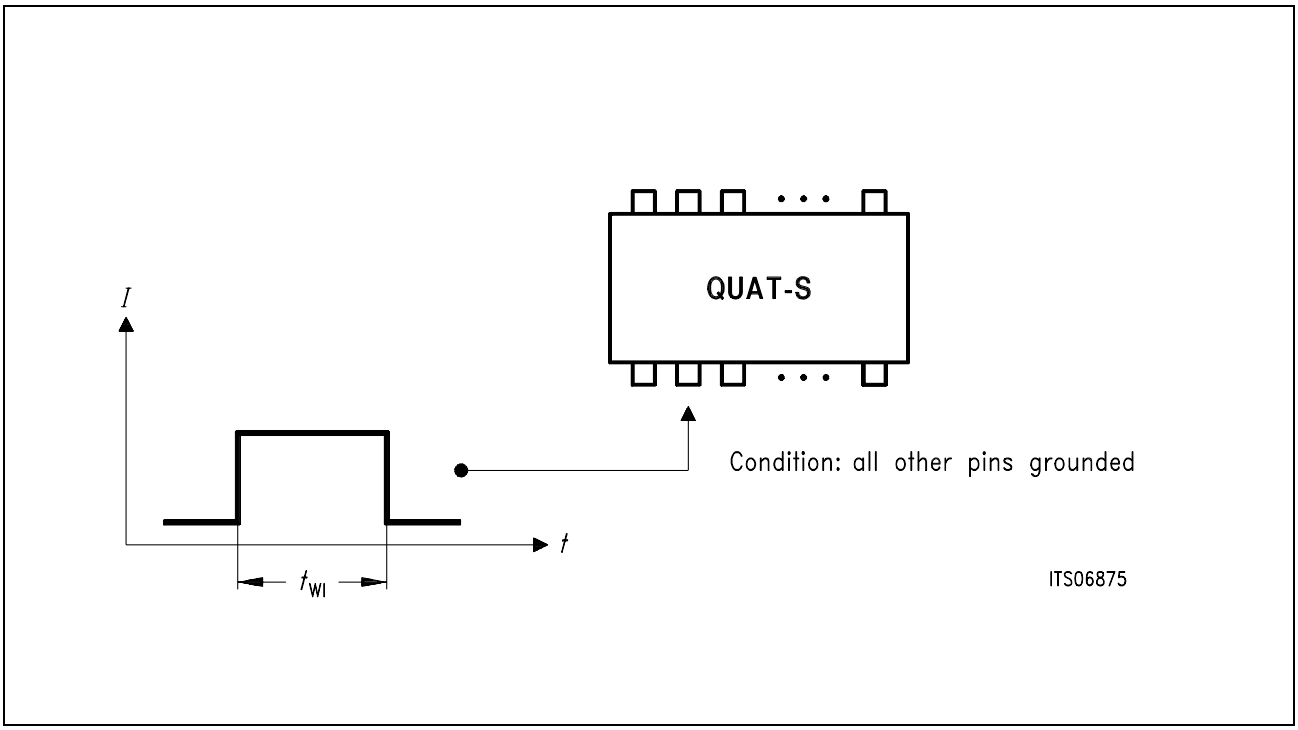
5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Stresses above the listed values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse. For the destruction current limits refer to **figure 29.**



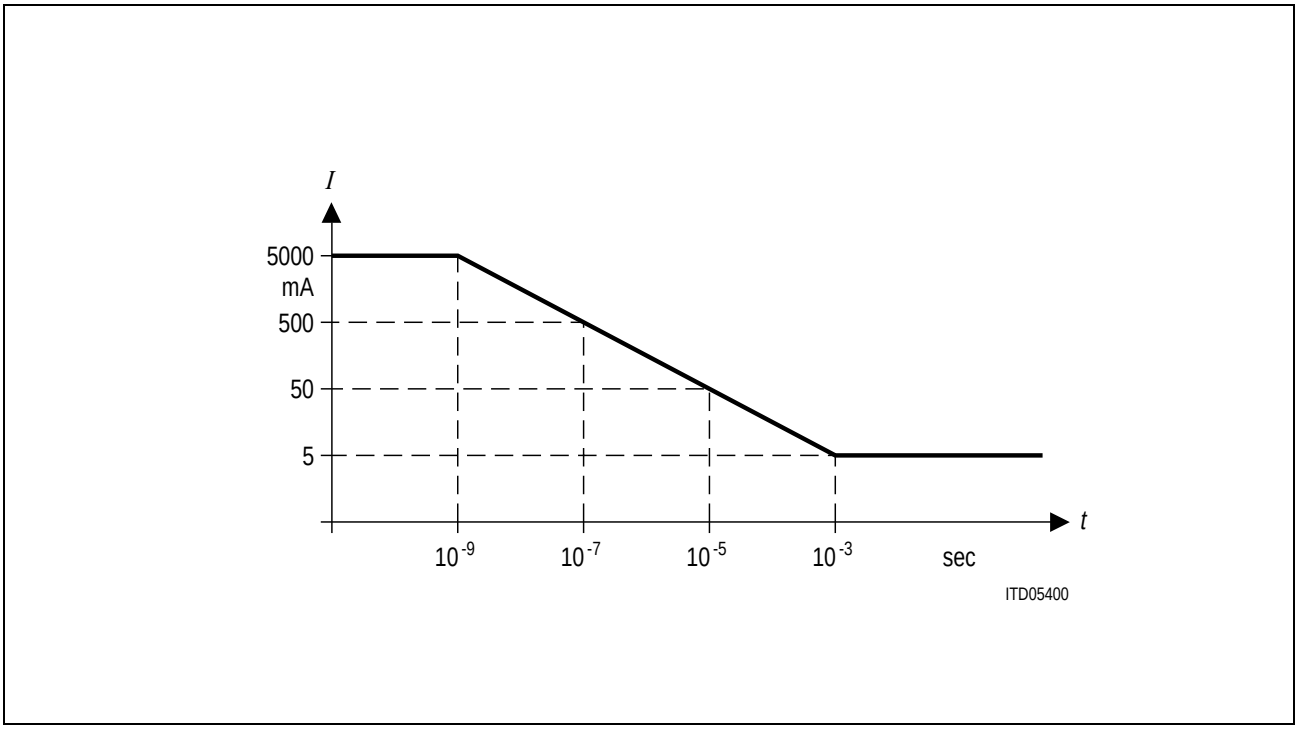


Figure 29
Maximum Line Input Current for the Receiver

5.2 DC Characteristics

Pin	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All pins except SXna,b; SRna,b XTAL1, 2	Input voltage	V_{IL}	– 0.4	+ 0.8	V	
	Input high voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
	Output low voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
DRDY, IDO	Output low voltage	V_{OL1}		0.45	V	I_{OL} = 7 mA
All pins except SXna,b; SRna,b; XTAL1, 2	Output high voltage	V_{OH}	2.4		V	I_{OH} = – 400 µA
			V_{DD} – 0.5		V	I_{OH} = – 100 µA
	Input leakage current	I_{LI}		+ 1	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		+ 1	µA	0 V ≤ V_{OUT} ≤ V_{DD}
SXna,b	Absolute value of output pulse amplitude ($V_{SXna} - V_{SXnb}$)	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω[1)] R_L = 400 Ω[1)]
SXna,b	Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω[1)]
SXna,b	Transmitter output impedance	Z_X	10 0		kΩ Ω	inactive or during binary one (V_{DD} = 0 … 5 V) during binary zero R_L = 50 Ω
SRna,b	Receiver input impedance	Z_R	30 100		kΩ Ω	V_{DD} = 5 V V_{DD} = 0 V
XTAL1	Input high voltage	V_{IH}	3.5	V_{DD} + 0.4	V	
XTAL1	Input low voltage	V_{IL}	– 0.4	1.5	V	
XTAL2	Output high voltage	V_{OH}	4.5		V	I_{OH} = 5 µA, C ≤ 50 pF
XTAL2	Output low voltage	V_{OL}		0.4	V	I_{OH} = 5 µA, C ≤ 50 pF

Note: [1)] Due to the transformers, the load resistance as seen by the circuit is four times R_L.

DC Characteristics (cont'd)

Pin	Parameter		Symbol	Limit Values		Unit	Test Condition
				min.	max.		
	Power supply current	operational	I_{CC}		55	mA	V_{DD} = 5 V inputs at V_{SS}/V_{DD}
		power down			5	mA	No outputs loads, no XTAL1
		power down			10	mA	No output loads, with XTAL1

5.3 Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
All pins except SXn a, b	Pin capacitance	C_{IO}		7	pF
SXn a, b	Output capacitance against V_{SS}	C_{OUT}		10	pF
XTAL1, 2	External load capacitance	C_L		50	pF

5.4 Recommended Oscillator Circuits

Crystal nominal frequency: 7.68 MHz ± 100 ppm

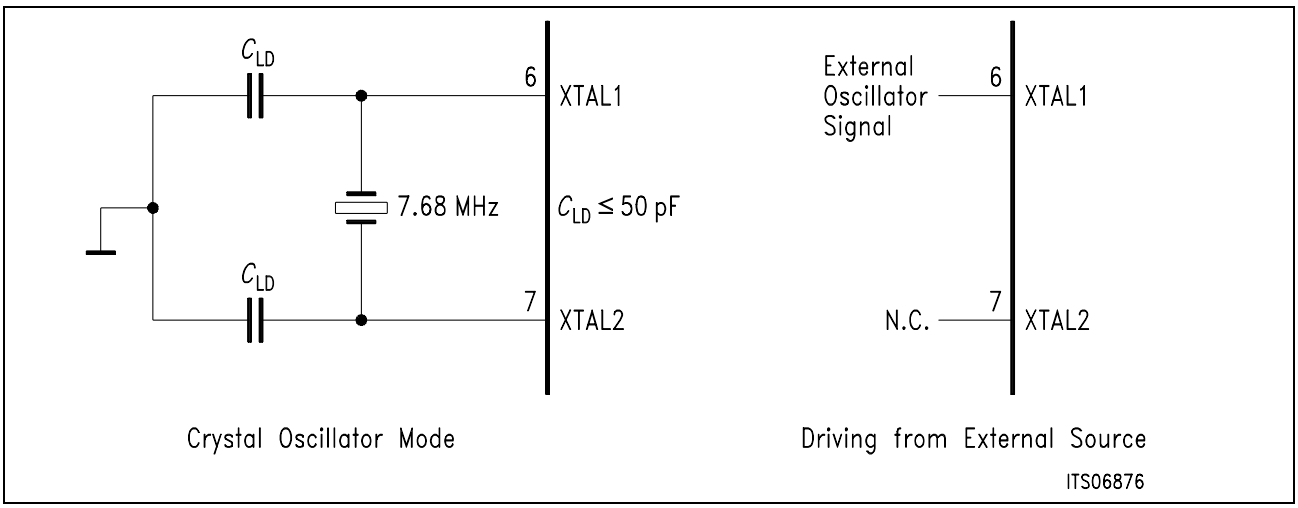


Figure 30
Recommended Oscillator Circuits

5.5 AC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %

AC testing: Set-up, Hold, Delays
Inputs are driven at V_{DD} – 0.5 V for a logic “1” and 0.45 V for a logic “0”. Timing measurements are made at 2.0 V for a logic “1” and at 0.8 V for a logic “0”.

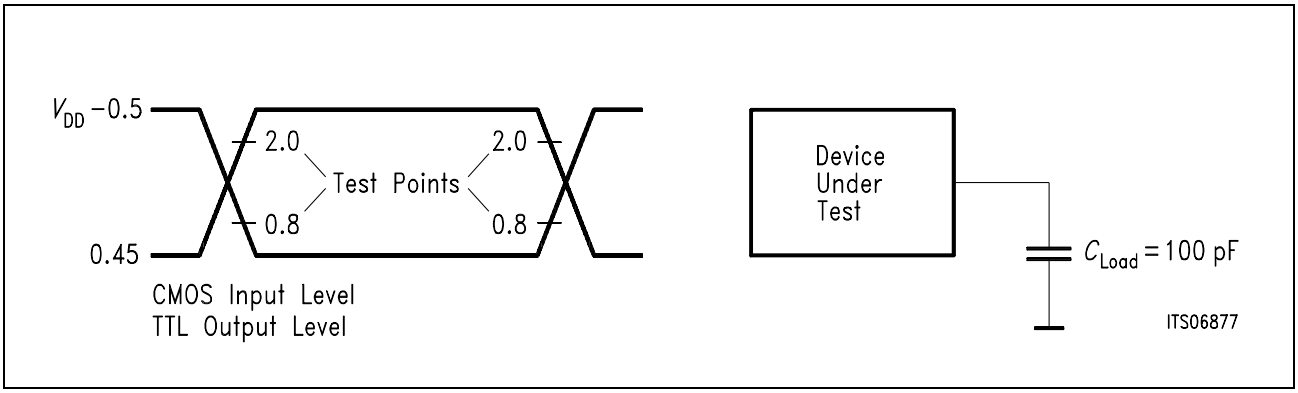


Figure 31
Input/Output Wave Form for AC Tests

Jitter

The clock input FSC is used as reference clock to provide the 192 kHz clock for the S/T interface. In the case of a desynchronous 7.68 MHz clock generated by an oscillator, the clock FSC should have a jitter of less than 50 ns peak-to-peak.

5.6 Clocks

CLK1

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High phase of clock	t_{WH}	250		ns	50 pF load capacitance at CLK1
Low phase of clock	t_{WL}	250		ns	50 pF load capacitance at CLK1
Clock period	T_p	650.8	651.2	ns	

CLK2

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High phase of clock	t_{WH}	40		ns	50 pF load capacitance at CLK2
Low phase of clock	t_{WL}	40		ns	50 pF load capacitance at CLK2
Clock period	T_P	130.16	130.24	ns	

CLK2 is directly derived from the oscillator clock and can drive up to 6 oscillator inputs of other communication ICs, e.g. ISAC-S, PEB 2085.

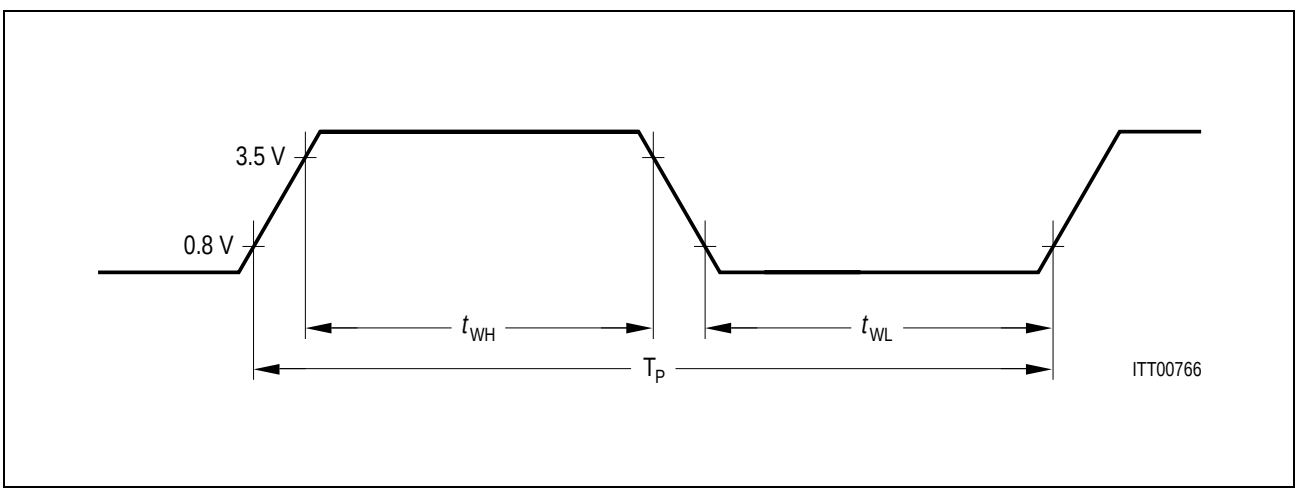


Figure 32
Definition of Clock Period and Width

5.7 IOM®-2 Interface Timing

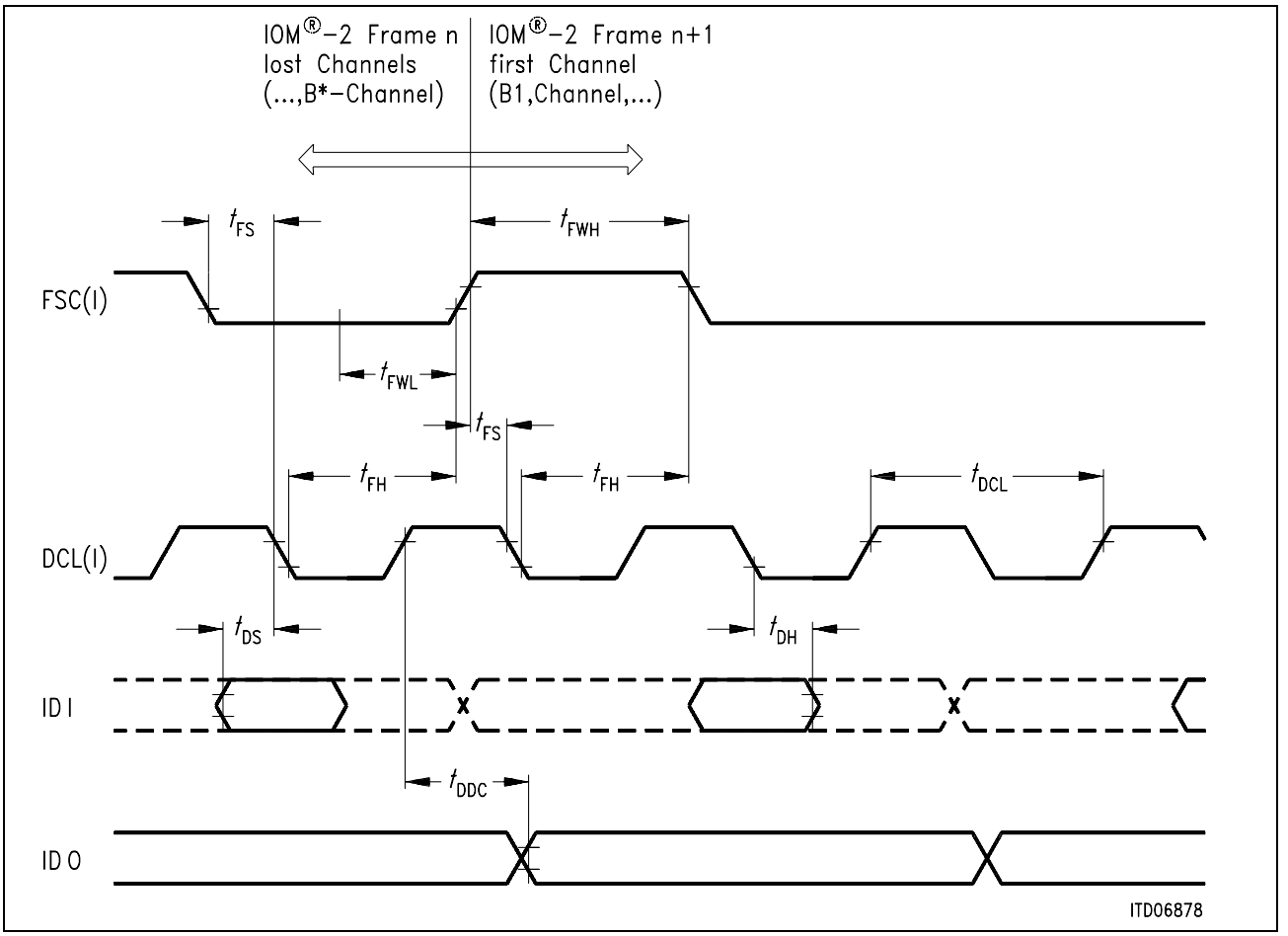


Figure 33
Timing of the IOM®-2 Interface with Double Data Rate DCL

Timing Characteristics of the IOM®-2

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Frame sync hold	t_{FH}	30			ns	
Frame sync setup	t_{FS}	70			ns	
Frame sync high	t_{FWH}	130			ns	
Frame sync low	t_{FWL}	t_{DCL}				
Data delay to clock	t_{DDC}			100	ns	
Data delay to frame[1)]	t_{DDF}			150	ns	
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

Note: [1)] $t_{DDF} = 0.5\ t_{DCL} + t_{DDC} - t_{FH}$

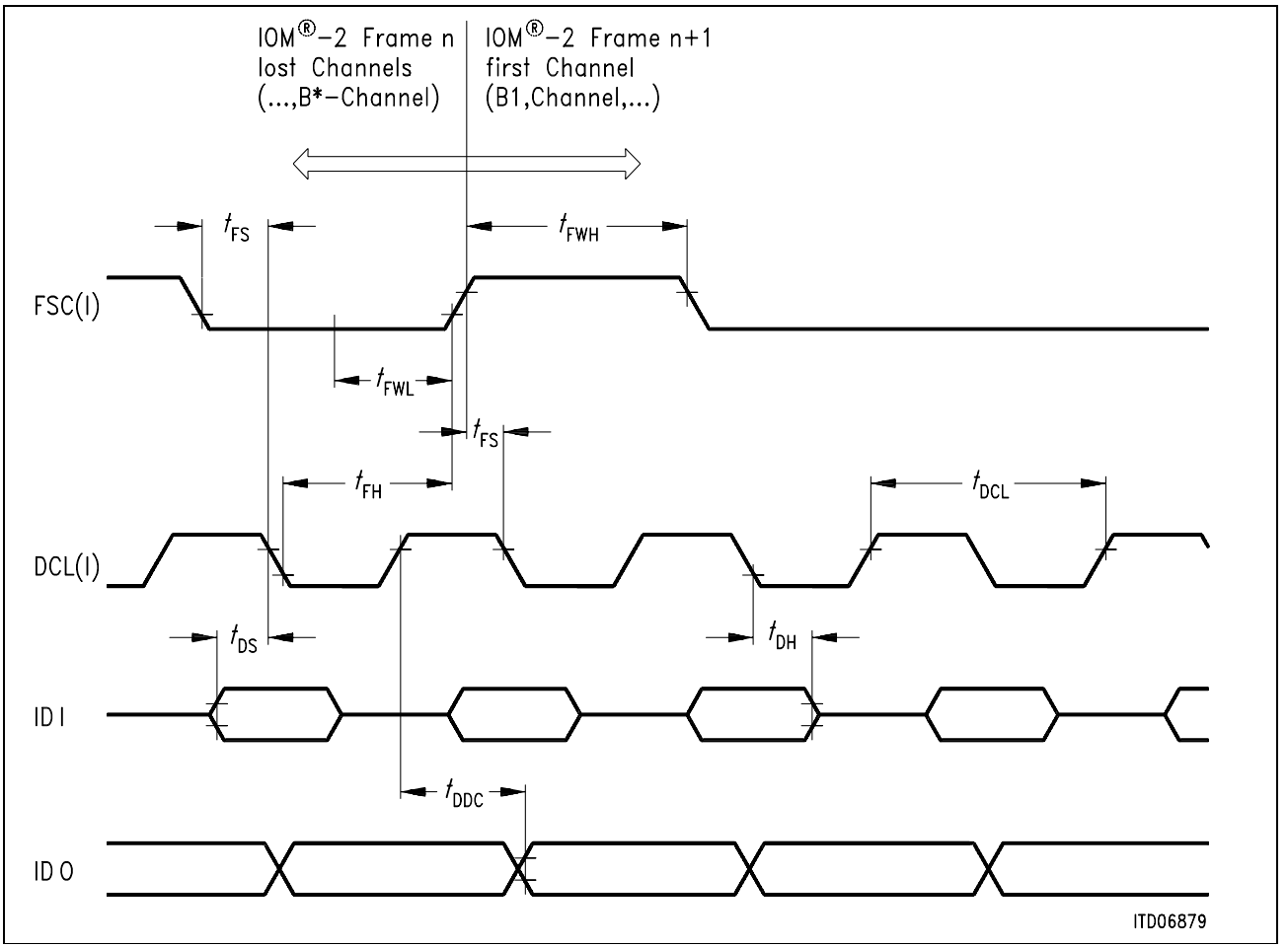


Figure 34
IOM®-2 Interface Timing with Single Data Rate DCL

Timing Characteristics of the IOM®-2

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Frame sync. hold	t_{FH}	30			ns	
Frame sync. setup	t_{FS}	70			ns	
Frame sync. high	t_{FWH}	130			ns	
Frame sync. low	t_{FWL}	t_{DCL}				
Data delay to clock	t_{DDC}			100	ns	
Data delay to frame[1)]	t_{DDF}			150	ns	
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

Note: 1) $t_{DDF} = 0.5\ t_{DCL} + t_{DDC} - t_{FH}$

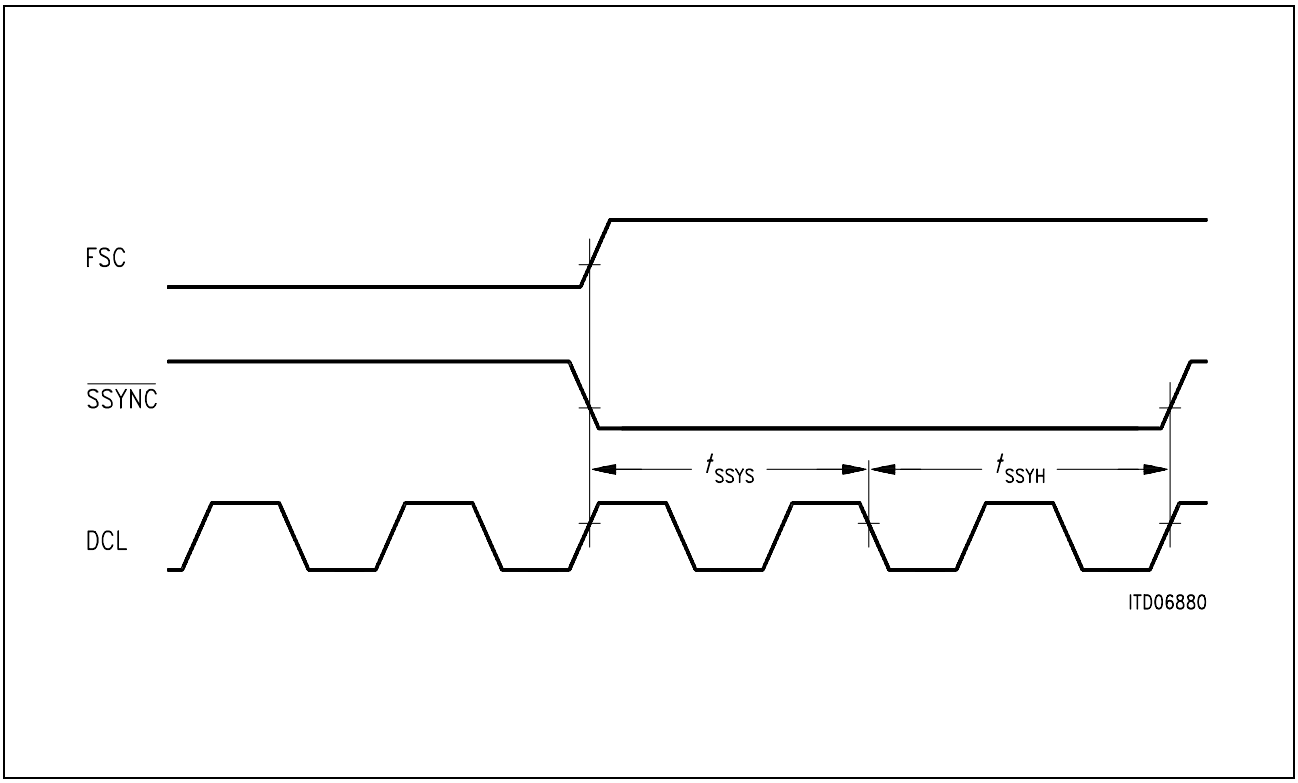


Figure 35
$\overline{\text{SSYNC}}$ Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Superframe sync. setup	t_{SSYS}	200		ns
Superframe sync. hold	t_{SSYH}	200		ns

5.8 Timing of Boundary Scan Test Interface

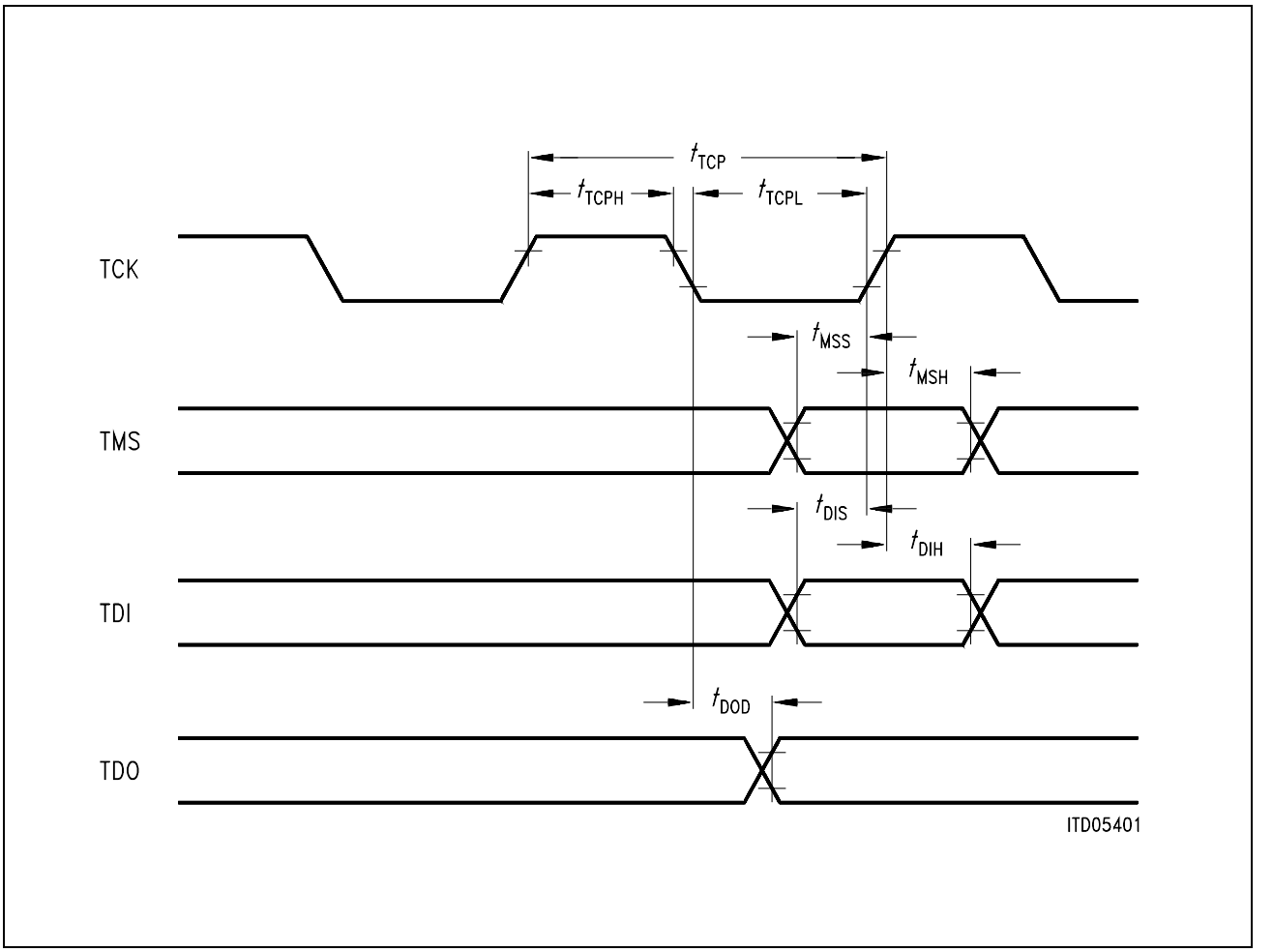


Figure 36
Boundary Scan Test Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Test clock period	t_{TCP}	160		ns
Test clock period low	t_{TCPL}	80		ns
Test clock period high	t_{TCPH}	80		ns
TMS setup time to TCK	t_{MSS}	30		ns
TMS hold time from TCK	t_{MSH}	30		ns
TDI setup time to TCK	t_{DIS}	30		ns
TDI hold time from TCK	t_{DIH}	30		ns
TDO valid delay from TCK	t_{DOD}		60	ns

5.9 Transceiver Characteristics

The transceiver comprises the transmitter output stages, the differential-to-single ended receiver input stage, the loop switch, the peak detector, and the threshold comparators.

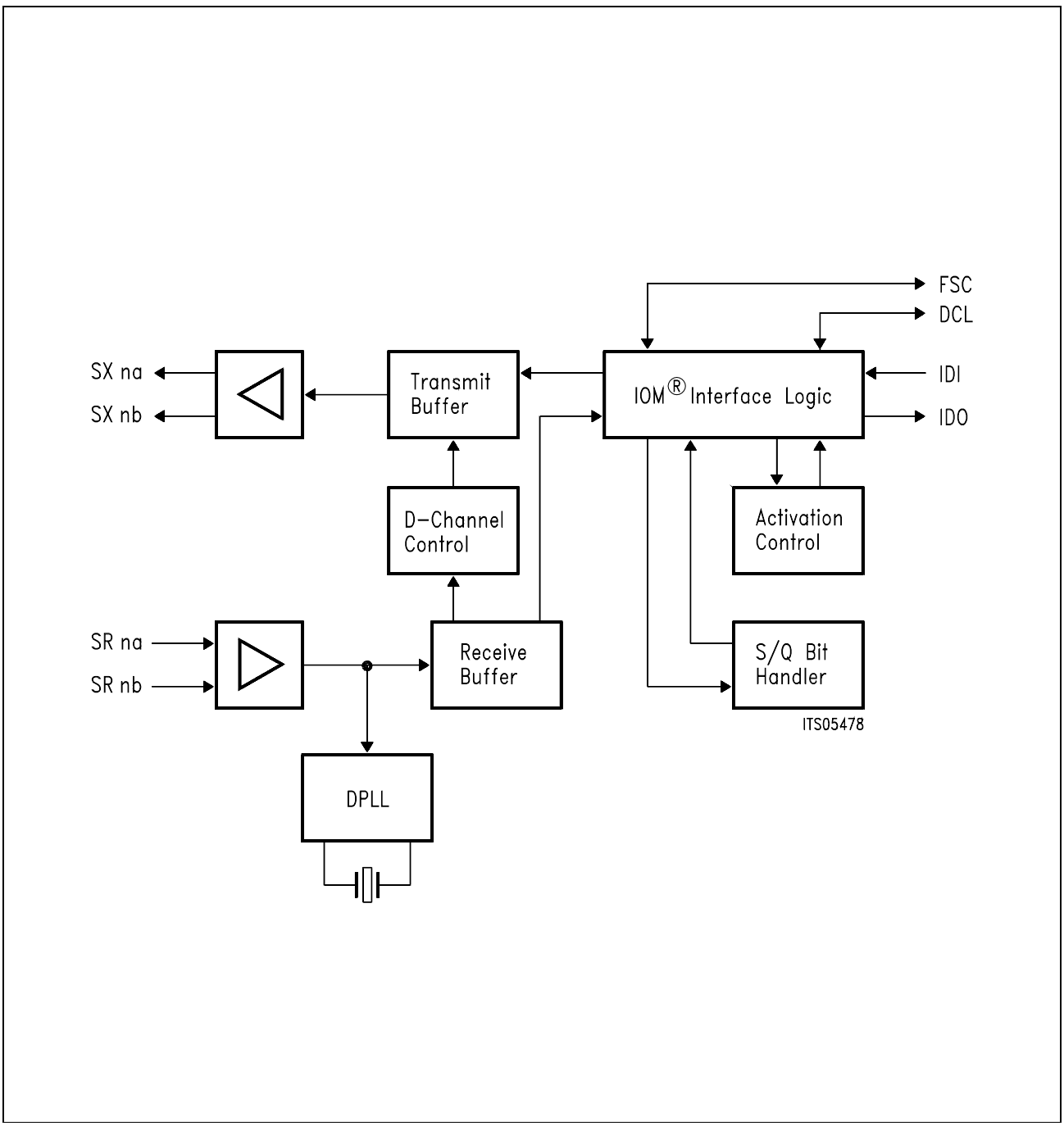


Figure 37
Transceiver Architecture of one S/T-Channel

When transmitting a binary ZERO, the transmitter output is ± 2.1 V (difference between SXna and SXnb), when transmitting a binary ONE, it is tristate. The receiver input range is ± 2.5 V to ± 85 mV, the latter being a hardwired minimum peak level.

Transmitter Performance

Cable 0.6 mm, 120 nF/km

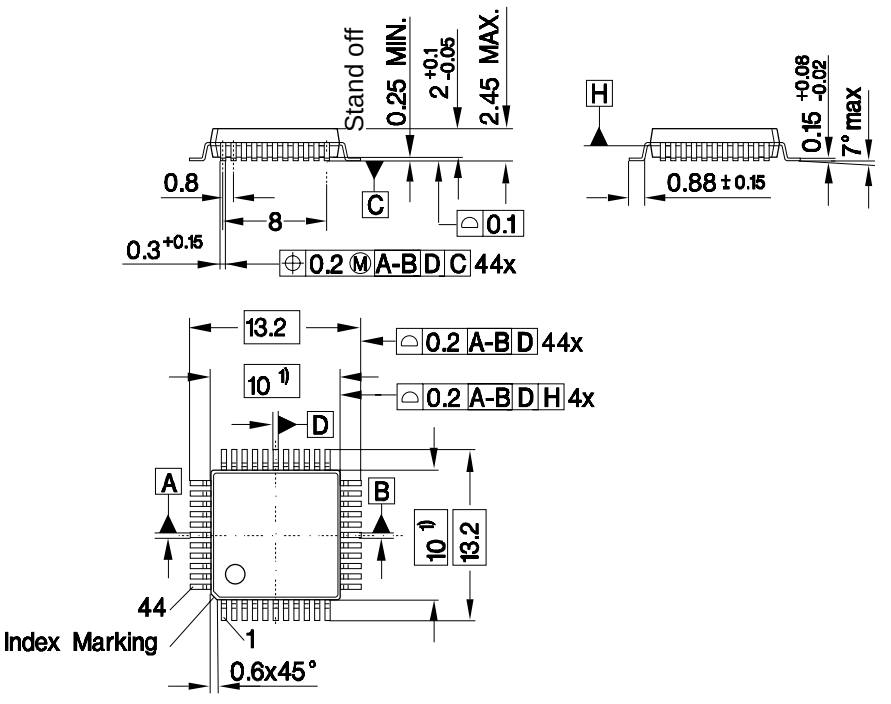
Configuration	Condition	Distance TE-TE	Distance TE-NT/LT
Point-to-point	no noise	–	980 m
	200 / 2000 kHz 100 mVpp	–	940 m
Ext. passive bus	no noise	120 m	720 m
(Roundtrip < 2 µs)	200 / 2000 kHz 100 mVpp	120 m	540 m

Cable 0.6 mm, 30 nF/km

Configuration	Condition	Distance TE-TE	Distance TE-NT/LT
Point-to-point	no noise	–	> 1500 m
	200 / 2000 kHz 100 mVpp	–	> 1050 m
Ext. passive bus	no noise	> 250 m	> 1250 m
(Roundtrip < 2 µs)	200 / 2000 kHz 100 mVpp	> 250 m	> 800 m

6 Package Outlines

Plastic Package, P-MQFP-44-2
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05622

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

7 Appendix

List of Transformer Manufacturers and S_0 Transformers

The following list contains transformers recommended by different manufacturers for use with Siemens S_0 transceivers.

Transformers marked with * have been tested in Siemens S evaluation boards and have shown positive test results concerning pulse shape and impedance requirements of ETS 300 012.

Manufacturers	Transformers
APC	
	APC 2040 S
	APC 1020 S
	APC 3060 S
	APC 9018 D
	APC 3366 D
Pulse Engineering	
	PE-68975*
	PE-64995
	PE-65495
	PE-65795
	PE-68995
S + M Components	
	B78384-A1060-A2*
	B78384-P1111-A2
Vacuumschmelze VAC	
	T60403-L4025-X021*
	T60403-L4097-X011*
	T60403-L5051-X006*
	T60403-L4021-X066
	T60403-L4025-X095
	T60403-L4097-X029
	T60403-L5032-X002
VALOR	
	PT 5001
	PT 5069
	ST 5069
VOGT	
	543 21 002 00*
	543 21 004 00*