ICs for Communications

Very High Bitrate Digital Subscriber Line Chipset

VDSL-A/-D/-L

PEB 22810 Version 2.1

PEB 22811 Version 2.1

PEB 22812 Version 2.1

Product Overview 11.99 DS 1

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1 Overview

1.1 General Description

The Infineon Technologies POTSWIRE™ VDSL chipset is a highly integrated solution for very flexible VDSL systems and other high speed modem and DSL products. It consists of the data pump PEB 22812, the analog chip PEB 22811 and the line driver PEB 22810. Based on a QAM line code the chipset complies with the ETSI VDSL requirements and the evolving ETSI, ITU and ANSI standards. It excellently deals with POTS/ISDN services on the same twisted pair and is compatible with xDSL services in the same multi-cable and with amateur radio. Symmetric data rates of up to 14.6 Mbit/s and asymmetric data rates of up to 26 Mbit/s downstream and 3.25 Mbit/s upstream can be provided. The modem chipset can be used in the exchange or cabinet and in the network termination unit (NT). The VDSL chipset and its interfaces are shown in figure 1.

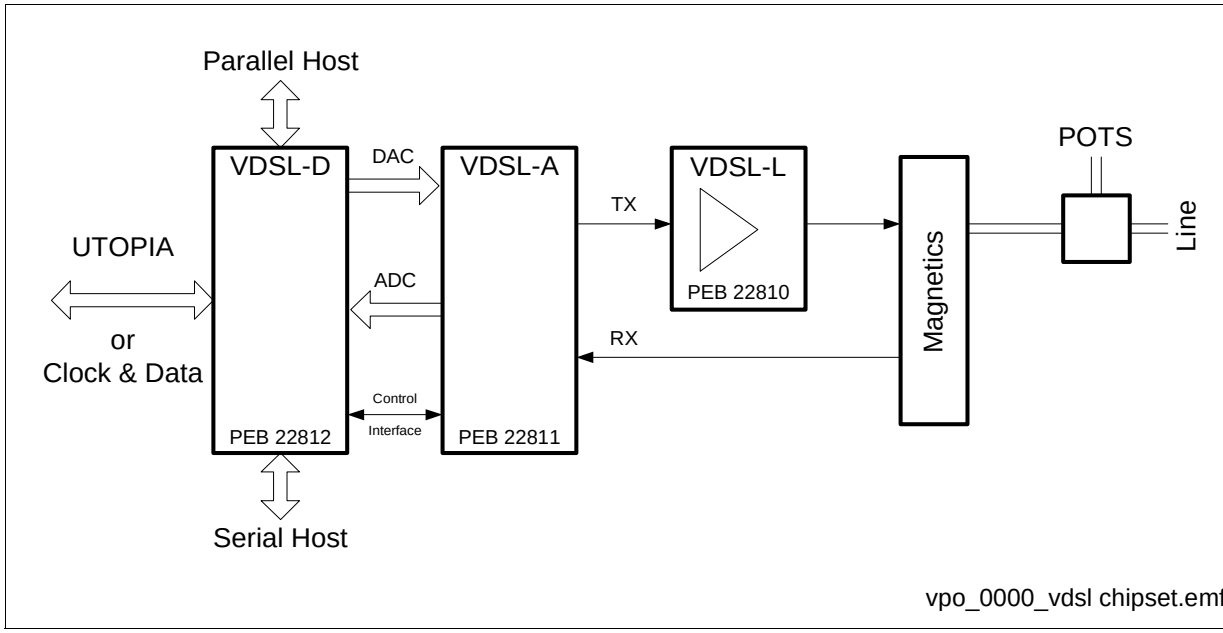

Figure 1 VDSL Chipset

With its integrated microcontroller the chipset is able to perform all of the link control functions. It can however be controlled by an optional external host which can access the modem's registers via a parallel or serial interface. The chipset provides a UTOPIA level 1 master or UTOPIA level 2 slave interface for ATM applications and a clock&data interface which can be used as a general interface .

1.2 System Features

- Complete chipset for VDSL modems and high speed modems
- Compliant with requirements from ETSI TM6, ANSI T1E1.4, and FSAN
- Quadrature Amplitude Modulation (flexible constellations: QAM4-QAM256)
- Frequency Division Duplexing (FDD)
- Bandwidth up to 30 Mbit/s supported
- Spectral compatibility with POTS/ISDN, ADSL, HDSL and SDSL systems and narrowband interferers
- Amateur radio and RFI compatible with programable transmit notches
- Flexible carrier frequencies and bit rates
- Power boost option for extended reach
- Blind modem timing recovery and equalization
- Power down mode combined with warmstart capability (less than 100 ms startup time)
- Embedded microcontroller and internal communication channel for stand alone operation
- Integrated SRAM for interleaving
- Integrated DCXO
- Master (LT) or slave (NT) operation selectable
- Optimized solution for ATM based networks (full UTOPIA)
- Clock & data interface (PMTC interface)
- Low power consumption (1.3 W total for modem)
- Supply voltage +/- 5V and 2.0/3.3V
- Reach of up to 1.5 km with maximum bit rate, longer distances at reduced bit rates

1.3 Applications

- VDSL application according to VDSL standard and FSAN requirements in CO and NT
  - Fast internet access
  - Video on Demand
  - Remote LAN connection
  - Teleworking
- Infrastructure
  - Upgrade of T1/ E1 connections
  - connection of wireless basestations
  - Fiber extension
- High speed Ethernet modems
  - Ethernet connection and Video on demand in hotels
  - LAN to LAN connection

1.4 VDSL Frequency Bands and Performance

The VDSL chipset is very flexible and can operate with different line rates and various constellations at programmable center frequencies. It therefore allows to support spectral compatibility with POTS/ISDN (in same cable), xDSL, ISDN PRA (in same bundle) and amateur radio interferers if needed.

Bitrates between 1.5 and 26 Mbit/s are supported. Examples for payload rates:

- 12.96 Mbit/s VDSL-FSAN system and ANSI medium range symmetric service.
- Symmetric 9.72 Mbit/s for ETSI S2 rate (Payload of 4xE1)
- Asymmetric operation of 25.92/3.24 Mbit/s for ANSI medium range service.
- Multiple T1/E1.
- 10 Mbit/s for Ethernet applications.

1.5 Features VDSL-D

TQFP-144

- Supports the evolving ETSI, ANSI and ITU standards for the copper local loop.
- Full UTOPIA interface to standard ATM components.
- Clock&Data interface
- Supports operation with POTS/ISDN traffic existing over the same pair.
- Symmetrical data transmission at bit rates from 1.5 Mbit/s up to 14.6 Mbit/s
- Asymmetrical data transmission at bit rates up to 25.92 Mbit/s downstream and 3.24 Mbit/s upstream
- Bit Error Rate of less than 10^{-7} with noise margin of 6 dB.
- Flexible constellations: QAM 4 - QAM 256
- Transmit notching for amateur radio band compatibility
- Robust operation on severely distorted lines and narrowband interference.
- Blind modem timing recovery and equalization
- Single latency – with or without programmable latency.
- Integrated interleaver with internal SRAM
- On-chip Reed-Solomon FEC.
- Near-end and far-end loopback capability.
- Operate as slave (NT) or master (LT) according to configuration mode.
- Internal processor for stand alone operation and monitoring.
- Embedded communication channel between the peer controllers in both sides of the link.
- Includes parallel interface to external host and serial interface to standard PC.
- Low power consumption: 0.3W at symmetric 10 Mbps
- 2.0/3.3 Volt supply
- P-TQFP144 packaging
- IEEE 1149.1 JTAG test access port

Type	Package
PEB 22812	TQFP-144

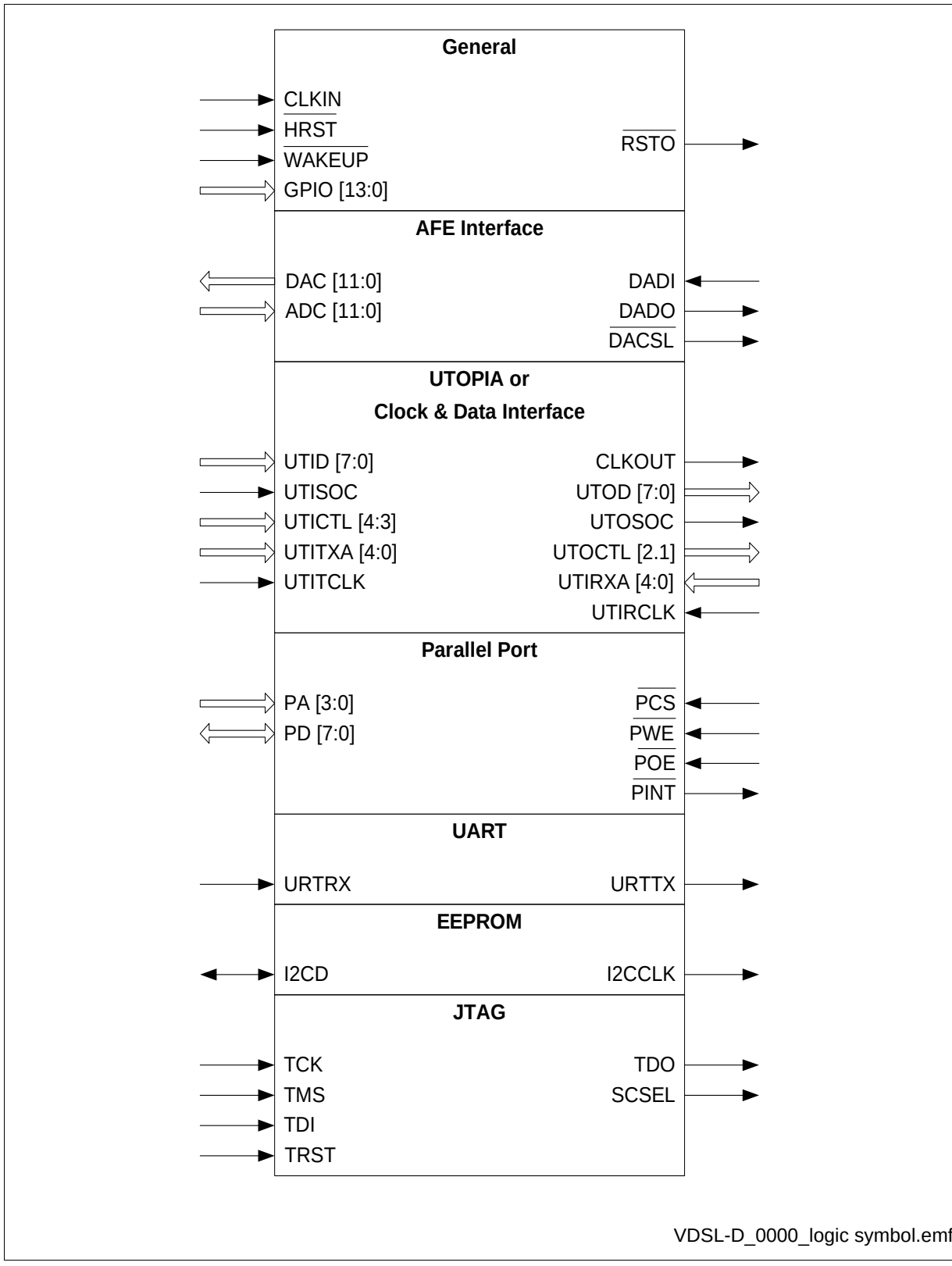

Figure 1 Logic Symbol VDSL-D

1.6 Features VDSL-A

P-MQFP 64

- Configurable for central office/ONU and NT side
- All operating modes of VDSL-D supported
- Symmetric data rates of up to 14.6 Mbit/s
- Asymmetric data rates of up to 25.92 Mbit/s downstream and 3.24 Mbit/s upstream
- 12 bit digital-to-analog converter
- 11 bit analog-to-digital converter (16 bit dynamic range with variable gain amplifier)
- Internal anti-aliasing filter and smoothing filter - programmable corner frequency
- Digital controlled crystal oscillator (DCXO) for timing recovery
- Power management for optimizing transmit PSD
- Variable Gain Amplifier for Automatic Gain Control
- PSD mask requirements of ETSI TS 101 270-1 supported
- PSD mask is designed to achieve spectral compatibility with with xDSL Systems, ISDN and narrowband interferers
- Low power consumption: 700 mW
- Single +5 V supply
- Power down modes supported
- P-MQFP64 package

Type	Package
PEB 22811	P-MQFP 64

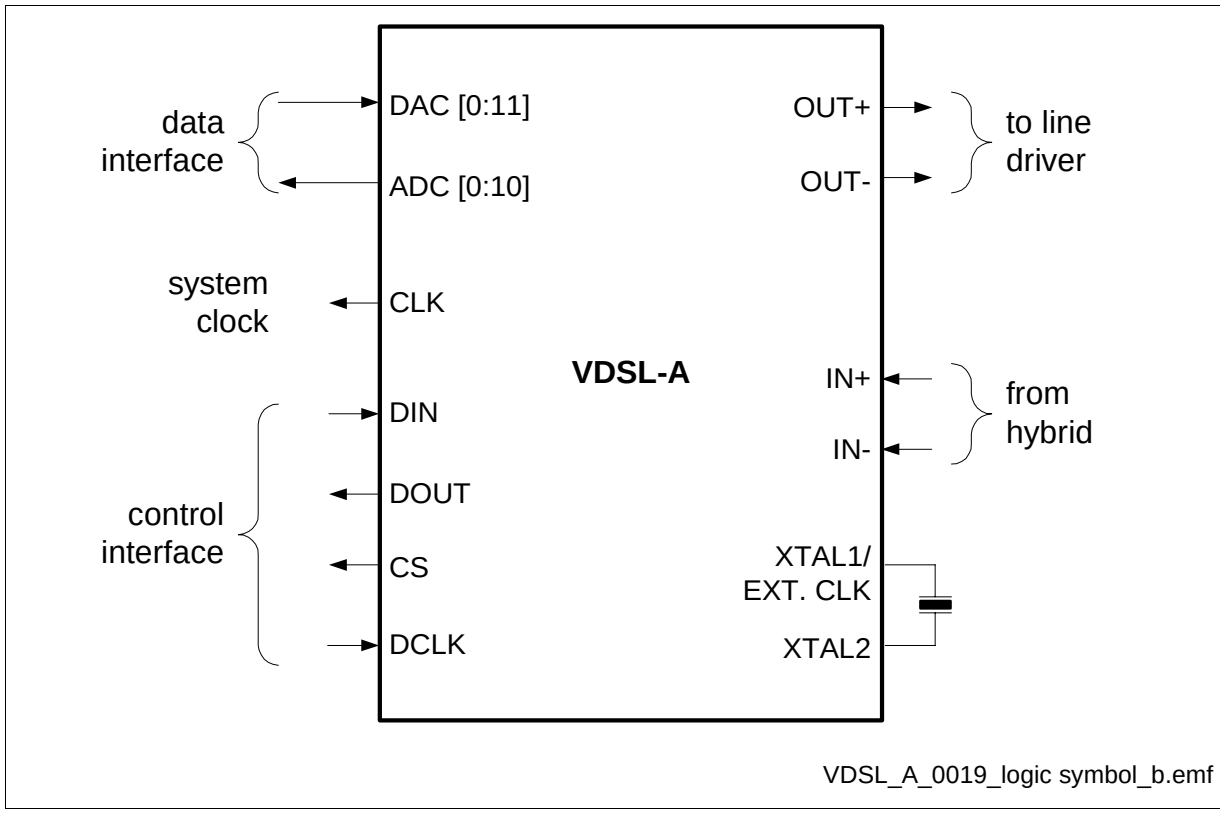

Figure 2 Logic Symbol VDSL-A

1.7 Features VDSL-L

P-DSO-8-1

- Line Driver for Very-high bitrate Digital Subscriber Line (VDSL) Systems and High-Speed Modems for NT and LT
- Configurable as one differential driver or two single-ended drivers
- +/- 5V supply voltage
- 14 V_{p-p} differential voltage swing at +/-5V
- Input level shifter for common mode suppression
- 280 mW power dissipation at +/- 5V supply
- 10 dBm transmit power on the line at +/- 5V
- -50 dB Total Harmonic Distortion at f = 8 MHz, V_{pp} = 14 V, 80 Ohm
- 150 MHz bandwidth (-3 dB), R_L = 80 Ohm
- Unity gain stable
- P-DSO-8-1 package

Type	Package
PEB 22810	P-DSO-8-1

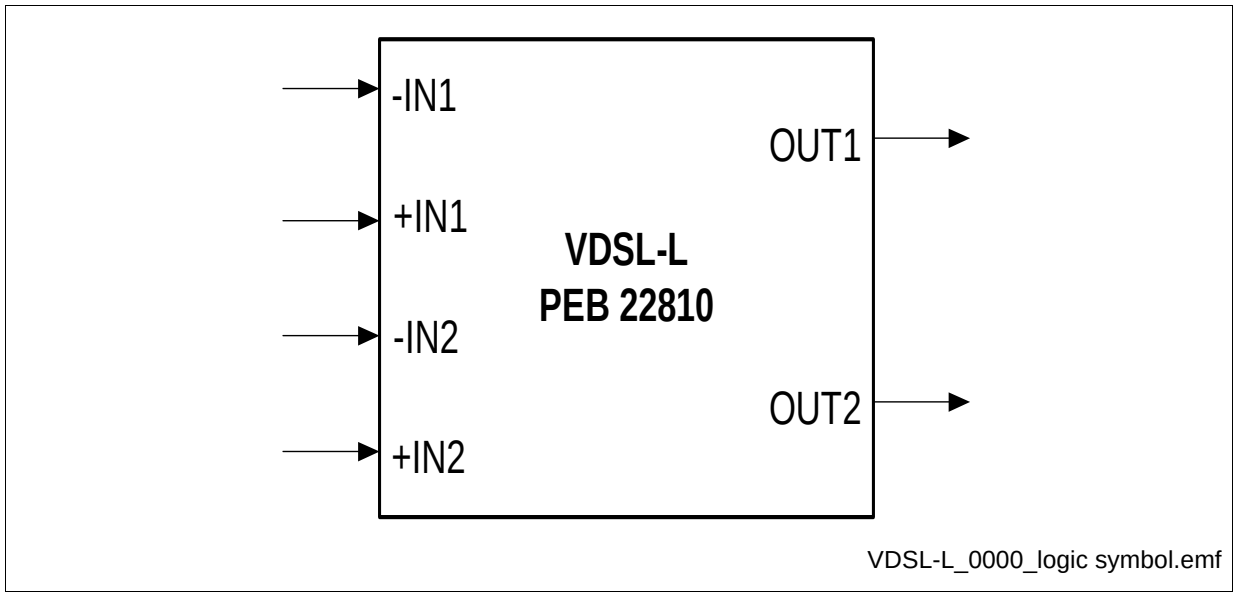

Figure 3 Logic Symbol VDS,L-L

2 VDSL Digital IC (VDSL-D)

2.1 Functional Description

The digital sections of the VDSL modem are implemented in the VDSL-D. These include the digital functions of the Physical Medium Dependent (PMD), the Transmission Convergence (TC) layer functions, the application independent transmission convergence functions (PMS-TC) and the transmission convergence functions (TPS-TC).

The digital functions of the ***PMD*** include the QAM modem core and the interface to the analog front end VDSL-A. The modem core mainly includes timing recovery, and automatic gain control (AGC) support, transmit and receive filters, a linear equalizer and a decision feedback equalizer.

The ***TC*** layer functions are divided into two parts. One part is the **PMS-TC** (Physical Medium Specific-TC). The PMS-TC functions are data randomizing, Reed Solomon forward error correction, data interleaving and payload framing.

The second part of the TC is the **TPS-TC** (Transport Protocol Specific-TC) which is application specific and is used to adapt the user application and payload to the format of the VDSL modem. One of two interfaces is available to the user. The ATM TPS-TC function supports the transfer of ATM cells in the user payload of the modem. A UTOPIA interface is used to connect to external system elements such as the Segmentation and Reassemble (SAR) device. The second TPS-TC is a general purpose interface. A clock&data interface is provided for the connection to external devices.

The VDSL-D has an embedded controller that performs the control and management functions of the VDSL modem. The VDSL-D is able to operate independently without intervention from an external host. The chipset can however be controlled by an optional external host via the parallel or the serial interface.In stand alone mode, all modem configurations (i.e. rates, frequencies) can be saved in an external EEPROM that is controlled by the VDSL-D. In host mode, either the EEPROM or the host can save the modem configurations.

The functional block diagram of VDSL-D is shown in Figure 2.

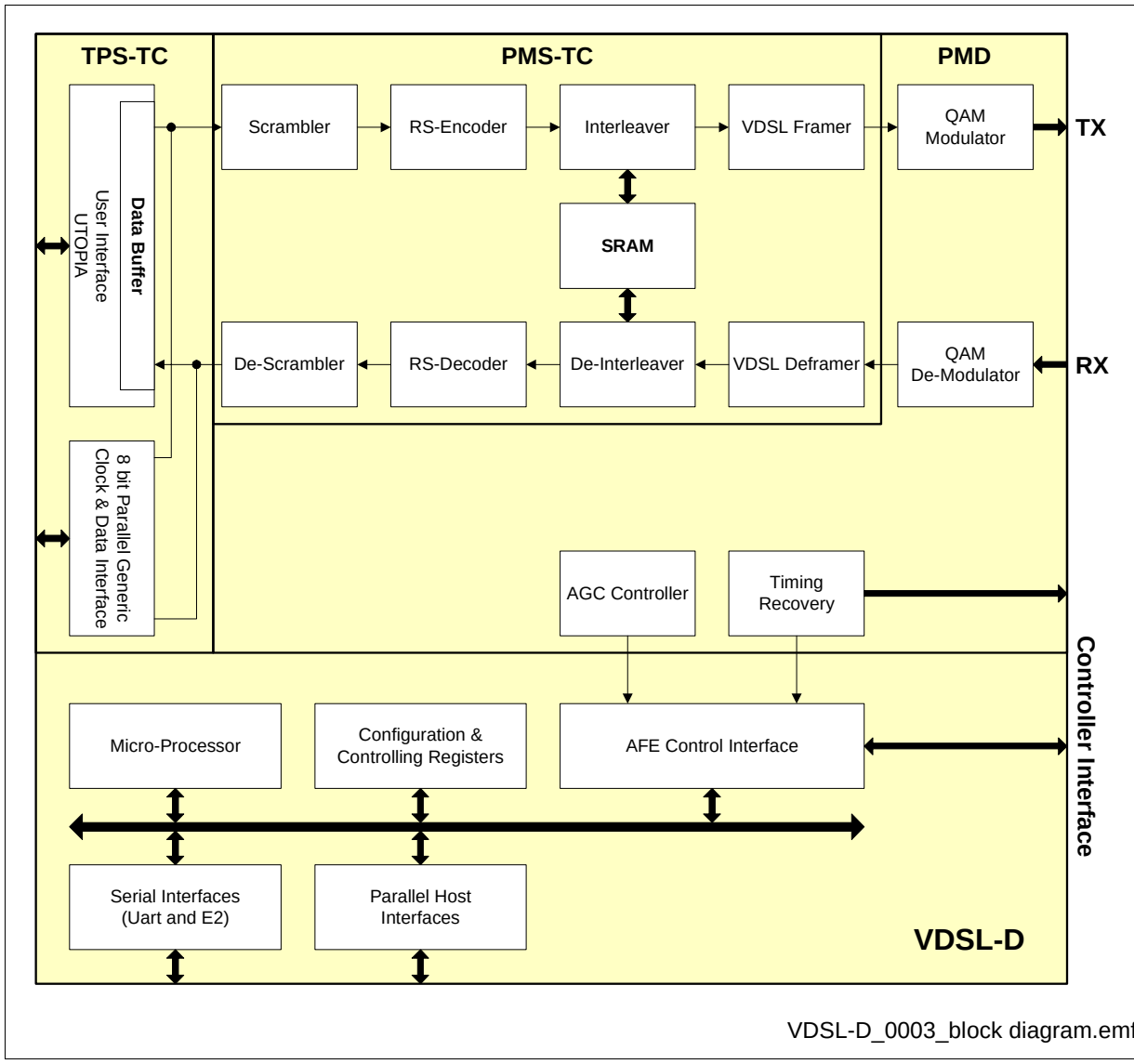

Figure 4 VDSL-D block diagram

2.1.1 Transmit Path

User Data Interface (TPS-TC)

The user data interface provides the UTOPIA (Universal Test & Operation Physical Interface for ATM) for ATM cell transmission and a clock&data interface. The UTOPIA interface can be configured as a level 2 slave with 5 address lines or as a level 1 master with control of 1 slave component .The HEC (Header Error Correction) is computed and written to byte 5 of the 53 byte ATM cell. The interface operates in cell mode at rates of up to 33 MHz with an 8 bit wide data path. The clock&data interface provides a full duplex connection to external interface devices.

Data Buffer (TPS-TC)

A data buffer of 4 cells is provided for rate adaptation between the user interface and the modem. An external buffer will be required in the ATM chip sets if the user applications do not operate at the rate of the VDSL line.

Scrambler (PMS-TC)

A scrambler is used for data randomization required by the VDSL modem. Scrambling generates a statistically balanced bit stream.

RS-Encoder (PMS-TC)

A Reed Solomon forward error correction (RS-FEC) encoder protects payload and header transmission and corrects up to 8 bytes in every codeword of 237 payload bytes.

Convolutional Interleaver (PMS-TC)

Convolutional interleaving of the protected payload is done for protection from impulse noise. The range of protection is programmable with a consequential delay added to the inherent delay of the modem (programmable latency mode). The VDSL-D has an *internal SRAM* to hold the intermediate interleaver and deinterleaver data.

VDSL Framer (PMS-TC)

A VDSL Framer provides VDSL framing, including user payload encapsulation and overhead insertion.

QAM Modulator (PMD)

The QAM core’s task is to do QAM modulation according to the programmed modulation scheme and frequencies.Transmit notching is implemented for amateur radio compatibility

2.1.2 Receive Path

The receive path of the VDSL-D includes the following functions:

QAM Demodulator (PMD)

The QAM demodulator works according to the programmed modulation scheme and frequencies using digital filters and blind equalization.

VDSL Deframer (PMS-TC)

This unit performs VDSL frame extraction, including user payload and overhead extraction.

Convolutional Deinterleaver (PMS-TC)

Convolutional de-interleaving of the protected payload is done in this section.

RS-Decoder (PMS-TC)

Reed Solomon FEC decoding for correction of up to 8 bytes in every codeword of 237 payload bytes.

Descrambler (PMS-TC)

The descrambler is used to recover randomized data.

Data Buffer (TPS-TC)

A data buffer of 128 cells is provided for rate adaptation between the user interface and the modem. An external buffer will be required in the ATM chip sets if the user applications do not function at the rate of the VDSL line.

User Data Interface (TPS-TC)

The user data interface works as described in the transmit direction.

AGC control (PMD)

The AGC controller adapts the power, which depends on the line length, to the ADC input. The internal processor calculates the receive signal characteristics and uses this calculation to control the variable gain amplifier of the VDSL-A.

Timing Recovery (PMD)

In slave mode the timing recovery unit extracts the clock from the receive signal and generates the sampling clock within a timing recovery loop.

2.2 Interfaces

UTOPIA

The Universal Test & Operation Physical Interface for ATM (UTOPIA) provides the interface between the physical layer (PHY) of the digital IC and the ATM layer. The UTOPIA interface can be configured as a level 2 slave with 5 address lines or as a level 1 master with control of 1 slave component. The HEC is computed and written to byte 5 of the 53 byte ATM cell. The interface operates in cell mode at rates of up to 33 MHz with an 8 bit wide data path.

Clock&Data Interface

The clock&data interface provides a full duplex connection to external devices.

Parallel Host Interface

This interface is used to control the modem, to change internal parameters and registers and for debugging purposes.

Serial Host Interface

The serial host interface has the same functions as the parallel host interface, but can be accessed by any standard PC or microcontroller.

VDSL-A Interface

The interface to the VDSL-A includes a data interface and a control interface. The data signals are required for interfacing the DAC and ADC in the VDSL-A. The control interface is used for VDSL-A register access, DCXO-control for timing recovery, AGC and power management.

EEPROM Interface

The VDSL chipset can be connected to an external EEPROM in which modem configuration information can be saved. The EEPROM is accesible only to the VDSL-D and is maintained automatically by the internal controller.

JTAG Interface

The VDSL chipset supports chip level and board level testing (boundary scan, self tests etc). Therefore a standard IEEE 1149.1 JTAG interface is implemented.

2.3 Embedded Controller

The VDSL-D has an embedded controller that controls the operation of the modem and performs the commands generated by the host via the host interface. The modem controller can communicate with the peer controller on the opposite side of the VDSL link via the embedded message channel, which is part of the VDSL overhead. The embedded controller allows stand alone operation.

2.4 Operating Modes

The VDSL chipset in general can operate in one of two basic modes, ***LT mode*** for use in the exchange or cabinet, or ***NT mode*** for use in the NT unit.

The frequency band allocation, the baud rate and the QAM constellations are programmable.

The application interface can be programmed as a UTOPIA bus for ATM applications or as a clock and data interface for general purpose applications.

3 VDSL Analog IC (VDSL-A)

3.1 Functional Description

The analog front end of the VDSL modem is implemented in the PEB 22811. It consists of the digital-to-analog and the analog-to-digital converters, the reconstruction and the anti-aliasing filters (PREFI/POFI), the power contol unit, the variable gain ampifier and the interfaces to the datapump PEB 22812. A digitally controlled crystal oscillator (DCXO) is included for clock generation and timing recovery. Therefore the VDSL chipset only needs a simple crystal and not an expensive external VCXO. The VDSL-A can be used in the exchange or cabinet and in the NT unit.

The block diagram of the VDSL Analog IC is shown in Figure 3.

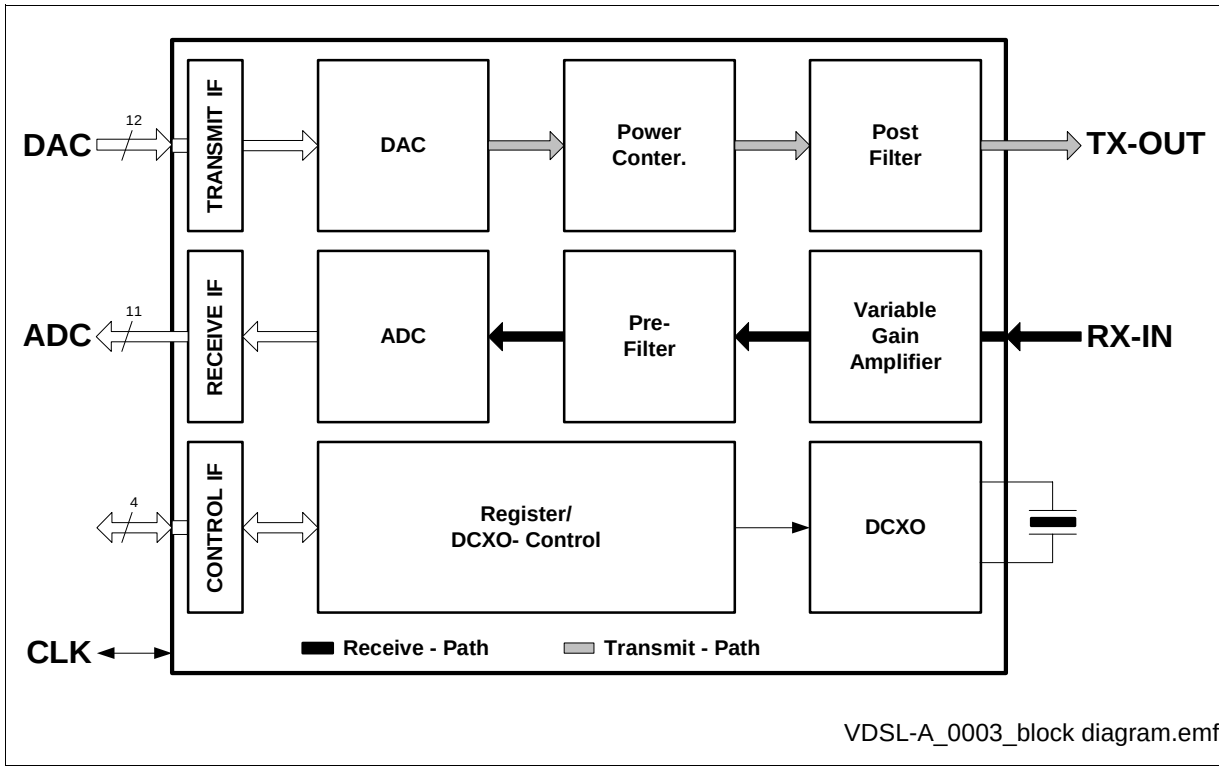

Figure 5 VDSL-A block diagram

3.1.1 Transmit Path

Digital-to-Analog Converter (DAC)

For digital-to-analog conversion a converter with a resolution of 12 bits is implemented at sampling frequencies up to 30 MHz.

Power Controller

Power management is done by a power control unit in order to optimize the transmit power for different loop lengths.

In upstream direction a VDSL modem located rather close to the cabinet causes strong far end crosstalk (FEXT). In that case the power control unit may be used to reduce power in 1 dB steps.

Power management functionality enables the modem to optimize the power for balanced performance between the upstream and downstream while reducing crosstalk between systems.

A power boost option is provided by the line driver.

Postfilter

The postfilter (reconstruction filter) is a filter with a programmable corner frequency (6...10MHz). In upstream direction an external filter can be used for compliance with the ETSI PSD-mask (out of band noise). In downstream direction no external filter is needed.

3.1.2 Receive Path

Analog-to-Digital Converter (ADC)

The ADC achieves a resolution of 11 bits at sampling frequencies up to 30 MHz.

Prefilter

The prefilter (anti-aliasing filter) is designed to meet the anti-aliasing requirements of the VDSL modem and has the same characteristics as the POFI.

Variable Gain Amplifier (VGA)

The signal power at the input of the ADC is highly dependent on the transmission line length. Therefore AGC (Automatic Gain Control) functionality is needed to adapt the signal to the ADC range. The internal processor of the datapump calculates the characteristics of the receive signal and controls the VGA in the analog front end PEB 22811. The dynamic range of the VGA covers -8.5 to 30 dB. The VGA step size is 0.43 dB.

3.2 Interfaces

Data Interfaces

Glueless data interfaces to the A/D and D/A converters are provided on the PEB 22811 and PEB 22812. The transmit data interface and the receive interface have a width of 12 bits and 11 bits, respectively.

Control Interface

The following information is transmitted via the control interface between VDSL-D and VDSL-A:

- Control data for the DCXO
- General data for VDSL-A operation
- Status monitoring data

3.3 Clock Generation

The system clock is generated by an internal digitally controlled crystal oscillator circuit (DCXO) in VDSL-A. A simple crystal between 12 MHz and 30 MHz has to be connected externally, dependent on the desired mode of operation. The accuracy of the externally connected crystal has to keep +/-50 ppm.

When the VDSL system is operating in LT mode (master mode), the DCXO is used as a masterclock. In NT mode (slave mode), a timing recovery loop (digital PLL) is controlled by the digital IC VDSL-D. The control data are sent to the integrated DCXO of VDSL-A. The tuning range is +/-150 ppm. The DCXO resolution is 2 ppm and can be enhanced by the switching mode.

4 Line Driver (VDSL-L)

The block diagram of the VDSL Line Driver IC is shown in Figure 4.

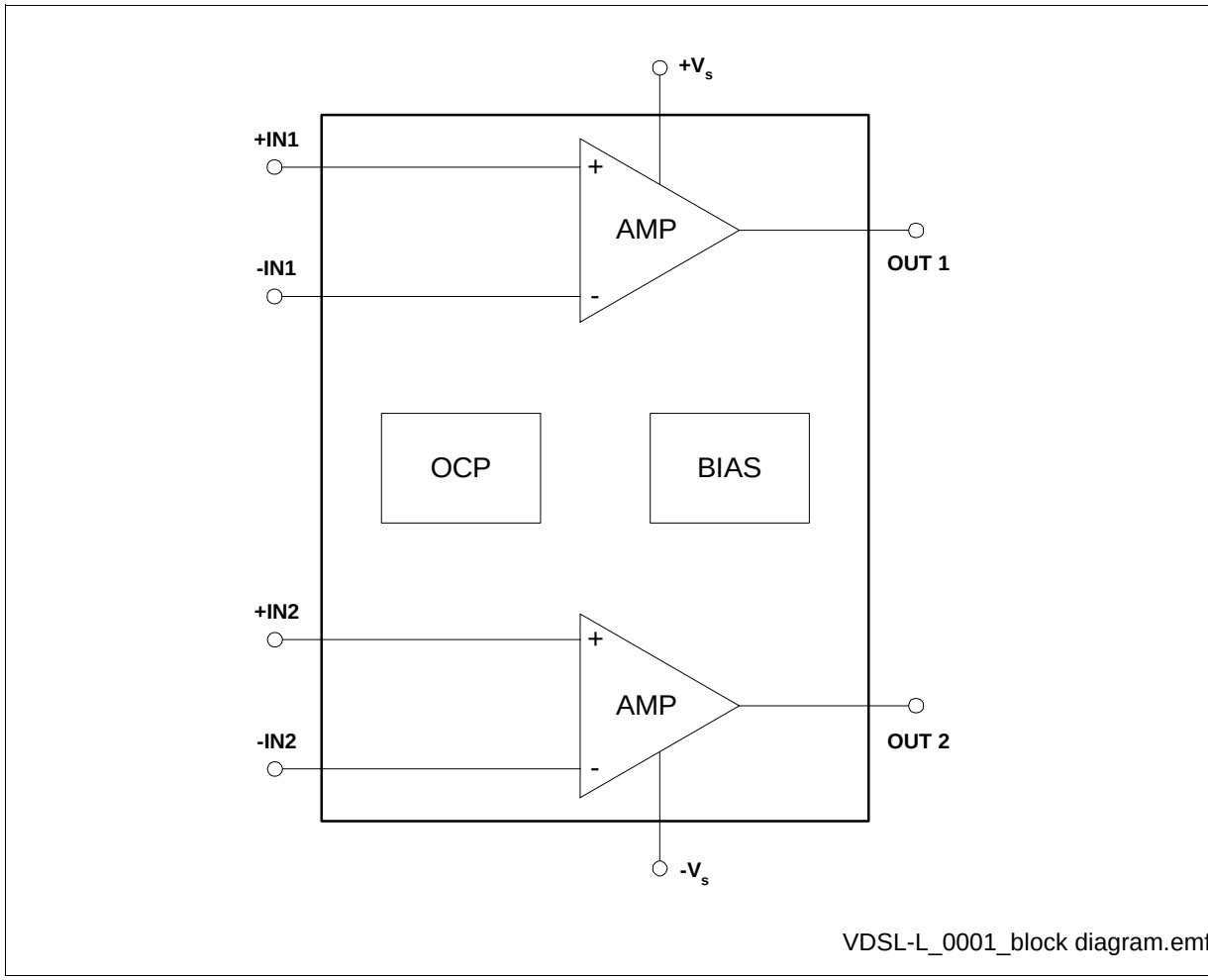

Figure 6 VDSL-L Block Diagram

The PEB 22810 line driver has a maximum transmit power of 11.5 dBm at 80 Ohms and a power dissipation of 280mW. A power-down mode is provided. The line driver is overcurrent protected (OCP unit).

5 Application Notes

Duplex Splitter and POTS/ISDN Splitter

According to FDD (Frequency Division Duplexing) the spectrum of the twisted pair line is split into the transmit and receive band. This is done by a hybrid circuit and by a high-pass or a low-pass according to the line end respectively as shown in figure 8. Additionally the POTS/ISDN services have to be separated by a high-pass and a low-pass as shown in figure 5.

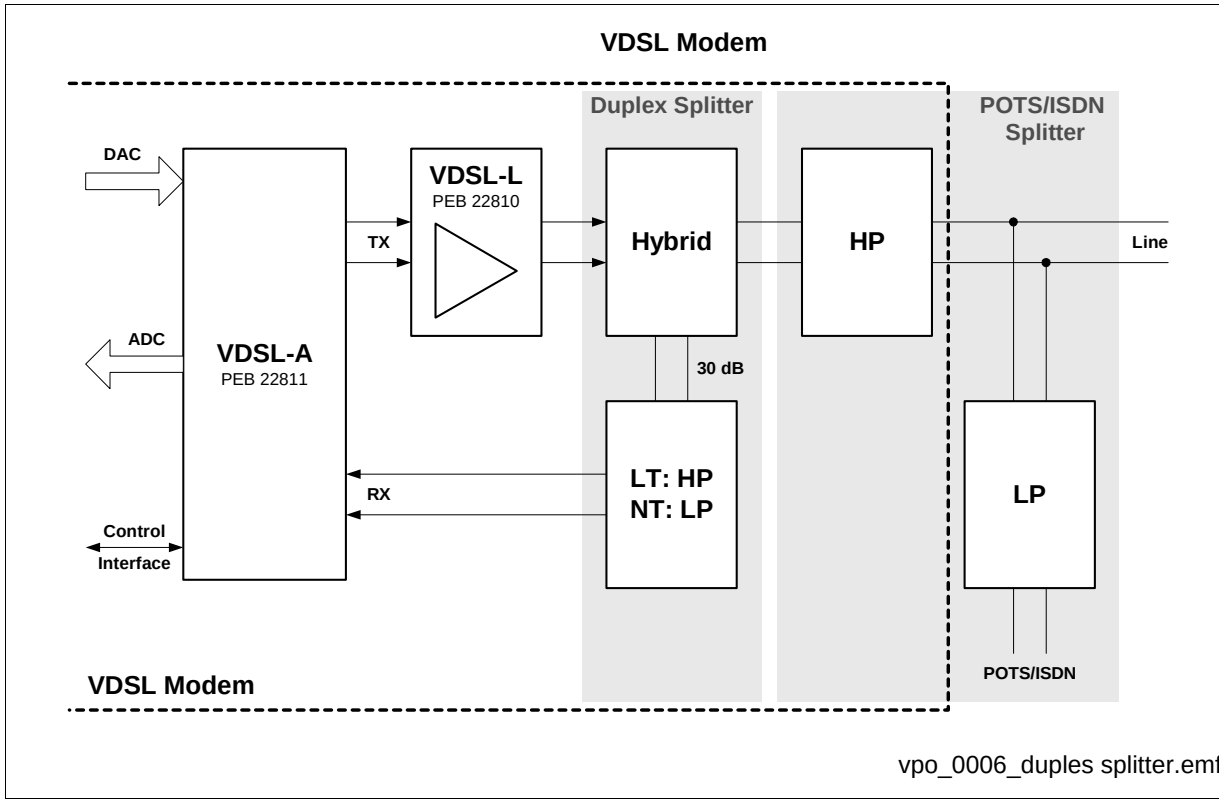

Figure 7 Duplex Splitter and POTS/ISDN Splitter

The system architecture separates the LP and the HP modules of the POTS/ISDN splitter. The LP will physically reside outside the VDSL modem and the HP will physically be part of the VDSL modem.

All of the above mentioned filters are very small in size and only one additional capacitor is used in the system for decoupling the ADC.

6 Glossary

ADC	Analog-to-Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AFE	Analog Front End
AGC	Automatic Gain Control
ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
AWG	American Wire Gauge
BER	Bit Error Rate
CRC	Cyclic Redundancy Check
DAVIC	Digital Audio-Visual Council
DAC	Digital-to-Analog Converter
DCXO	DigitallyControlled Crystal Oszillator
DS	Downstream
ETSI	European Telecommunications Standards Institute
FDD	Frequency Division Duplexing
FEC	Forward Error Correction
FEXT	Far End Crosstalk
FSAN	Full Service Access Network Group
FTTB	Fiber to the Building
FTTC	Fiber to the Curb
FTTCab	Fiber to the Cabinet
FTTEx	Fiber to the Exchange
FTTH	Fiber to the Home
FTTN	Fiber to the Node
HDSL	High Bit-rate Digital Subscriber Line
ISDN	Integrated Services Digital Network
ISDN-BRA	ISDN Basic Rate Access
ISDN-PRA	ISDN Primary Rate Access
LAN	Local Area Network
LT	Line Termination

MAC	Media Access Control
MII	Medium Independent Interface
MQFP	Metric Quad Flat Package
NEXT	Near End Crosstalk
NT	Network Termination
OCP	Overcurrent Protection Unit
ONU	Optical Network Unit
OTP	Overtemperature Protection Unit
PC	Personal Computer
PHY	Physical Layer Interface
PLL	Phase Locked Loop
PMD	Physical Medium Dependent
PMS	Physical Medium Specific
POTS	Plain Old Telephone Service
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
RFI	Radio Frequency Interference
RS	Reed Solomon
RX	Receive Signal
SDSL	Single-Line Digital Subscriber Line
SNR	Signal to Noise Ratio
TC	Transmission Convergence
TX	Transmit Signal
TPS	Transport Protocoll Specific
UTOPIA	Universal Test and Operation Physical Interface for ATM
VCXO	Voltage Controlled Crystal Oscillator
VDSL	Very High Speed Digital Subscriber Line
VDSL-D	Digital Transceiver PEB 22812
VDSL-A	Analog Front End PEB 22811
VDSL-L	Line Driver PEB 22810