Preliminary Product Overview, Rev. 2.0, May 2004

VINETIC®

Voice and Internet Enhanced Telephony Interface Concept

PEB 3324
PEB 3322
PEB 3332
PEB 3320
PEB 3314
PEB 3394
PEB 3304
PEB 4264/-2
PEB 4364
PEB 4265/-2
PEB 4365
PEB 4266
PEB 4262
PEB 4268

Wireline Communications

Infineon technologies

Never stop thinking.

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Preliminary Product Overview

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Page	Subjects (major changes since last revision)
	VINETIC-2CPE added
	Featurelist updated

Preface

This Preliminary Product Overview describes the Voice and Internet Enhanced Telephony Interface Concept (VINETIC®) chip set family. For more VINETIC® related documents, please see our webpage at http://www.infineon.com/vinetic.

To simplify matters, the following synonyms are used:

VINETIC®-x: Synonym used for all codec versions VINETIC®-4VIP, VINETIC®-2VIP, VINETIC®-2CPE, VINETIC®-4C, VINETIC®-4M, VINETIC®-4S, VINETIC®-8S and VINETIC®-8M.

VINETIC®-4x: Synonym used for 4-channel versions of the VINETIC® family. To simplify matters only the 4-channel versions are depicted in this document in most cases.

SLIC: Synonym used for all SLIC versions SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E, SLIC-P, SLIC-LCP and SLIC-DC.

Attention: The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4264) and SLIC-E (PEB 4265) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in the specification, also TSLIC-S and TSLIC-E can be deployed.

Organization of this Document

This Preliminary Product Overview is divided into 11 chapters. It is organized as follows:

- **Chapter 1, Family Overview**
  A general description of the chip set, the key features, and some typical applications.
- **Chapter 2, VINETIC® Host Interface Description**
  Connection information including the different interface types.
- **Chapter 3, Codec/SLIC Features (BORSCHT Functions)**
  The main functions of the chip set are presented with functional block diagrams.
- **Chapter 6, Operating Modes**
  A brief description of the operating modes and the integrated test and diagnostic functions.
- **Chapter 4, Signalprocessing Capabilities of the VINETIC®**
  A short overview of DSP performance necessary for different algorithms.
- **Chapter 5, Programming of the VINETIC®**
  A general description of the *VINETIC®-x* command structure.
- **Chapter 7, Firmware Architecture**
  A general description of the *VINETIC®-x* software system

- **Chapter 8**, **Electrical Characteristics**
  Parameters, symbols, and limit values are provided for the chip set.
- **Chapter 9**, **Application Circuits**
  External components are identified. Illustrations of balanced ringing, unbalanced ringing, and protection circuits are included.
- **Chapter 10**, **Package Outlines**
  Illustrations and dimensions of the package outlines.
- **Chapter 11**, **Terminology**
  List of abbreviations and descriptions of symbols.
- **Chapter 12**, **Index**

Attention: ***This document is a pre release version of the VINETIC® product overview.***

Related Documentation

in preparation

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1 Family Overview

The VINETIC® is a family of devices for analog telephone line provision. VINETIC® devices are available in different granularity (0, 2, 4 and 8 analog voice channels) and also with different levels of DSP performance (VIP, CPE, M, C, S). The seamless connection to a broad range of SLICs provides the most effective solution for a wide range of applications, from high density CO/DLC/PBX linecards to low-cost CPE applications. Significant boardspace reduction can be achieved through the integrated DSP for voice processing and packetization.

The VINETIC® provides system solutions for the following applications:

- Access Network:
  - Central Office - TDM
  - Digital Loop Carrier - TDM, VoATM, VoIP
  - FTTH - TDM, VoATM, VoIP
  - WLL - TDM, VoIP
- PBX:
  - Analog Linecard - TDM, VoIP
- Customer Premises Equipment:
  - Residential Gateway / Home Gateway / Internet Telephony Gateway (ITG) - VoIP
  - Integrated Access Device (IAD) - VoIP, VoATM
  - Cable Modems / Media Terminal Adapter (MTA) - VoIP
  - Analog Telephony Adapter (ATA) - VoIP

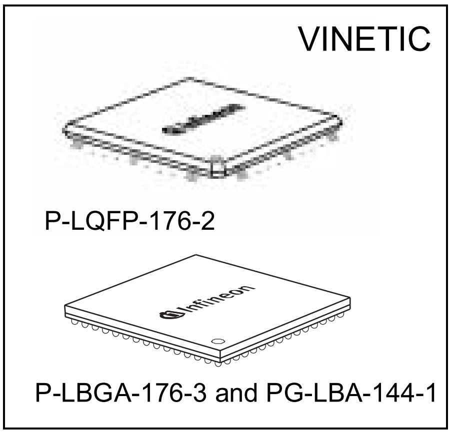
To cover these applications, the VINETIC® devices are pin- and software-compatible, allowing the maximum flexibility while offering the optimized feature set per application.

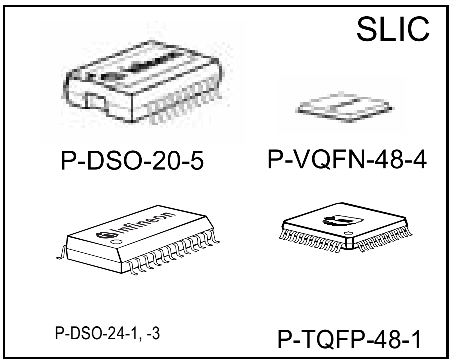
Voice and Internet Enhanced Telephony Interface Concept VINETIC®

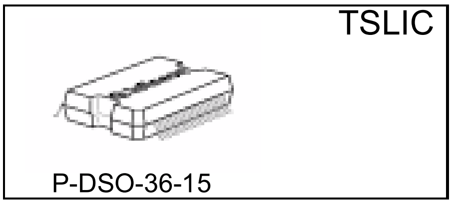
Executive Summary

The VINETIC® family integrates the DSP and RAM for voice processing into the codec/SLIC chip set, thereby offering a unique set of features for voice over packet:

- **Cost and Boardspace Reduction** - codec, DSP and RAM are integrated into one small package providing significant cost and boardspace advantages.
- **Scalability** - VINETIC® supports each voice channel with the necessary amount of DSP performance due to the encapsulation of codec and DSP.
- **Flexibility** - the VINETIC® family offers 2 to 8 analog ports and various level of DSP performance, while remaining pin- and software-compatible.
- **World-Wide-Usage** - The VINETIC® can be adapted to different country requirements without a hardware change (AC and DC path, ringing, metering, etc. are programmable).
- **Future Proof** - the integrated RAM for downloading advanced codecs or Infineon DSP software guarantees that for future remote updates the system will remain state-of-the-art technology.
- Designed for Voice over Packet (**VoIP, VoDSL, Cable, VoATM)**







Type	Package
PEB 3324, PEB 3322, PEB 3332, PEB 3320, PEB 3314, PEB 3394, PEB 3304	P-LQFP-176-2, P-LBGA-176-3, PG-LBGA-144
PEB 4364, PEB 4365	P-DSO-36-15
PEB 4264/-2, PEB 4265/-2, PEB 4266	P-DSO-20-5, P-VQFN-48-4
PEF 4268	P-DSO-24-1, -3, P-TQFP-48-1

Table 1 *VINETIC®-x* Versions

Chip Set[1]	VINETIC®-4VIP	VINETIC®-2VIP	VINETIC®-2CPE	VINETIC®-0	VINETIC®-4M/-8M	VINETIC®-4C	VINETIC®-4S/-8S
Product ID	PEB 3324	PEB 3322	PEB 3332	PEB 3320	PEB 3314/ PEB 3318	PEB 3394	PEB 3304/ PEB 3308
Analog Channels	4	2	2	0	4/8	4	4/8
Echo Cancellation (G.165, G.168)	up to 128 ms	up to 128 ms	up to 16 ms	up to 128 ms	up to 16 ms	up to 16 ms	No
ADPCM (G.726)	Yes	Yes	Yes	Yes	Yes	Yes	No
Complex Voice Codecs (G.723, G.728, G.729)[2]	Yes	Yes	Yes	Yes	No	No	No
Fax Relay T.38	Yes	Yes	Yes	Yes	No	No	No
Signal processing functions[3]	Yes	Yes	Yes	Yes	Yes	Yes	No
AAL2, RTP packetization, Jitter Buffer	Yes	Yes	RTP only	Yes	Yes	No	No
Integrated Code RAM for Firmware Download	Yes	Yes	Yes	Yes	Yes	No[6]	No´[6]
Line testing AITDF[4]	Yes	Yes	GR909 only	Yes	Yes	Yes	Yes
World wide programmability of analog BORSCHT[5] functions	Yes	Yes	Yes	–	Yes	Yes	Yes

1) All 4-, 2- and 0-channel devices are pin- and software compatible, except the VINETIC-2CPE that is optimized for CPE market; for 8-channel codecs contact local sales.

2) Patent indemnification available.

3) e.g. DTMF generation and detection, Caller ID (CLIP) generation (FSK), Universal Tone Detection (UTD), Answering Tone Detection (ATD), Caller-ID detection, Universal Tone Generator (covering Japanese Tones), Call Progress Tone detector.

4) Advanced Integrated Test and Diagnosis Functions.

5) Battery feed, Ringing, Signaling (supervision), Coding, Hybrid for 2/4-wire conversion, Testing, Hook thresholds, Teletax metering.

6) Versions up to v1.4 provide also RAM for firmware download

Table 2 SLIC Versions[1]

Marketing Name	SLIC-S	TSLIC-S	SLIC-S2	SLIC-E	TSLIC-E	SLIC-E2	SLIC-P	SLIC-LCP	SLIC-DC
Product ID	PEB 4264	PEB 4364	PEB 4264 -2[2]	PEB 4265	PEB 4365	PEB 4265 -2[3]	PEB 4266	PEB 4262	PEB 4268
Channels	1	2	1	1	2	1	1	1	1
Internal Ringing	45 Vrms balanced	45 Vrms balanced	45 Vrms balanced	85 Vrms balanced	85 Vrms balanced	85 Vrms balanced	85 Vrms bal., 50 Vrms unbal.	external ringing	DC/DC generator included 60Vrms
Longitudinal Balance	53 dB	53 dB	60 dB	53 dB	53 dB	60 dB	53 dB	60dB with adaption to external compon-ents	48 dB
Maximum DC feeding	32 mA	32 mA	50 mA	32 mA	32 mA	50 mA	32 mA	50 mA	32 mA
Neg. Battery Voltages	2	2	2	2	2	2	2/3	2	0

Table 2 SLIC Versions[1] (cont'd)

Add. positive Voltages	1	1	1	1	1	1	0	0	1 (unreg. 12-35V)
Technology	90 V Smart Power	90 V Smart Power	90 V Smart Power	170 V Smart Power	170 V Smart Power	170 V Smart Power	170 V Smart Power	170 V Smart Power	170 V Smart Power

1) For broadband SLICs for the Infineon ADSL combo solution (Integrated Voice and Data IVD - GEMINAX-S PEB 4561 and GEMINAX-S MAX PEF 55801), please contact local sales.

2) Chip marked as PEB 4264

3) Chip marked as PEB 4265

Table 3 VINETIC® Features

-VIP	-2 CPE	-M	-C	-S	-0	VINETIC® Features
Common Features						
2/4	2	4/8	4	4/8	0	Number of fully programmable codecs with enhanced signal processing capabilities[1]
●		●	●	●	●	Pin-compatible and software compatible
●	●	●	●	●		Glueless interface to Infineon SLICs family: SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E and SLIC-P, SLIC-LCP and SLIC-DC[2], GEMINAX-S, GEMINAX-S MAX
Integrated DSP Features						
						Integrated DSP
●	●	●			●	– with RAM for VoIP/VoDSL/VoATM and software download capability[3]
●	●	●	●		●	– for enhanced signal processing
●	●	●			●	RTP packetization & jitter buffer (adaptive and fixed; 200ms)
●	●	●			●	RTCP support
●		●			●	AAL2 cell generation & jitter buffer (adaptive and fixed; 200ms)
●		●			●	Compatible with ITU-T I.366.2
●	●	●			●	Compatible with RFC 1889 specification
●	●	●			●	Compatible with Packet Cable specification
●		●			●	PacketOverPCM functionality
●	●	●	●	●	●	Integrated DTMF generator
●	●	●	●		●	Integrated DTMF decoder
●	●	●	●		●	Integrated Caller ID (FSK) generator, according to Bellcore 202 and V.23
●	●	●	●		●	Integrated Caller ID (FSK) detector, according to Bellcore 202 and V.23
●	●	●	●		●	Integrated fax/modem detection by Universal Tone Detection unit (UTD), In-band tone detection
●	●	●	●		●	Integrated Universal Tone Generator (UTG) including holwer tone and japanese tone generation
●	●	●	●		●	Call Progress Tone (CPT) Detector
●		●	●	●		Optimized filter structure for modem transmission, enhanced modem performance for improvement of V.90 transmission

Table 3 VINETIC® Features (cont'd)

-VIP	-2 CPE	-M	-C	-S	-0	VINETIC® Features
●	●	●	●		●	Multi-party conferencing
●	●	●			●	3-Party conferencing via packet network
●	●	●	●	●	●	G.711
●	●	●			●	G.711 Annex I (Packet Loss Concealment), G.711 Annex II (VAD + CNG)
●	●	●	●		●	G.726 ADPCM
●	●				●	G.729 A, B
●	●				●	G.723.1
●	●				●	G.728, G.728 Annex I (Packet Loss Concealment)
●	●				●	G.729 E
●	●				●	iLBC[4)]
●	●	●			●	Voice Activity Detection (VAD)
●	●	●			●	Comfort Noise Generation (CNG)
 ● ●	 ●	 ●	 ●		 ● ●	Algorithms for Line Echo Cancellation exceeding G.165, G.168, G.168-2000, G.168-2002: – up to 128 ms tail length – up to 16 ms tail length
●	●	●			●	Voice Play Out (reordering, fixed and adaptive jitter buffer, clock synchronization)
●	●				●	T.38 Fax Relay Support including all required datapump algorithms V.17, V.21, V.27ter, V.29
●	●				●	Text phone support V.18

Codec/SLIC Features

●	●	●	●	●		Worldwide programmability for AC and DC parameters
●	●	●	●	●		Specification in accordance with ITU-T Recommendation Q.552 for interface Z
●		●	●	●		Specification in accordance with ITU-T Recommendation G.712, and applicable LSSGR(GR-506/507 etc.), GR-57, EIA/TIA-464 and other applicable worldwide standards.
●	●	●	●	●		Integrated balanced/unbalanced ringing capability fully software programmable up to 85 Vrms ringing voltage, Crest-factor selection between 1.2 and 1.6, frequency range between 15 and 75Hz
●		●	●	●		External ringing support
●		●	●	●		Programmable 12/16 kHz teletax generation (metering) and integrated notch filtering
●	●	●	●	●		Programmable battery feeding with capability for driving longer loops
●	●	●	●	●		Ground/loop start signaling
●		●	●	●		Ground key detection
●	●	●	●	●		Polarity reversal
●	●	●	●	●		Message Waiting Indication
●	●	●	●	●		Automatic modes for POTS signaling and Power Management
●	●	●	●	●		Advanced Integrated Test and Diagnostic Functions (AITDF) for local loop monitoring (including GR-909) and board production test capabilities.
●	●	●	●	●		On-hook transmission

Table 3 VINETIC® Features (cont'd)

-VIP	-2 CPE	-M	-C	-S	-0	VINETIC® Features
●	●	●	●	●		Power optimized architecture with power management capability (integrated battery switches)
●		●	●	●	●	Part of ADSL IVD and IPVD solution
●	●	●	●	●		Direct connection of Clare Litelink III device

Interface Features

●	●	●	●	●	●	PCM/µC interface selectable
2	1	2	2	2	2	PCM interface (number of highways)
●	●	●	●	●	●	Parallel Host interface: Intel/Motorola compatible
●	●	●	●	●	●	Serial control interface, SCI (Infineon) compatible, SPI compatible
●	●	●	●	●		SLIC interface compatible with DuSLIC® SLICs
●	●	●	●	●	●	JTAG interface for boundary scan

Available Packages[5)]

●	●	●	●	●	●	P-LQFP-176
●	●	●	●	●	●	P-LBGA-176
	●	●[6)]	●)6	●)6		PG-LBGA-144

Additional Features

●	●	●	●	●	●	SW compatible between different VINETIC devices
●		●	●	●	●	HW compatible between different VINETIC devices
●	●	●	●	●	●	Driver and API for Linux and VxWorks

1) 8-channel devices in preparation

2) In preparation.

3) All VINETIC® devices up to version v1.4 include RAM for download

4) in preparation

5) Green Packages in preparation, contact local sales for details

6) only available for production from v2.1 onwards

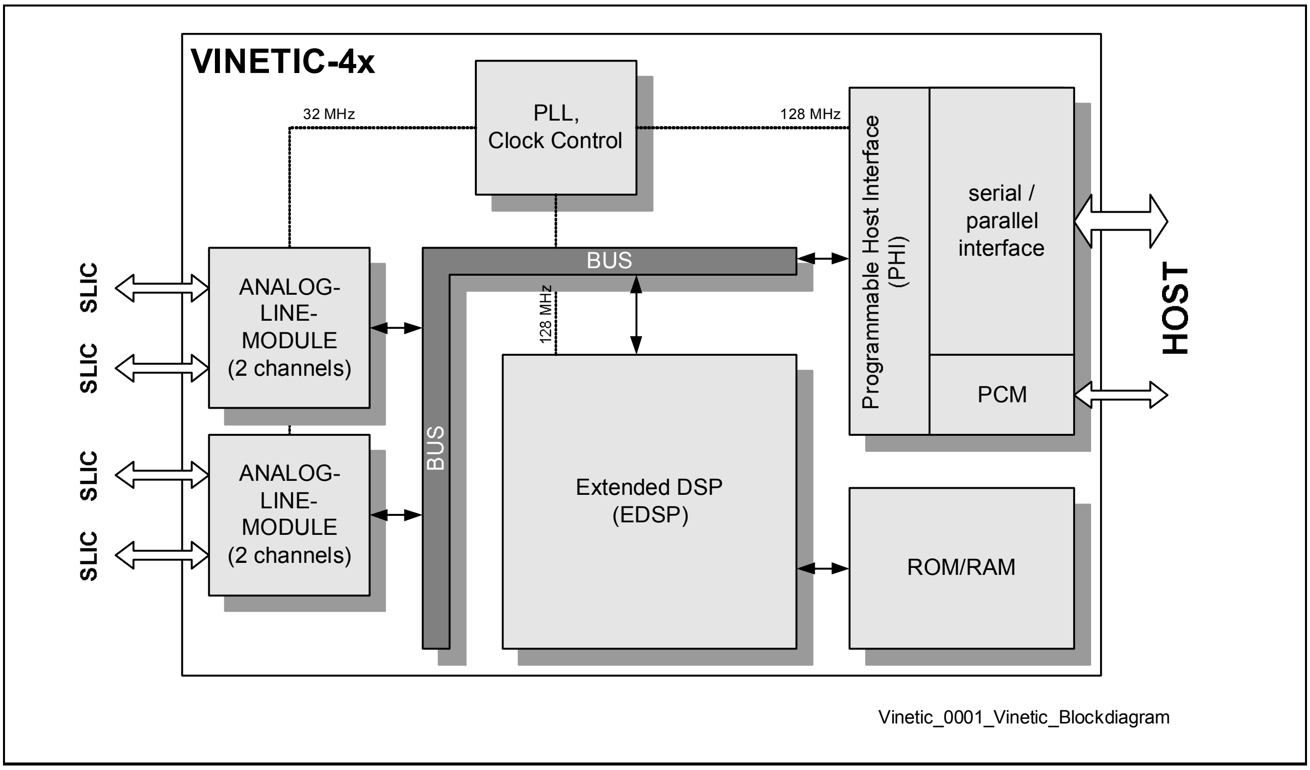


Figure 1 Block Diagram VINETIC®-4x

Figure 1 shows the typical block diagram of a VINETIC® 4-channel device.

1.1 Pin Diagram VINETIC®-4x

1.2 P-LQFP-176-2 Pin Diagram

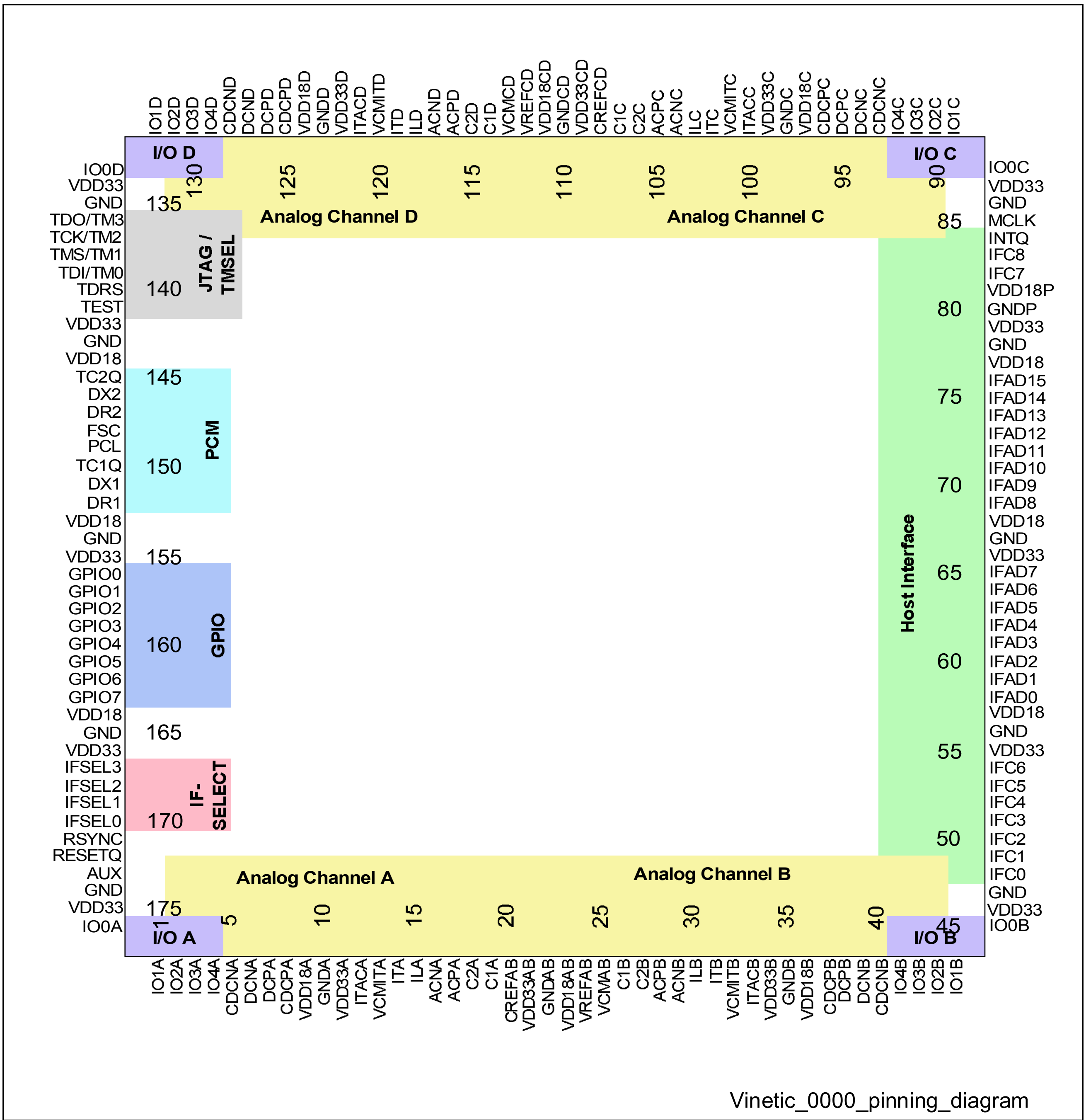


Figure 2 P-LQFP-176-2 Pin Diagram

1.3 P-LBGA-176-3 Pin Diagram

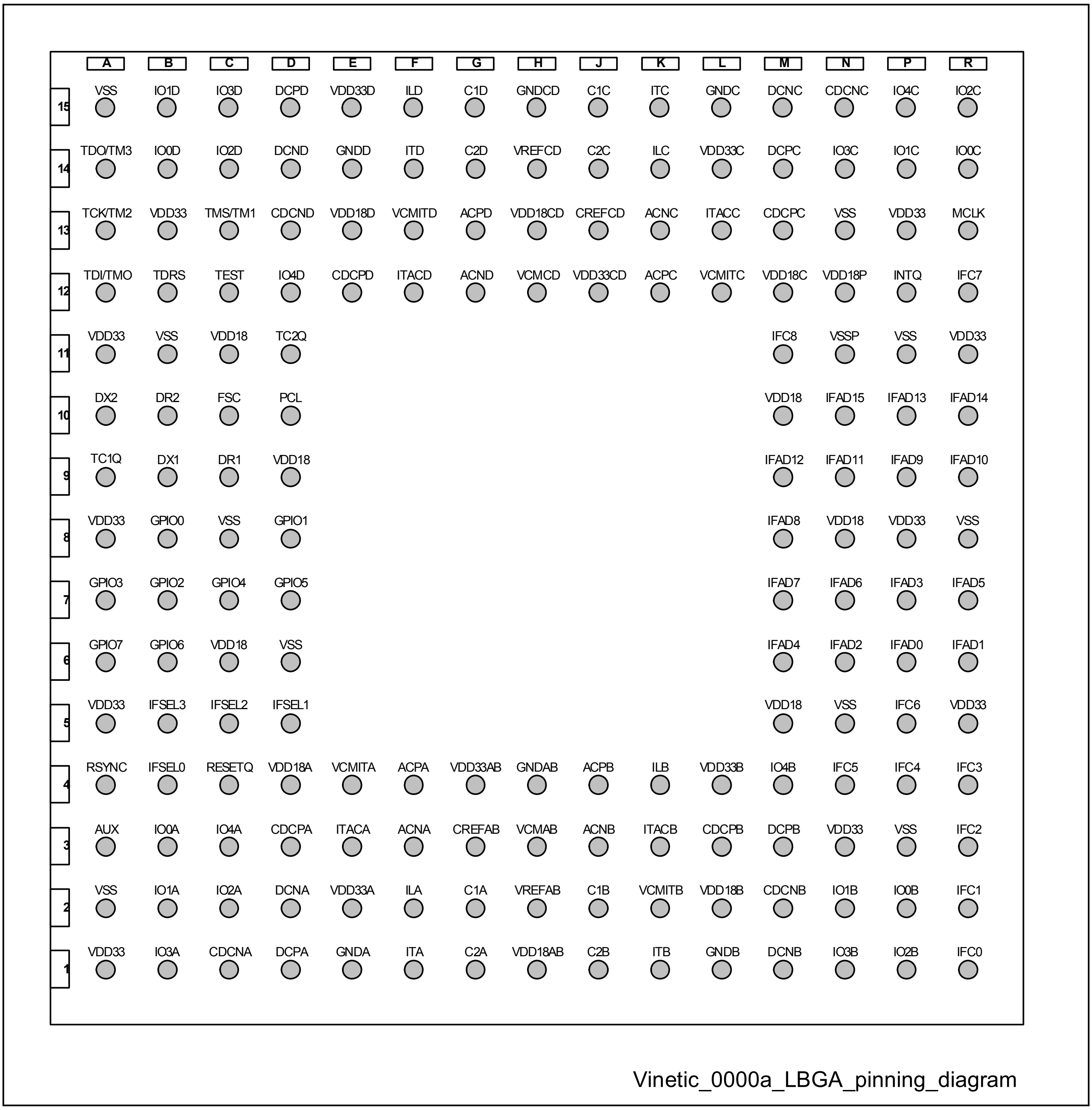


Figure 3 P-LBGA-176-3 Pin Diagram

1.4 PG-LBGA-144 Pin Diagram (4-channel devices)

Vinetic_0000a_HDLC_LBGA_144_pinning_diagram_21

1.5 PG-LBGA-144 Pin Diagram (2-channel devices)

	A	B	C	D	E	F	G	H	J	K	L	M
12	dnc	dnc	dnc	dnc	dnc	dnc	dnc	dnc	dnc	dnc	dnc	dnc
11	dnc	dnc	dnc	ITACD	VDD33A	dnc	VDD18A	VDD33A	ITACC	dnc	dnc	dnc
10	dnc	ITD	dnc	VCMITD	ILD	dnc	dnc	ILC	VCMITC	dnc	ITC	dnc
9	TDRSQ	TDI/TM0	TMS/TM1	TEST	dnc	dnc	dnc	dnc	TDO/TM3	INTQ	GNDP	VDD18P
8	VDD33	VDD18	dnc	TCK/TM2	DR1	GNDA	GNDA	IFC8	PCL	IFAD4	IFAD7	VDD33
7	DR1	DX1	FSC	DX1	dnc	GND	GND	IFC7	IFC4	IFAD6	IFAD5	VDD18
6	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GND	GND	GPIO7	IFC0	IFAD2	IFAD3	VDD18
5	VDD33	VDD18	GPIO6	RSYNC	AUX	GNDA	GNDA	GPIO5	IFC2	IFAD0	IFAD1	VDD33
4	IFSEL2	IFSEL0	IFSEL1	RESETQ	IO0A	CREFAB	VCMAB	IO0B	IFC3	IFC1	IFC5	IFC6
3	C1A	ITA	DCNA	VCMITA	ILA	C2A	VREFAB	ILB	VCMITB	DCNB	ITB	C1B
2	IO4A	IO3A	CDCNA	ITACA	VDD33A	VDD18A	C2B	VDD33A	ITACB	CDCNB	IO3B	IO4B
1	IO1A	IO2A	CDCPA	DCPA	ACNA	ACPA	ACPB	ACNB	DCPB	CDCPB	IO2B	IO1B

Vinetic_0000a_2CPE_LBGA_144_pinning_diagram

1.6 Logic Symbol VINETIC®-4x

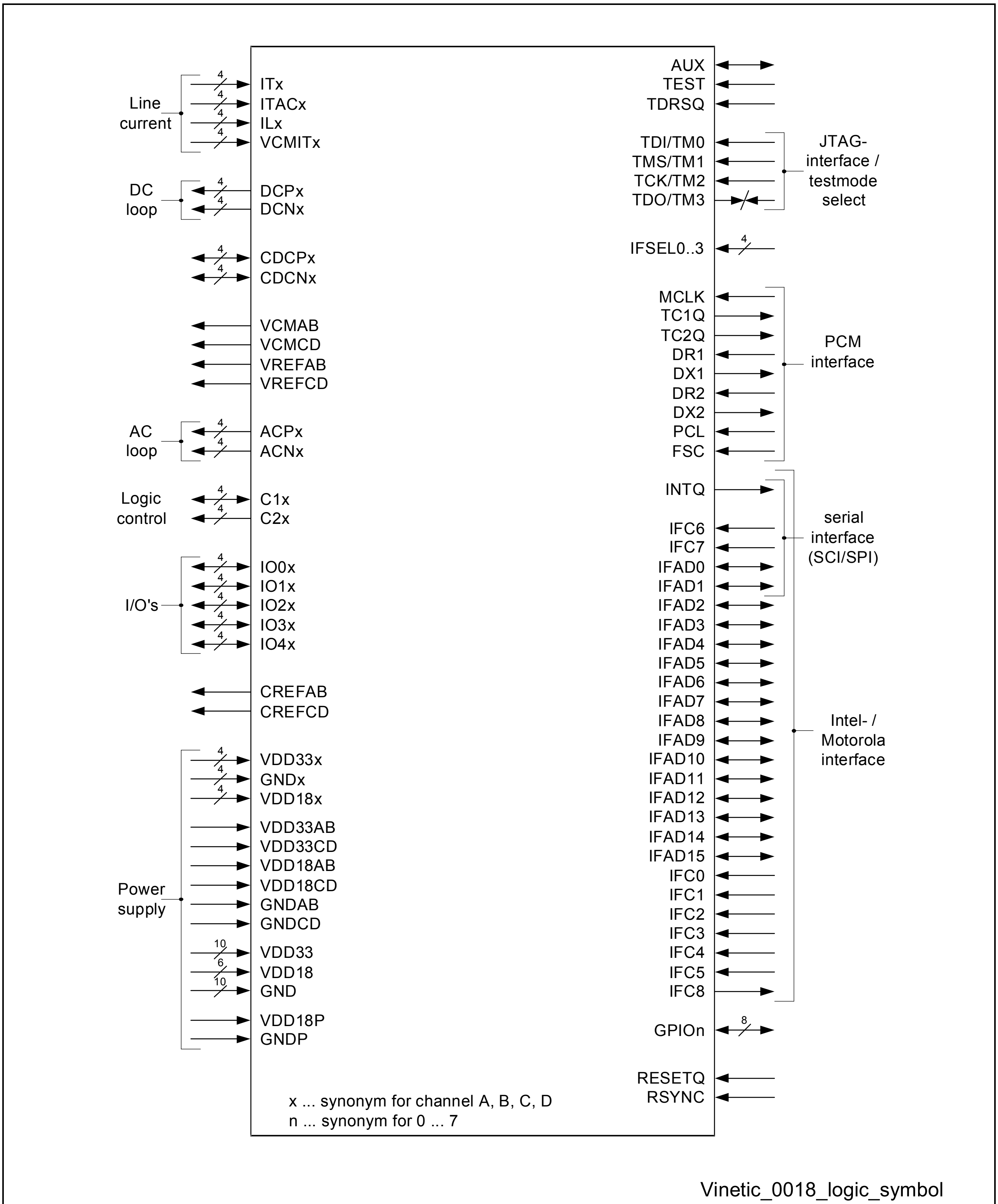


Figure 4 Logic Symbol VINETIC®-4x

1.7 Typical Applications

The following applications are only a small part of the numerous possibilities when using the VINETIC® chip set:

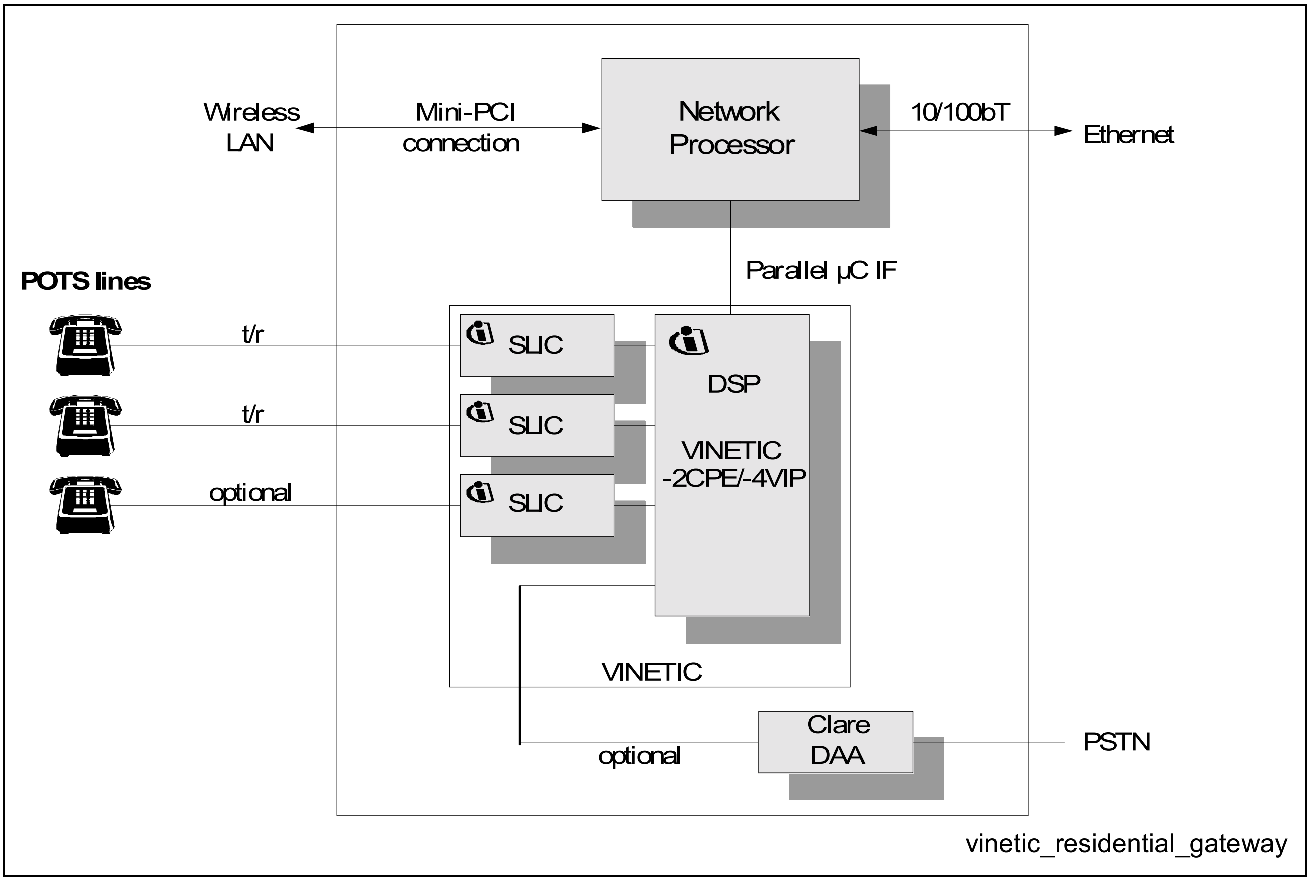


Figure 5 Residential Gateway / ATA / VoIP Router

Figure 5 shows a residential gateway that allows to extend the home network by introducing VoIP and a wireless data connection to it. The existing Ethernet connection is terminated by a network processor that enables additional functionality like firewalling, routing, and other data services as well as the voice call control. To keep the network as optimized as possible, the VINETIC®-2CPE for two voice channels or the VINETIC®-4VIP for four channels takes care of all the functionality that is voice related. All jitter buffering, RTP packetization, tone generation and detection including event handling and voice processing (compression G.72x, T.38 fax relay modem modulations, line echo cancellation) is handled within the DSP of the VINETIC®. No external memory or other components is needed. All the analog functionality is covered at the same time, including ringing, feeding, line testing, and supervision. The number of POTS lines can easily be increased by adding more VINETIC® devices if desired.

For an FXO operation to connect to the PSTN network, the VINETIC® devices allow direct connection to DAAs and provide all necessary signal processing functionality like Caller-ID detection.

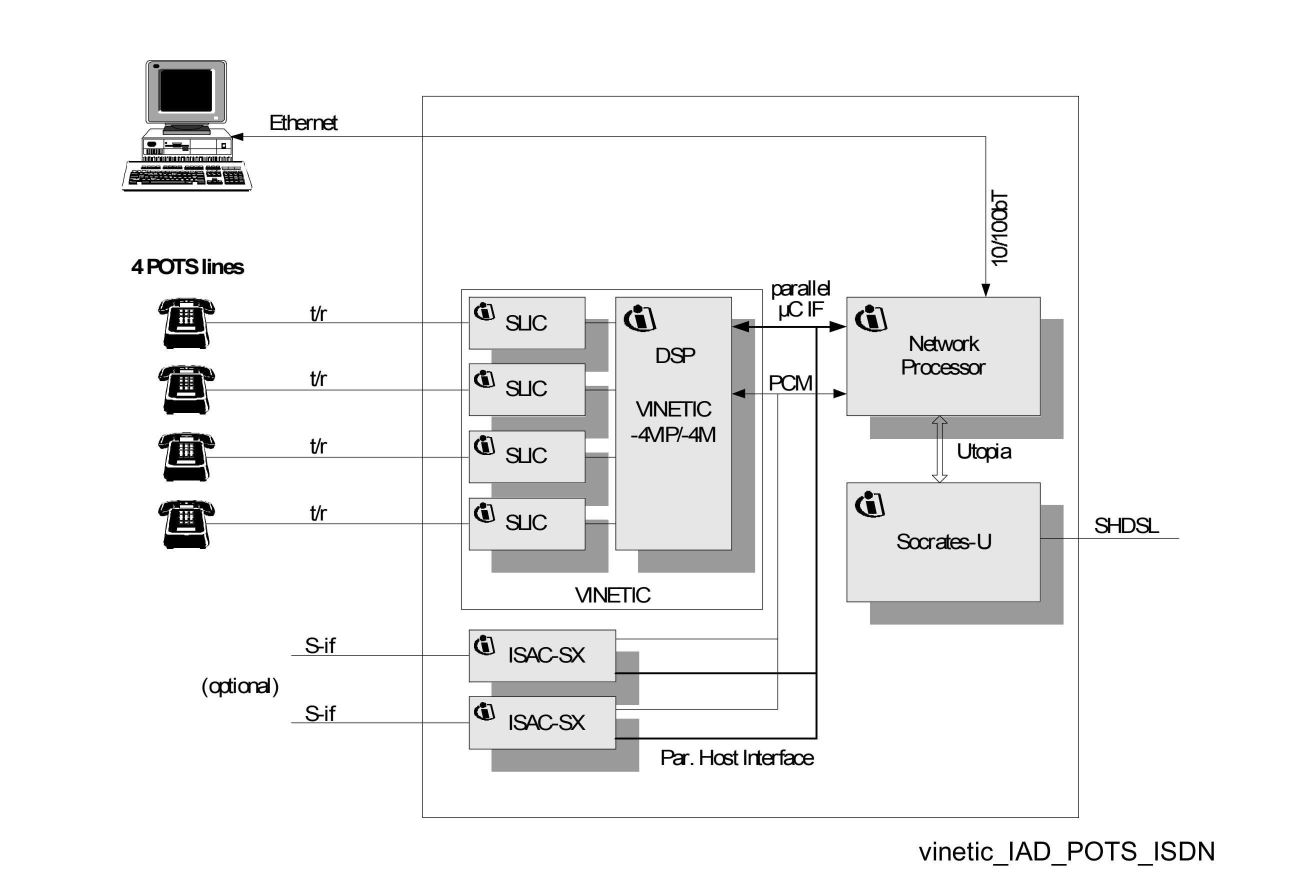


Figure 6 IAD serving POTS and ISDN (European Version)

Figure 6 shows an highly integrated G.SHDSL Integrated Access Device (IAD). The application consists of four major blocks: the SHDSL-transceiver, the network controller, the ISDN S-transceiver (the ISAC-SX devices are an option for european IADs), and the POTS part including voice processing (VINETIC®).

Analog signals from the POTS telephones are terminated within the VINETIC® chip set and then digitized. In a next step these signals are packetized and sent via tha microprocessor interfaces to the host controller. All necessary fucntions for AAL2 or RTP packetization including jitter buffer and compression are executed within the VINETIC®.

Additionally voice and tone processing like DTMF, CLIP and line echo cancellation (LEC) is also performed within the VINETIC® chip set.

When using the optional ISDN transceivers it is also possible to apply the LEC and compression features of the VINETIC® chip set to the ISDN channels. Voice from the ISAC-SX is transferred via PCM to the DSP of the VINETIC®, where the voice processing is performed. The VINETIC® is able to handle both voice compression (G.723.1, G.728 or G.729) and Near End LEC for up to 4 channels simultaneously or G.726 and LEC for up to 8 channels. In the application above all voice channels could be operated with ADPCM compression and line echo cancellation with a single VINETIC® chip set without external memory.

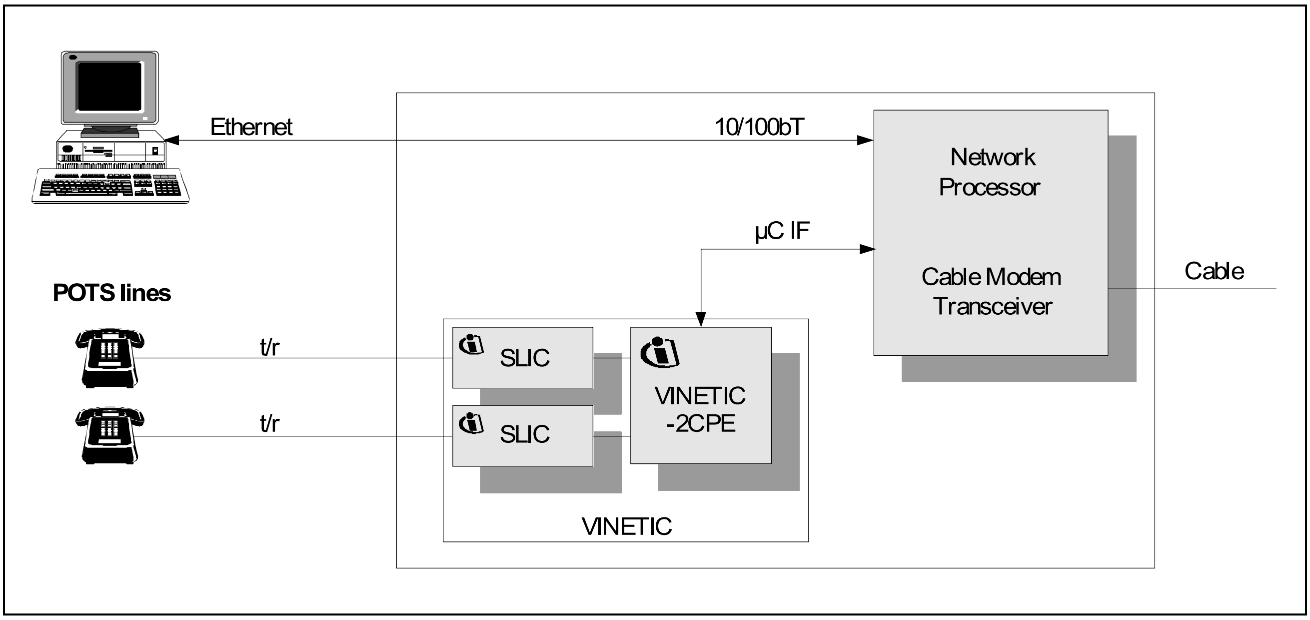


Figure 7 Cable Modem / Settop Box / SMTA / EMTA

The VINETIC® chip set fulfills all requirements for packetized voice over cable (see **Figure 7**). The voice data is transferred in RTP packets, allowing the network processor an easy packetization for transmitting it via VoIP over the cable network. The VINETIC® system is conform to PacketCable specification.

Fax-relay T.38 is also supported by the VINETIC® chip set. No additional DSP for voice processing or fax termination is needed in the system.

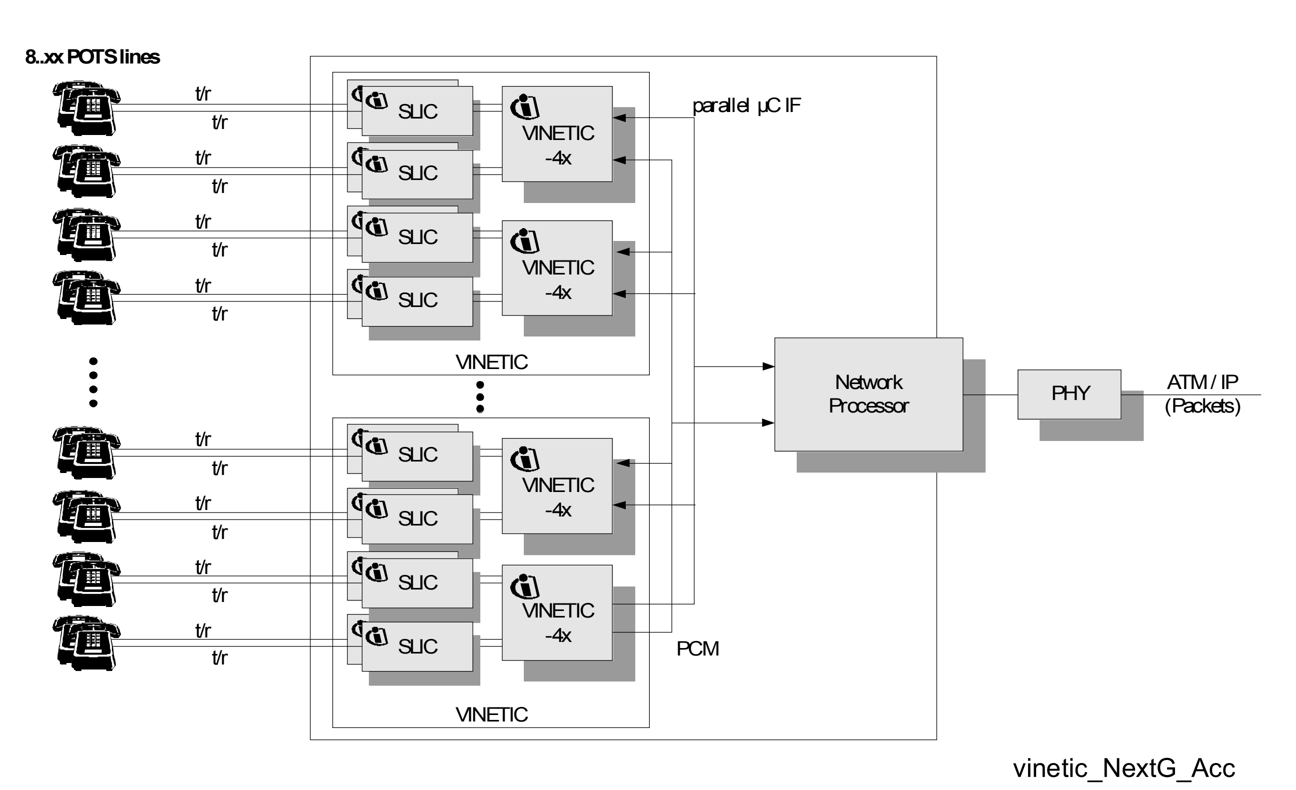


Figure 8 Next Generation Access Network Linecard

Next generation Access Networks / DLCs are using ATM or IP networks to transmit data and voice. VINETIC® is highly scalable and allows to install as many codecs in parallel as required by the linecard design. The integrated line testing, ring generation and small footprint SLIC chips makes VINETIC® an optimum fit for these high density applications.

Both RTP and AAL2 are supported by VINETIC® enabling the network processor to have either an IP or an ATM backbone.

2 VINETIC® Host Interface Description

The host interface of the VINETIC® is operated by a programmable host interface controller (PHI) which allows a flexible and easy adaption to various interface types. For programming the VINETIC® and performing data/packet transfer from/to VINETIC® a parallel interface or a serial microcontroller interface can be used. Additionally VINETIC® has an interface to PCM data.

VINETIC® 8/16-Bit Parallel Interfaces

The parallel interface can be operated in Intel 8/16-bit mode (multiplexed/demultiplexed) or in 8/16-bit Motorola mode.

Note: VINETIC®-2CPE and VINETIC® devices with PG-LBGA-144 package only support 8-bit interfaces

VINETIC® Serial Interfaces

The VINETIC® serial microcontroller interface (µC interface = SCI) is compatible with Motorola SPI and is electrically compatible with DuSLIC®. The PCM interface has 2 PCM highways and can be operated together with the serial µC interface or the parallel interface.

Note: VINETIC®-2CPE only supports one PCM interface

2.1 VINETIC® Host Interface Configurations

The VINETIC® host interface can be set into one of the following modes:

- 8-bit INTEL multiplexed mode + PCM interface (2 PCM highways)
- 8-bit INTEL demultiplexed mode + PCM interface (2 PCM highways)
- 16-bit INTEL multiplexed mode + PCM interface (2 PCM highways)
- 16-bit INTEL demultiplexed mode + PCM interface (2 PCM highways)
- 8-bit MOTOROLA mode + PCM interface (2 PCM highways)
- 16-bit MOTOROLA mode + PCM interface (2 PCM highways)
- VINETIC® serial µC interface (compatible with Motorola SPI and DuSLIC®) + PCM interface (2 PCM highways)

Note: VINETIC®-2CPE only supports 8-bit and serial interfaces with only one PCM highway

Note: VINETIC® devices with PG-LBGA-144 package only support 8-bit interfaces

Data transfers to and from the VINETIC® are either performed via a mailbox system and via the controller interface, or via PacketOverPCM.

The VINETIC® supports the widely used microcontrollers: e.g. ADM 5120, MPC850, MPC860, MPC8260, C165UTAH, ARM and MIPS based processors, etc.

All parallel and serial interfaces (host interfaces) use the same (multiplexed) pins. The desired interface type is selected by means of pin strapping.

3 Codec/SLIC Features (BORSCHT Functions)

3.1 BORSCHT functions

- Battery Feed

The DC battery feed for the subscriber equipment has to be adapted to different applications and country specific requirements. With the VINETIC® chip set, the feed characteristic is programmable in a wide range without any hardware change.

- Overvoltage Protection

Overvoltage protection is indispensable to prevent damage to the line circuit if the system is exposed to high voltages that can result from power lines crossing or lightning strikes.

The robust high voltage SLIC technology together with low cost external protection components, form a reliable overvoltage protection solution for the SLIC against overvoltages from the Tip and Ring lines.

- Ringing

The VINETIC® chip set integrates the ringing generator thus reducing the BOM by obsoleting the ring relay and ring generator. VINETIC® supports unbalanced and balanced ringing up to 85 V_{RMS}. With balanced ringing, the ringing voltage is applied differentially to the Tip and Ring lines. With unbalanced ringing, the ringing voltage is applied single-ended to either the Tip or Ring line. Balanced ringing is generated by SLIC-E/-E2 and SLIC-S, while SLIC-P can generate both balanced and unbalanced ringing. In addition the SLIC-DC integrates a DC/DC converter and simplifies CPE applications significantly while reducing BOM cost at the same time.

- Signaling (Supervision)

VINETIC® detects off-hook in both non-ringing (hook switch detection) and ringing modes (ring trip detection). The thresholds for ring trip detection within VINETIC®-4x can be programmed without changes to external components.

- Coding

VINETIC®-4x encodes an analog input signal to a digital PCM signal and decodes a PCM signal to an analog signal. Both A-law and µ-law coding is supported and can be selected via software.
Some members of the VINETIC® family also add ADPCM coding and low-bitrate vocoders

- Hybrid for 2/4-wire Conversion

The subscriber equipment is connected to a 2-wire interface (Tip and Ring) where information is transmitted bidirectionally. For digital transmission through the switching (PSTN) network, the information must be split into separate transmit and receive paths (4 wires). To avoid generating echoes, the hybrid function requires a balanced network matched to the line impedance. Hybrid balancing can be programmed in the VINETIC® device without any external components.

- Testing

In conventional solutions, testing of local loop and linecard requires a remote test unit and test relays. VINETIC®, however, internally offers the possibility of accurate line and board testing, thus avoiding the need for external test unit and relays.

Programmability

One of the main advantages of VINETIC® is that all SLIC and codec functions are programmable through software. The configuration software VINETICOS can be used to program at each port indepenently the following functions:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude, waveform (sinusoidal, trapezoidal, crest factor)
- Hook thresholds
- TTX modes

3.2 Advanced Integrated Test and Diagnostic Functions (AITDF)

3.2.1 Introduction

Subscriber loops are affected by a variety of failures and thus must be monitored. This requires access to the subscriber loop as well as specific test equipment. The tests involve measurements of resistance, capacitance, leakage, and any interfering currents and voltages.Traditionally up to 2 relays, and a test unit was necessary to perform such tests. VINETIC® integrates both the generation and detection of the test signals as well as the functionality of the relays.

3.2.2 VINETIC® Line Testing

The VINETIC® chip set uses its Advanced Integrated Test and Diagnostic Functions (AITDF) to perform all tests necessary for monitoring the local loop. The measurements can be accomplished not only on a channel specific basis, but also concurrently on all channels. This allows a strong reduction of the testing time compared to conventional test methods. Thus VINETIC® helps to increase quality of service and to reduce costs.

The VINETIC® line testing supports GR-909 line testing requirements.

Line Test Capabilities

The line test comprises the following functions:

- Loop resistance measurement:
  The DC loop resistance can be determined by supplying a constant DC voltage $V_{TR,DC}$ to the Ring- and Tip line and measuring the DC loop current via the IT pin.
- Leakage current:
  – Leakage current Tip/Ring
  – Leakage current Tip/GND
  – Leakage current Ring/GND
- Ringer/Line capacitance:
  Capacitance measurements can be performed by using the integrated ramp generator function. Loading a capacitor $C_{Measure}$ with a constant voltage ramp results in a constant current which is proportional to $C_{Measure}$.
  – Line capacitance Tip/GND
  – Line capacitance Ring/GND
- Foreign voltage measurement:
  Three analog input pins per voice channel can be used for direct and differential measurement of external voltages.
  – Foreign voltage measurement Tip/GND
  – Foreign voltage measurement Ring/GND
  – Foreign voltage measurement Tip/Ring
  – Supervision of Battery voltages
- Measurement of ringing voltage
- Measurement of line feed current
- Measurement of supply voltage V_{DD} of the VINETIC®-4x
- Measurement of transversal- and longitudinal current.
- Noise Measurement

3.2.3 Board and Production Testing

The VINETIC® chip set has a set of signal generators and features implemented to accomplish a variety of diagnostic functions that can be used in production tests. Various test loops and measurement features are completing this tool suite.

4 Signalprocessing Capabilities of the VINETIC®

The VINETIC®-VIP, -M and -C versions are equiped with an EDSP module (Enhanced Digital Signal Processor module) to perform voice and tone processing functions.
The maximum available signal processing capability of the EDSP is limited by the 128 MCycles/s and the internal RAM.

Table 4 gives an overview on the performance demands of the different algorithms/ functions available and how many resources of them can be activated. As each FW version offers a different subset, a document is available that lists the available resources per firmware version. For further description of the functions refer to **Chapter 7** or the VINETIC® documentation available.

Table 4 Provided Algorithms for VINETIC®[1)]

Algorithm/Function	Module[2)]	MCycle/s	max. # of ressources available[3)]
Operating System (Base load of internal control, Command Mailbox handling, ..)		typ. 15	1
DTMF Receiver	Signaling	1.0	4
Caller ID Transmission	Signaling	1.5	4
Universal Tone Detection (UTD) / V.18	Signaling	1.2	4
ATD 2.1 kHz, Modem Tone Detection with Phaseshift (phase reversal, amplitude modulation) / DIS	Signaling	1.3	4
DTMF generation[4)]	Signaling	1.8	4
Near End Line Echo Cancellation (LEC), G.165/G.168 (NLP included): – LEC 8 ms – LEC 16 ms	PCM, ALM, Coder	 4.4 5.4	4
Far End Line Echo Cancellation, G.168 (NLP incl.): – LEC 32 ms – LEC 64 ms – LEC 128 ms	PCM, ALM, Coder	 11.0 17.0 29.0	4
G.711 (block based [5,5ms]): G.711, G.711 Annex I (BFI), G.711 Annex II (VAD, CNG), jitter buffer, protocol handling G.711 (sample based)	Coder PCM	5.0[5)] 0.6	8 16

Table 4 Provided Algorithms for VINETIC®[1)] (cont'd)

Algorithm/Function	Module[2)]	MCycle/s	max. # of ressources available[3)]
G.711 Annex I (BFM)	Coder	0.6	8
G.711 Annex II (VAD + CNG)	Coder	0.7	8
G.726 for Coder Module (block based [11ms]) G.726 for PCM Module (sample based)	Coder PCM	11.4[5)] 5.5	8
G.723.1 (packet size 30 ms)	Coder	12.4[5)]	4
G.729 A, B (packet size 10, 20 ms)	Coder	10.7[5)]	4
G.729 A, B, E (packet size 10, 20 ms)	Coder	20.9[5)]	4
G.728 (packet size 5, 10, 15, 20 ms) incl. G.728 Annex I (Packet Loss Concealment)	Coder	19.5[5)]	4
Automatic Gain Control AGC	Coder	0.7	8
T.38	Coder	(typ. 10)	4

1) not all algorithms/functions are supported with all devices. See **Table 3 on Page 13** for details.

2) Refer to **Chapter 7** for the definition of the modules

3) not all devices and all firmware versions support all the given number of resources. A firmware status sheet is available showing the exact number of resources available per version.

4) DTMF generation can be realized by using EDSP ressources or by using the integrated ALM tone generators. Using the integrated ALM tone generators doesn't allocate EDSP ressources.

5) Numbers for block/packet based coder channels include Voice Play Out (reordering, jitter buffer, clock synchronization) and Packetization (AAL2 or RTP/RTCP)

At the Coder Module different coders can be activated in receive and transmit direction. In this case the max. # of MCycle/s of both coders has to be taken into account.

The Far End Line Echo Cancellation has shared ressources with the low-bitrate coders. Therefore each activated Far End LEC channel will reduce the available number of coder channels by one.

5 Programming of the VINETIC®

This chapter gives an overview on the command/data structure of the VINETIC® chip devices. For further information see the *User Manual Software Description*.

VINETIC® uses a flexible command structure which can be used with parallel and serial interfaces.

Note: In the following chapters, downstream indicates the direction from the host controller to the VINETIC, upstream the direction from VINETIC to the host controller)

5.1 Command/Data Structure in Downstream Direction

Each command consists either of one single command word, or of two command words followed by data. The first command word contains information about the read/write status, the type of the command/mode and the VINETIC®channel addressed. The second command word defines length and destination (or source respectively) for control data or in case of packet data only the length information.

Four different command types can be distinguished:

1. **Packets:** Packets are indicated by a voice packet operation identifier (**VOP**) or a packet based event transmission operation identifier (**EVT**) within the CMD-bits of the first command word. The first command word contains read/write (bit 15) and channel information also. The second command word includes the number of following data words and the information if there is an even or odd number of bytes in the packet:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	R/W =0	0	0	**VOP/EVT**					reserved				channel			
2nd word	reserved		ODD	reserved					length							
n x data	data															

2. **Read/Write Commands for Register Access:** There are three types of read/write commands (depending on the HW-module to be addressed) that differ in the CMD-bits of the first command word:
   a. status operation (**SOP**) commands provide access to configuration and status register of the Analog-Line-Modules.
   b. coefficient operation (**COP**) commands enable the configuration of the coefficent registers of the Analog-Line-Modules.
   c. Interface operation (**IOP**) commands are needed to set all registers related to the Programmable Host Interface (PHI).
   The first command word contains read/write (bit 15), broadcast (bit 13) and channel

information. The second command word includes the offset of the register address and the number of the following data words

<table>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>1st word</td><td>R/W
=0</td><td>0</td><td>BC</td><td colspan="5">SOP/COP/IOP</td><td colspan="4">reserved</td><td colspan="4">channel</td></tr>
<tr><td>2nd word</td><td colspan="8">address offset</td><td colspan="8">length</td></tr>
<tr><td>n x data</td><td colspan="16">data (only write commands)</td></tr>
</table>

3. **Read/Write Commands for EDSP Operation:** EDSP operations are indicated by an EDSP operation command identifier (**EOP**) within the CMD-bits of the first command word). The first command word contains read/write (bit 15), broadcast (bit 13) and channel information . The second command word includes information about the SW-module which should be addressed, the command and the length of the following data:

<table>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>1st word</td><td>R/W
=0</td><td>0</td><td>BC</td><td colspan="5">EOP</td><td colspan="4">reserved</td><td colspan="4">channel</td></tr>
<tr><td>2nd word</td><td colspan="3">SW-module</td><td colspan="5">extended command</td><td colspan="8">length</td></tr>
<tr><td>n x data</td><td colspan="16">data (only write commands)</td></tr>
</table>

4. **Short Commands:** Short commands consist of the first command. The first command word contains read/write (bit 15), broadcast (bit 13) and channel information also.

<table>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>1st word</td><td>R/W
=0</td><td>1</td><td>BC</td><td colspan="9">command or operational state</td><td colspan="4">channel</td></tr>
</table>

5.2 Command/Data Structure in Upstream Direction

In upstream direction four different data types can be distinguished:

1. **Packets:** Packets in upstream direction have the same command structure as packets in downstream direction, but the R/W-bit of the first command word is set. The SC-bit is always cleared, the CMD-bits indicate a voice packet operation (**VOP**) or a packet based event transmission operation (**EVT**) and the CHAN-bits specify the corresponding channel. The second word includes the number of following data words and an indication whether there is an even or odd number of bytes in the packet.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	R/W =1	0	0	**VOP/EVT**					reserved				channel			
2nd word	reserved		ODD	reserved					length							
n x data	data															

2. **Responses to Read Commands for Register Access:** Responses to read commands for register access starts with the copy of the corresponding read command (first and second command word) sent by the host, followed by the requested data.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	R/W =1	0	BC	**SOP/COP/IOP**					reserved				channel			
2nd word	address offset								length							
n x data	data															

3. **Responses to Read Commands for EDSP Operation:** Responses to read commands for EDSP operation (**EOP**) start with the copy of the corresponding read command (first and second command word) sent by the host, followed by the requested data:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	R/W =1	0	BC	**EOP**					reserved				channel			
2nd word	SW-module			extended command					length							
n x data	data															

4. **Responses to Short Commands:** Responses to short commands do not repeat the command header, because they will be provided within a given command recovery time. Therefore only the requested data will be returned.

5.3 First Command Word

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	**SC**	**BC**	**CMD[4:0]**					**reserved (SUBCMD[3:0])**				**CHAN[3:0]**			

R/W Read/Write bit for defining a read or write command

SC Short Command bit defining the short commands for a fast register access to VINETIC® or operating mode change

BC Broadcast bit defining a broadcast message to all channels on the VINETIC®(only SOP, COP, EOP, and short commands)

CMD[4:0] Command bits defining the type of command: SOP, COP, IOP, VOP, EVT, EOP

SUBCMD[3:0] Only valid in case of a short command (SC = 1) and directly sets the operating mode or gives fast register accesse, e.g. the reading of the interrupt register (IR)

CHAN[3:0] Channel identifier.

5.4 Second Command Word

5.4.1 Second Command Word in Case of SOP, COP and IOP

Note: The second command word only exists if in the first command word bit SC = 0.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OFFSET[7:0]								**LENGTH[7:0]**							

OFFSET[7:0] The second command word specifies the internal offset for the subsequent data words. It is possible to send a variable number of data words with one command.

LENGTH[7:0] Number of following data words binary coded (in case of write command) or number of data words to be read (in case of read commands) respectively.

5.4.2 Second Command Word in Case of EOP, EVT and VOP

Note: The second command word only exists if in the first command word bit SC = 0.

For definition of the second command word in case of EOP, EVT and VOP see the *Preliminary User's Manual - Software Description*.

5.5 Data Words

Words following the first and second command words denote data.

For the data format, especially in case of packet based information (VOP and EVT), see the *Preliminary User's Manual - Software Description*.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[15:0]															

5.6 Data Handling

The VINETIC® includes an interface controller (Programmable Host Interface - PHI) which handles the communication between the host and the VINETIC®-4x internal units via a SW state machine. The VINETIC® handles packet data (VOP, EVT commands), command data (COP-, SOP-, IOP-, EOP-commands) and short commands (SC bit of first command word is set) as well as a direct memory access of the interrupt register (DIA) for SW-handshake (RDYQ bit in the DIA).

In downstream direction, packet data sent by the host to the VINETIC® (or PHI respectively) is stored in a in-buffer (packet in-box) and command data is stored in another in-buffer (command in-box). Subsequently these data are transferred to the EDSP of the VINETIC®.

In upstream direction packet/command data are transferred from the EDSP to internal out-buffers (packet out-box/command out-box) and the VINETIC® notifies the host controller via status registers and interrupt that data is ready for reading. The host can read the packet or command out-box via short commands (rPOBX → read packet out-box, rCOBX → read command out-box).

Because of varying command recovery times, the VINETIC® supports HW- and SW-handshake for speed optimization of the data transfer. The HW-handshake is done via the RDYQ line of the VINETIC® and the SW-handshake is done via the RDYQ bit in the

DIA register. To enable a fast access to the DIA register, the DIA register can be addressed directly via the DIA command. All other registers as well as the command and packet in- and out-box can't be addressed directly. For this the PHI handles the data transfer by address auto-incrementation.
Short commands are treated seperately and with higher priority than packet and command data and are not handled via the command mailbox.

To optimize the data transfer during download and/or for packet transmission the size of the in-boxes (command/packet) can be changed with the short commands wMAXCBX ("Maximize command in-box size" → Command in-box size = 255 / Packet in-box size = 31) and wMINCBX ("Minimize command in-box size" → Command in-box size = 31/ Packet in-box size = 255). The size of the out-boxes cannot be changed.

Before the host writes data to the VINETIC®, it has to make sure that there is enough free memory space in the desired packet- and/or command in-box. This is done by reading the FIBXMS (free in-box memory space) register via the short command rFIBXMS. As long as there is enough free memory space in the in-boxes (packets/ commands) the host is allowed to send data.

Every 125 µs the VINETIC® internal EDSP will read one packet and one command from the packet and command in-box. COP, SOP and IOP commands will be distributed to the corresponding units (COP and SOP → Analog-Line-Module, IOP → PHI). VOP, EVT and EOP commands will be processed by the EDSP.

In upstream direction the packet data sent from the VINETIC® to the host is stored in a 256 word out-buffer (packet out-box). The responses to read commands are stored a 32 word out-buffer (command out-box). If the EDSP wants to send data (VOP or EVT operations) to the host, it checks the free memory space in the packet out-box before writing the data. If there is not enough memory in the packet out-box the EDSP discards the data and sets the box-overflow flag in the Mailbox Status Register2 (BXSR2).

The communcation between host and VINETIC® can either be done by interrupt handling (maskable interrupt bits—one interrupt line from VINETIC® to the host) or by polling (host polls VINETIC® interupt and status registers).

6 Operating Modes

6.1 Overview of all VINETIC® Operating Modes

VINETIC® provides full control over the analog line status by a comprehensive set of modes that can be clustered into 7 groups:

Sleep Modes

Sleep Power Down Resistive

The VINETIC® is completely powered down. The SLIC feeds via an internal resistor the VBATH battery voltage onto the analog line (SLIC-P offers in addition the option of feeding the VBATR voltage).

On off-hook, an comparator in the SLIC wakes the VINETIC®. No debouncing of spikes is performed in this case

Power Down Modes

Power Down High Impedance

The selected channel of the VINETIC® is powered down with internal clocks and deglitching logic running, but no voice signals are processed. The SLIC is high impedance on the analog line.

This is the preferred state for a fault condition or an inactive line.

Power Down Resistive

The selected channel of the VINETIC® is powered down with internal clocks and deglitching logic running, but no voice signals are processed. The SLIC feeds via an internal resistor the VBATH battery voltage (SLIC-P offers in addition the option of feeding the VBATR voltage) onto the analog line. Off-hook detection is supported with programmable threshold values and a debounce timer.

This is the preferred state for an on-hook telephone.

Active Modes

Active Low and Active High

In active mode the complete voice path of the VINETIC® is active and also the SLIC is feeding the line. In active low the VBATL battery supply and in active high the VBATH battery supply is used.

This is the preferred state for off-hook telephone conversation and for on-hook transmission.

Active Boost

This special active mode is mainly used to drive extreme long lines. As battery voltages for driving the line the delta between VHR minus VBATH (for SLIC-P VBTR) is used.

Current Limitation

For above active modes the SLIC-P and the SLIC-LCP offer a selectable current limitation. The SLIC-P can be selected for either 60 or 90 mA. The SLIC-LCP between 75 and 110 mA.

Lower limitation is mainly used to limit the current flowing in fault cases and during ring-trip / off-hook transitions.

Active with Metering

For above active modes all VINETIC® devices support 12 and 16 kHz metering signals. Active with Metering switches the generation of such frequencies on.

Ringing Modes

Ringing (Active Boost)

In this state the VINETIC® generates a ringing signal according to the settings made for frequency, voltage, DC offset and crest factor and the SLIC applies it as balanced ringing onto tip and ring wire. Ring-trip is supported with programmable ring-trip levels

Ringing on Ring / Tip with Tip / Ring to Ground (SLIC-P only)

The SLIC-P offers in addition to balanced ringing also integrated unbalanced ringing. In this mode the ring voltage is only applied to either Ring or Tip wire, the other wire is pulled to ground.

Ring Pause Modes

Ring Pause is the default state for the time between two ring bursts. Off-hook detection is supported with programmable threshold values.

This is the preferred state for the time between two rings.

Ground Start Modes

In this mode ground start is supported.

Testing Modes

Testing modes are extensions of the active modes using various SLIC settings. Ring or the Tip wire can be set to high impedance (all SLICs) or GND (only SLIC-P). Ring and Tip wire can be set both to High Impedance and (all SLICs) or in addition to have some impedance for testing purposes (only SLIC-E v1.2 and

GEMINAX-S / -S MAX).
All these modes are intended for line testing and diagnosis functions.

6.2 Automatic Modes for POTS Signaling and Power Management

The following automatic modes[1] can be switched on/off by the user (AUTOMOD Automatic Mode Register):

1. Automatic mode “Off-hook detection (Auto Off-hook)”:
   Automatic switching to Active Mode after off-hook was detected.
   Power Down (PDRH, PDRR), Ringing, Ring Pause → Active
   Automatic switching to the current mode set by the host (indicated by MODE-SRC bits in register OPMOD-SRC) after on-hook was detected.
   Active → host mode
2. Automatic mode “Battery Switching for Power Management (Auto-Battery)”: change from ACTH to ACTL. A change will take place only once after off-hook was detected. A further change will not result in a mode change.
3. Automatic mode “Power Down Over Temperature”
   Automatic switching to Power Down High Impedance mode, when the SLIC detects overtemperature.
4. Automatic Ring Cadencing[2]
   A ring burst is executed with a programmed cadence including the transmission of Caller-ID.
5. Automactic Teletax (Metering)[3]
   The Teletax signal stops automatically after a programmable period.

[1] more automatic modes are in preparation
[2] only availabe from v2.1 onwards
[3] only available from v2.1 onwards

7 Firmware Architecture

7.1 Module Concept

The VINETIC®-4x has a modular firmware architecture, which is based on four different firmware module types:

- PCM-Interface-module
- Analog-Line-Interface-module
- Coder-module
- Signaling-module

These modules contain the functional blocks necessary for the implementation of typical voice over packet applications as well as standard TDM applications.

The **Figure 9** illustrates the module concept. The multiple arrows show the data path to the hardware, the single arrows symbolize signals which can be connected together via a signal-array.

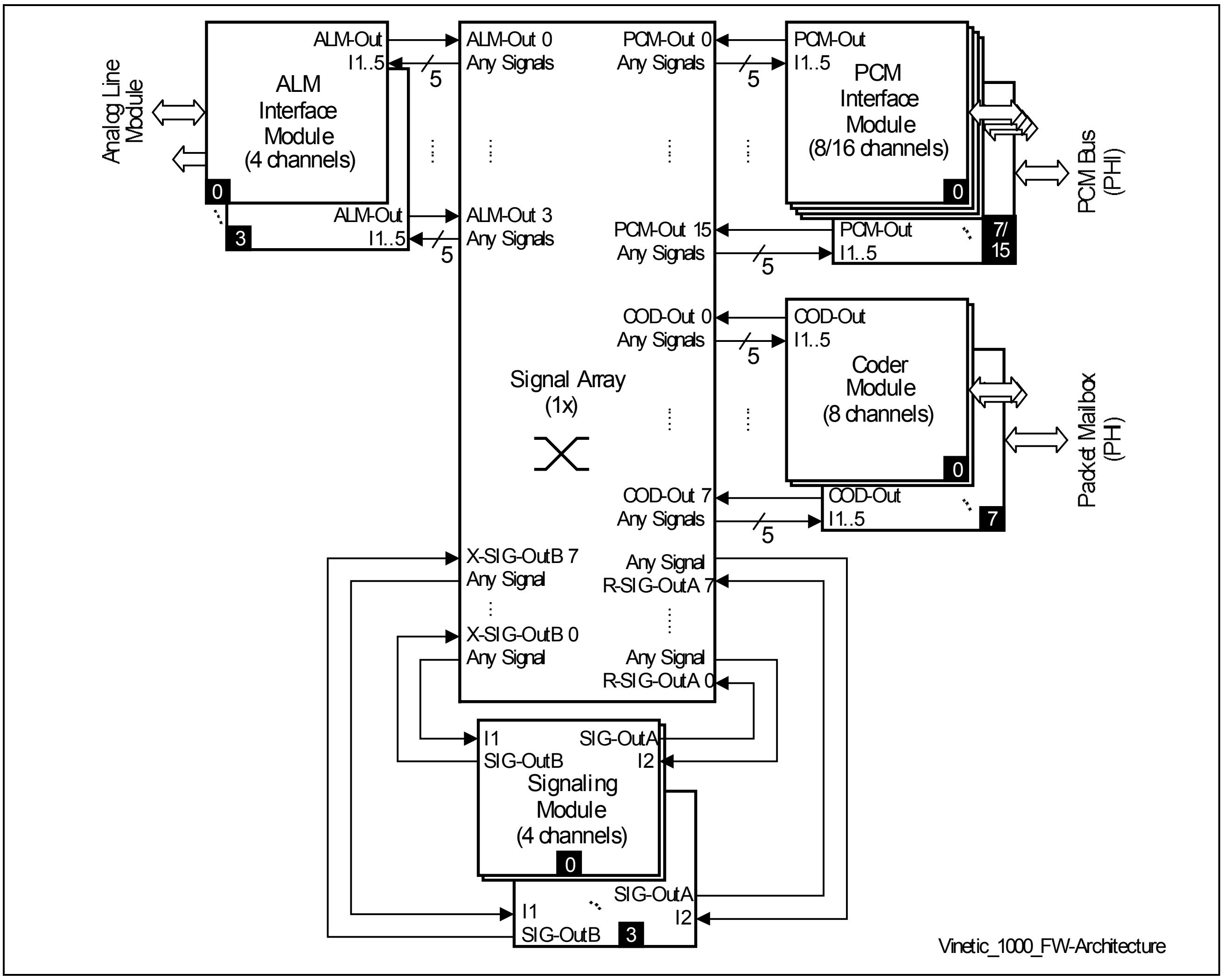


Figure 9 Module Concept

Each module contains 4, 8, or 16 channels. Each channel of each module can be connected with any channel of any module via the Signal-Array. The global signal array contains the output values of each channel from every module. Each channel input signal of each module can be connected with any signal in the signal array.

With the concept of the global Signal-Array the applied module functions can be adapted very easily and flexible to the needs of different applications. Typical module configurations will be provided by Infineon.

Note: Different firmware versions will provide subsets of the firmware modules described in this chapter.

Note: Check Firmware Status Sheet documentation for the exact number of supported modules and features within the modules.

7.2 PCM-Interface Module

The PCM-Interface-module supports up to 16 channels. Each channel can be activated separately and supports the following features:

- Decoder and encoder: G.726, G.711(without annex I and II, without CNG and VAD)
- RBS/CAS filtering for enhanced modem performance [1)]
- Conferencing (via ADDER submodule)
- Gain
- DC HP (DC high-pass)
- LEC (far end/near end) with NLP

Figure 10 shows one channel of the PCM-Interface-module:

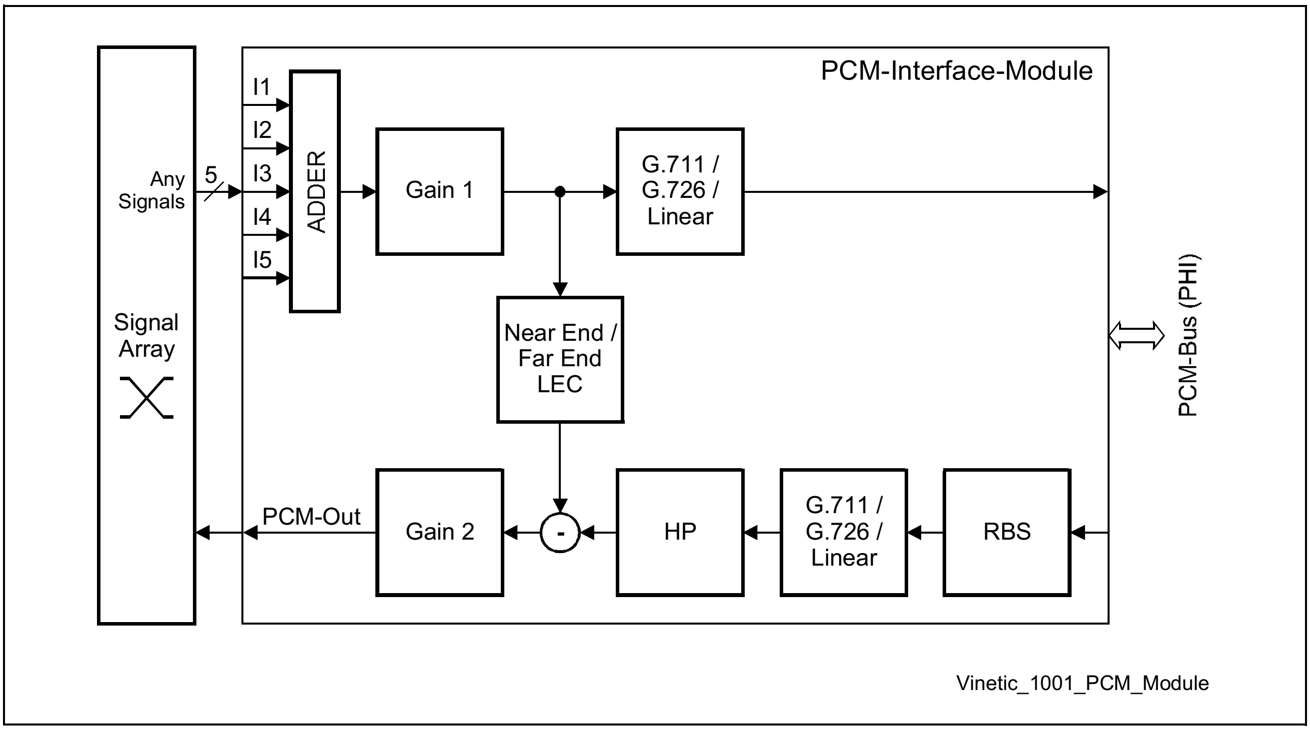


Figure 10 PCM-Interface Module

The **G.711/G.726/Linear** submodule performs either A/µ-Law, ADPCM coding/decoding or can be switched to 16 bit linear data (two consecutive PCM time slots).
The **LEC** submodule can be used to cancel a near or far end echo. A near end echo is generated via a local hybrid, a far end echo via a complete network .

The **RBS** (robbed bit signaling) submodule suppresses signaling information. It replaces the signaling information with a V.90 friendly pattern. The RBS module modifies the received PCM values and herefore it has to be in front of the PCM decoder.

The **Gain** submodules allow a gain adjustment of the transmit and receive path.
The **HP** submodule filters the DC part of the signal.

1) in preparation

7.3 Analog-Line-Module ALM

The VINETIC®-4x contains as many ALM modules as analog ports are specified for the corresponding device. The ALM module has a granularity of 2, as the hardware blocks are also the same granularity.
Channel one and two are within the Analog-Line-Module 1 (HW-Module), and channel three and four for the 4-channel devices are within the Analog-Line-Module 2 (HW-Module). Data is transferred from the SLIC devices via the Analog-Line-Module to the Signal-Array and vice versa.
Each ALM-Module channel supports the following features:

- Conferencing (ADDER Submodule)
- Gain
- LEC (far end/near end) with NLP

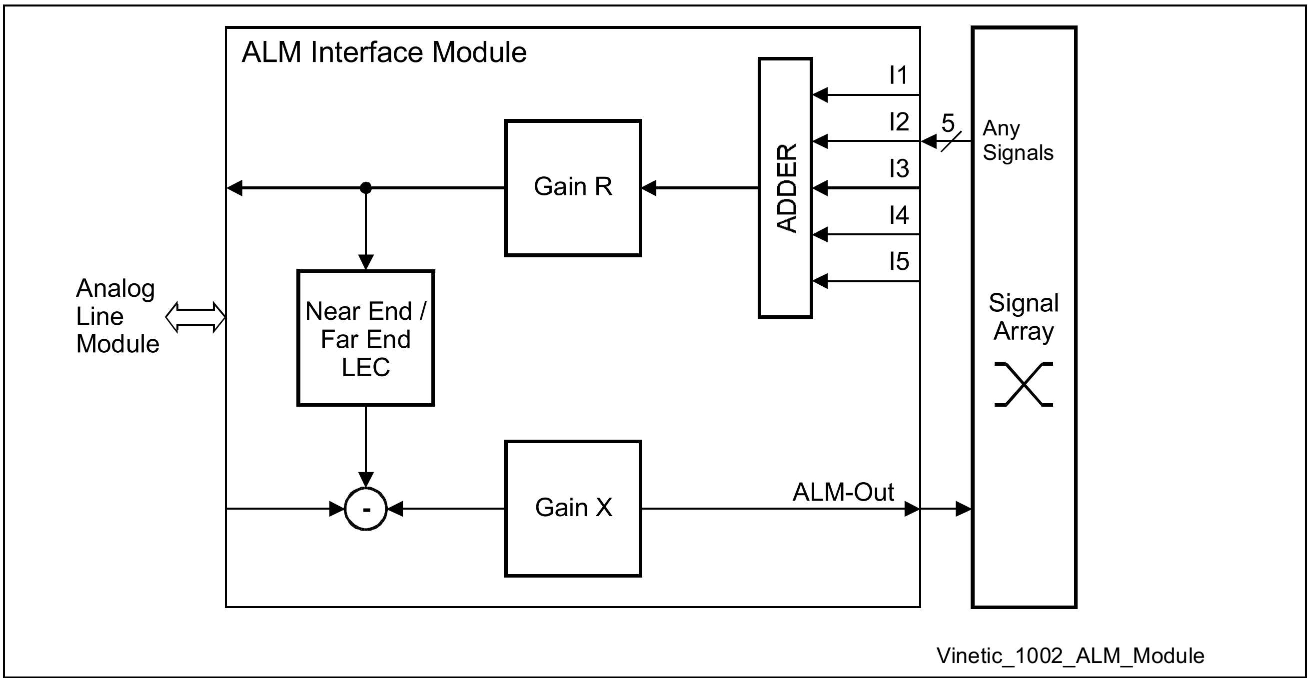


Figure 11 Analog-Line-Module ALM

The **Gain** submodules allow a gain adjustment of the transmit and receive path.

7.4 Signaling Module

The Signaling-Module supports up to 4 channels. Each channel supports the following features:

– DTMF Receiver
– 2 ATD (Answering Tone and DIS Detection)
– 2 UTD (Universal Tone and V.18 A Detection)
– DTMF/AT Generation
– CPT Detector
– CID Receiver
– CID (Caller ID) Sender
– DTMF / AT Generation
– Universal Tone Generator (UTG)
– Event Transmit Unit

Figure 12 shows one channel of the signaling module.

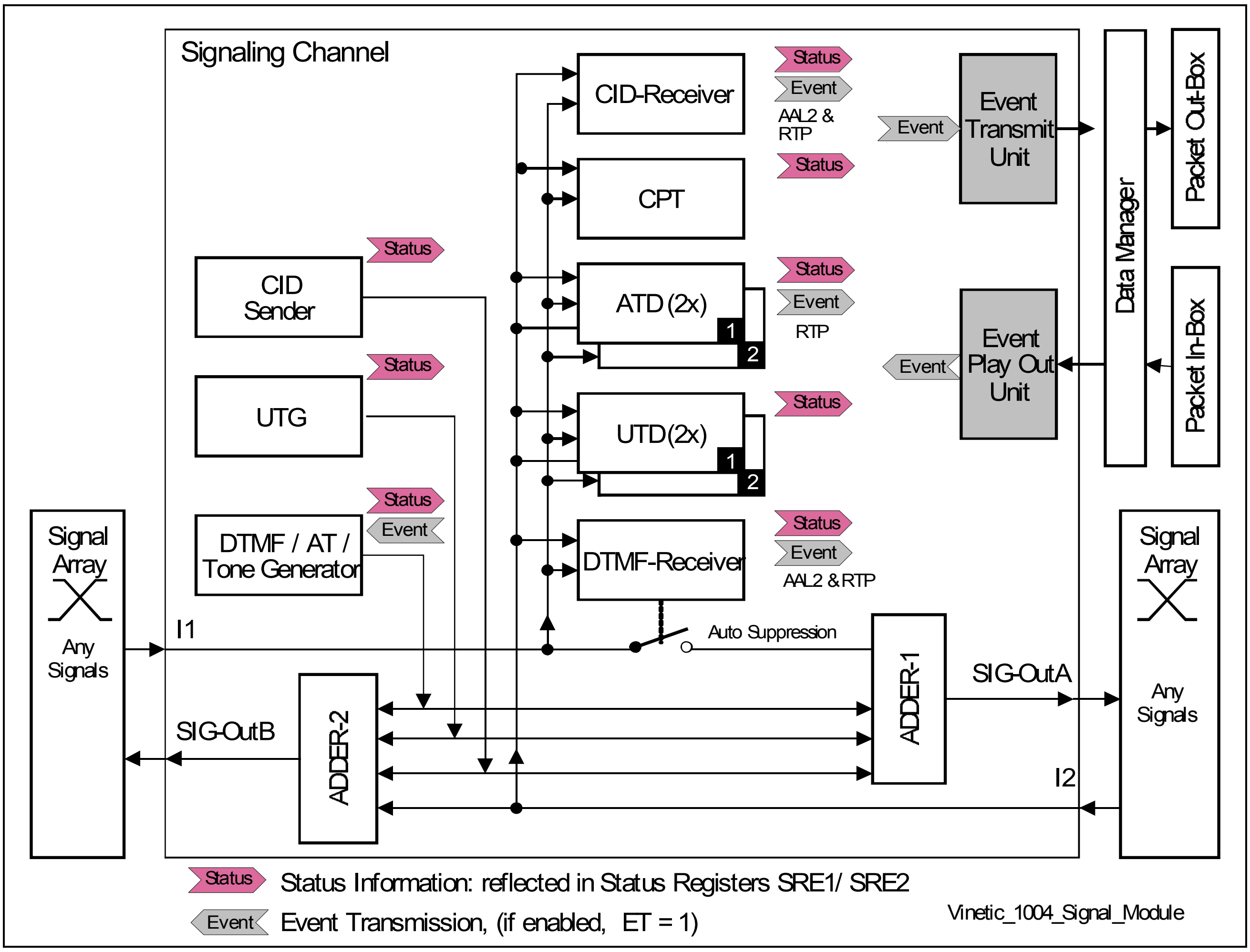


Figure 12 Signaling Module

The **DTMF Receiver** submodule is responsible for detection of DTMF signals. If a valid DTMF key is detected status bits are set and an interrupt is generated. The DTMF Receiver submodule has an early detection mode. This mode can be used to suppress DTMF signals (auto suppression) to avoid double sending of DTMF signals in packet networks. The DTMF Receiver submodule also provides event transmission support for RTP and the AAL2 protocols.

The **answering tone detection** submodules (**ATD1** and **ATD2**) have two different modes: They can detect the answering tone or the signal level. The signal level detection mode is needed for implementing the holding characteristic according to the G.164 specification.
Event transmission support is available for the RTP protocol.

The **universal tone detection** submodules (UTD1, UTD2) supports two different modes: They can detect a sine tone or the signal level. The signal level detection mode-mode is needed for implementing the holding characteristic according to the G.164 specification. Event transmission support is not available for the UTD submodule.

The **DTMF/AT Generator** submodule can generate DTMF signals, alert tones or any other dual tone frequencies. The host can decide, if it wants to program both frequencies independently or to program only a short coding for the DTMF and the AT frequencies. In the latter case the generator uses predefined frequencies. The host can select between two modes: It can control the whole timing by itself or it can use an automatic mode. In case of an automatic mode the host only has to set the frequencies and the generator controls the timing of the tones automatically. The generator supports event transmission also. For event transmission the generator provides two special modes which are optimized for the RTP and AAL2 support.

For the **CID Sender** submodule no event transmission support is available. The host can use the sender to send CID information according to V.23 or Bell 202 to an analog phone. The sender is configurable to cover all country specifications.

The **CID Receiver** can be used for FXO applications and detects FSK signals according to V.23 or Bell 202 standard.

The **Universal Tone Generator** (UTG) can generate a wide variety of tones, allowing also modulated multitones. This is required for howler tone generation and meeting the japanese tone specification.

The **Call Progress Tone Detector** (CPT) tracks in-band notification signals (busy, hang-up,...) and notifies the host accordingly.

Event processing is completely handled by the Event Transmit and the Event Play Out

units:
The **Event Transmit Unit** receives the events from the DTMF Receiver, ATD1 and ATD2, adds the event header and forwards the event to the packet out-box.
The **Event Play Out Unit** reorders the received events and synchronize them with the play out time of the corresponding coder channel (decoder path).

The status information of all submodules are written into the status registers.

7.5 Coder Module

The coder module supports up to 8 channels and has two different interfaces. The interface for the sample based side is the signal array (decoder output and encoder input) and the packet based interface is the packet mailbox. That means for example, that in receive direction a G.723 decoder and in transmit direction a G.729 encoder can be activated.

Each Encoder supports a Voice Activity Detection (VAD). For the VAD either a part of the standard solution or an Infineon proprietary solution can be used. Each decoder supports comfort noise generation (CNG) and packet loss concealment (PLC).

Each channel supports the following features:

- G.723.1 A, G.726 (ADPCM), G.728, G.729 (A, B, E),
- G.711 + Annex I (packet loss concealment), II (VAD/CNG format) encoder and decoder.
- VAD, CNG (for G.711, G.726 VINETIC® provides a proprietary VAD, CNG and signal power estimation)
- Packet Loss Concealment (as described in G.711, Annex I for G.711 and G.726)
- Packetized Voice Protocol Unit, which supports the RTP/RTCP and AAL2 protocol
- Voice Play Out unit (reordering, fixed and adaptive jitter buffer, clock synchronization)
- AGC (Automatic Gain Control)
- Clock synchronization between packet sender and receiver
- Multi-party conferencing
- Gain
- DC HP
- LEC (far end) with NLP for cancelling echoes originating from the packet network
- Decoder controlling via voice packet header
- Status Output
- Fax Datapump V.17, V.19, V.27ter, V.29 for T.38 fax relay

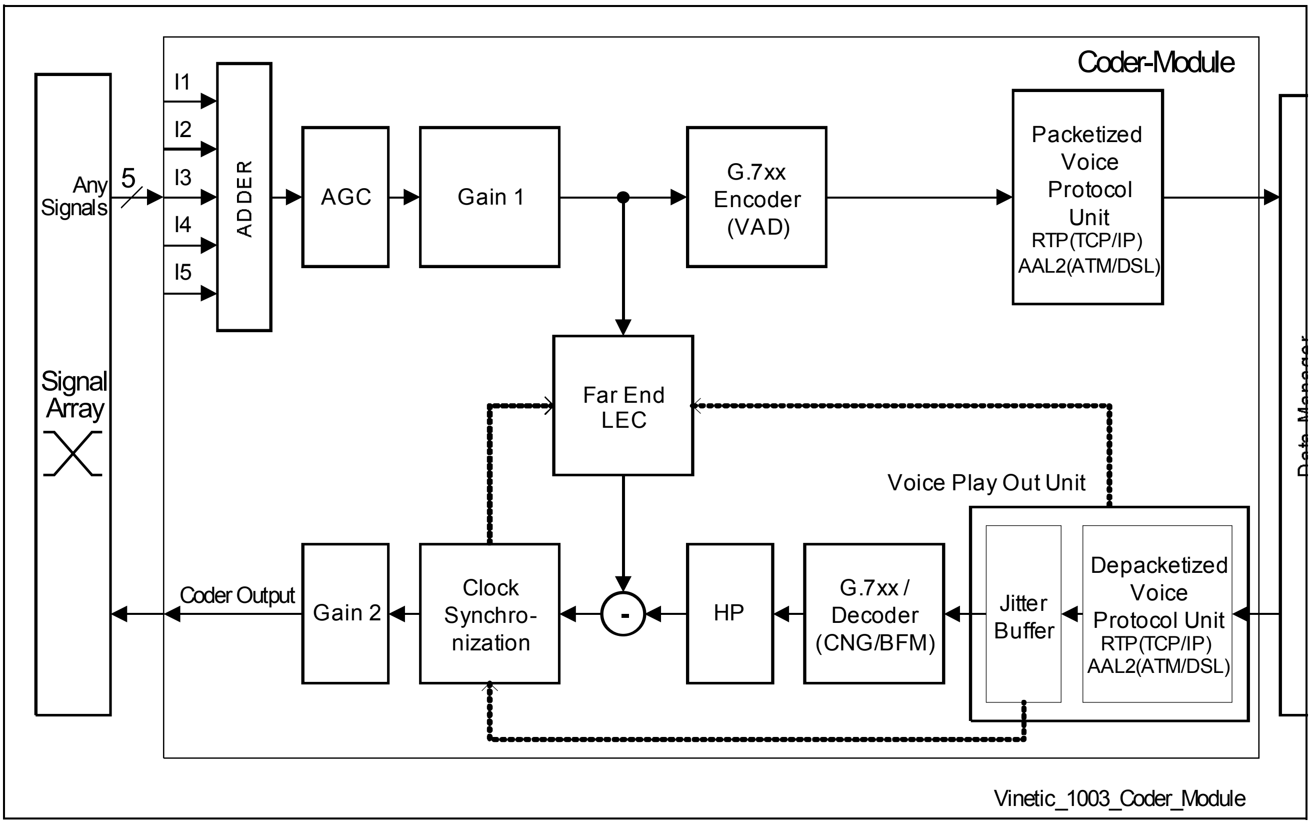


Figure 13 Coder Channel Module

The **AGC** can be used to gain and to limit the level of the input signal. The limitation should prevent clipping of the signal especially to be used with low bitrate encoders.

The **HP** in the decoder direction filters the DC part of the signal.

The far end **LEC** can be used to cancel the echo which occurs via the packet connection.

A global timer for the coder module automatically generates the timestamps for the voice and event packets for all coder and signaling channels.

The **packetized-voice protocol unit** block is responsible for adding (upstream direction) or deleting (downstream direction) a header containing the timestamp, the packet time (PTE) and the coder configuration to the voice data.

The **Voice Play Out** unit is responsible for packet reordering, to estimate the optimum jitter buffer size, to readjust the jitter buffer size, for clock synchronization, and determines the play out times for the received packets. A fixed and an **adaptive jitter buffer** is implemented. The maximum supported jitter buffer size is 200 msec, the granularity for packets is 5 msec.

7.6 Test Features

The following test features have been implemented: a peak detector, test loops, a MIPS meter and a version register.

The **peak detector** can be connected with any signal from the global Signal-Array and any memory location. It allows the search for maximum or minimum values since the last read access from the peak value register.

The **version register** contains the actual hardware and firmware version.

8 Electrical Characteristics

8.1 Operating Range VINETIC®

$V_{GNDA} = V_{GNDB} = V_{GNDC} = V_{GNDD} = V_{GNDAB} = V_{GNDCD} = V_{GNDD} = V_{GNDP} = 0$ V

Table 5 Operating Range VINETIC®

Parameter	Symbol	Limit Value			Unit	Test Condition
		Min.	Typ.	Max.		
Supply pins VDD18, VDD18i referred to the corresp. ground pins GND, GNDi (i = A, AB, B, C, CD, D, P)		1.71	1.8	1.89	V	
Supply pins VDD33, VDD33i referred to the corresp. ground pins GND, GNDi (i = A, AB, B, C, CD, D)		3.14	3.3	3.47	V	
Analog input pins IO2x, IO3x, IO4x, ILx, ITx, VCMITx, ITACx referred to the corresp. ground pins GNDx (x = A, B, C, D)		0	–	3.3	V	V_{DD33i} = 3.3 V
Analog output pins DCPx, DCNx ACPx, ACNx VREFy, VCMy C1x, C2x referred to the corresp. ground pins GNDx, GNDy (x = A, B, C, D, y = AB, CD)		 0.3 0.3 1.3 0	 – – –	 2.7 2.7 1.7 3.3	 V V V V	V_{DD33i} = 3.3 V R_{Load} > 900 Ω R_{Load} > 9 kΩ I_{Load} = ±4 mA I_{Load} < 250 µA
Analog pins for passive devices CDCPx, CDCNx CREFy referred to the corresp. ground pins GNDx, GNDy (x = A, B, C, D, y = AB, CD)		 0 0.5	 – 0.7	 3.3 0.9	 V V	V_{DD33i} = 3.3 V

Table 5 Operating Range VINETIC® (cont'd)

Parameter	Symbol	Limit Value			Unit	Test Condition
		Min.	Typ.	Max.		
Digital input/output pins (I/O pins, GPIO pins)						
High-level input voltage	V_{IH}	2.0		3.6	V	V_{OUT} >=V_{OH} (min)
Low-level input voltage	V_{IL}	– 0.3		0.8	V	V_{OUT} <= V_{OL} (max)
High-level output voltage	V_{OH}	2.4			V	I_{OH} = – 5 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
Input leakage current	I_{IL}			1	µA	V_{DD33} = 3.3 V V_{GND} = 0 V; all other pins are floating; V_{IN} = 0 V
Output leakage current	I_{OZ}			1	µA	V_{DD33} = 3.3 V V_{GND} = 0 V; V_{OUT} = 0 V
Input capacitance at digital signal pins (except IO0x, IO1x, IO2x, IO3x, IO4x; x = A, B, C, D)		–		5	pF	
Input transition rise or fall time at digital signal pins except IO0x, IO1x, IO2x, IO3x, IO4x; x = A, B, C, D)		0	–	5	ns	
Ambient temperature under bias	T_A	–40 0	– –	+85 +85	°C °C	 VINETIC®-2CPE

8.1.1 Power Consumption VINETIC®

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DD18} = V_{DD18A} = V_{DD18AB} = V_{DD18B} = V_{DD18C} = V_{DD18CD} = V_{DD18D} = V_{DD18P}$ = 1.8 V ± 5 %;

$V_{DD33} = V_{DD33A} = V_{DD33AB} = V_{DD33B} = V_{DD33C} = V_{DD33CD} = V_{DD33D}$ = 3.3 V ± 5 %

$V_{GNDA} = V_{GNDAB} = V_{GNDB} = V_{GNDC} = V_{GNDCD} = V_{GNDD} = V_{GNDP}$ = 0 V

Table 6 Power Consumption VINETIC®

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		Min	Typ	Max		
Power consumption in operation modes[1)]						
Deep Sleep	$P_{DDDSleep}$		60		mw	
Sleep all channels	$P_{DDSleep,\ 1.8\ V}$ $P_{DDSleep,\ 3.3\ V}$		70 50		mW mW	(MCLK, PCLK = 2 MHz)
Power down (PDH) all channels	$P_{DDPDH,\ 1.8\ V}$ $P_{DDPDH,\ 3.3\ V}$		70 25		mW mW	
Power Down (PDRH) all channels	$P_{DDPDRH,\ 1.8\ V}$ $P_{DDPDRH,\ 3.3\ V}$		100 80		mW mW	
Active one channel, Power Down (PDH) other channels	$P_{DDAct1,\ 1.8\ V}$		110		mW	VINETIC®-4S
			120[2)]		mW	VINETIC®-4C
			130 - 150[2)]		mW	VINETIC®-4M
			130 - 400[2)]		mW	VINETIC®-4VIP
	$P_{DDAct1,\ 3.3\ V}$		90		mW	all

Table 6 Power Consumption VINETIC® (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		Min	Typ	Max		
Active one channel, Power Down Resistive other channels	$P_{DDAct1,\ 1.8\ V}$	–	120		mW	VINETIC®-4S
			130[2]		mW	VINETIC®-4C
			140 - 160[2]		mW	VINETIC®-4M
			140 - 400[2]		mW	VINETIC®-4VIP
	$P_{DDAct1,\ 3.3\ V}$		120		mW	all
Active 4 channels	$P_{DDAct4,\ 1.8\ V}$		140		mW	VINETIC®-4S
			170[2]		mW	VINETIC®-4C
			200 - 280[2]		mW	VINETIC®-4M
			200 - 400[2]		mW	VINETIC®-4VIP
	$P_{DDAct4,\ 3.3\ V}$		280		mW	all

1) In Active modes the values of both supply rails 3.3 V and 1.8 V have to be added. The power values represent the latest generation. For details on power consumption per version, refer to version specific device datasheet

2) Depends on used EDSP load, representing the enabled features.

8.1.2 Power-Up Sequence VINETIC®

The 3.3V supply has to be applied before the 1.8V supply.

Table 7 Power-Up Sequence VINETIC®

Parameter[1]	Symbol	Limit Value			Unit	Test Condition
		Min.	Typ.	Max.		
Time between power-up of VDD33, VDD33i and VDD18, VDD18j, VDD18P	t_{PU}	0	–	–	ms	

1) i, j = A, AB, B, C, CD, D

Note: No voltage is to be applied to any input or output pin before the VDD33 voltages are applied.

8.2 Operating Range SLIC-S/-S2

Table 8 Operating Range SLIC-S/-S2

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Battery voltage L [1]	V_{BATL}	–60	–15	V	Referred to BGND
Battery voltage H [1]	V_{BATH}	–65	–20	V	Referred to BGND
Auxiliary supply voltage	V_{HR}	3.1	45	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	–	90[2]	V	–
V_{DD} supply voltage	V_{DD}	 4.75 3.1	 5.25 5.5	 V V	referred to AGND SLIC-S V 1.1 SLIC-S V 1.2
Ground voltage difference BGND, AGND	–	–0.4	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	V_{DD}	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	–40	85	°C	–
Junction temperature	T_J	–	125[3]	°C	–

1) If the battery switch is not used, pins VBATL and VBATH should be connected externally. In this case the full voltage range of –15 V to –65 V can be used.

2) This value is identical with the maximum rating value, therefore value must not be exceeded; supply tolerances have to be taken into account. For impact on overvoltage protection see the Application Note *Protection for SLIC-S/-S2 PEB 4264/-2 against Over-Voltages and Over-Currents.*

3) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

8.3 Operating Range SLIC-E/-E2

Table 9 Operating Range SLIC-E/-E2

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Battery voltage L [1]	V_{BATL}	–80	–15	V	Referred to BGND
Battery voltage H [1]	V_{BATH}	–85	–20	V	Referred to BGND
Auxiliary supply voltage	V_{HR}	5	85	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	–	150	V	–
V_{DD} supply voltage	V_{DD}	4.75	5.25	V	Referred to AGND
Ground voltage difference BGND, AGND	–	–0.4	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	3.5	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	–40	85	°C	–
Junction temperature	T_J	–	125[2]	°C	–

1) If the battery switch is not used, pins V_{BATL} and V_{BATH} should be connected externally. In this case the full voltage range of –15 V to –85 V can be used.

2) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

8.4 Operating Range SLIC-P

Table 10 Operating Range SLIC-P

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Battery voltage L[1]	V_{BATL}	–140	–15	V	Referred to BGND
Battery voltage H[1]	V_{BATH}	–145	–20	V	Referred to BGND
Battery voltage R[1]	V_{BATR}	–150	–25	V	Referred to BGND
Total battery supply voltage	$V_{DD} - V_{BATR}$	–	155	V	–
V_{DD} supply voltage	V_{DD}	3.1	5.5	V	Referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	–0.4	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	3.5	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	–40	85	°C	–
Junction temperature	T_J	–	125[2]	°C	–

[1] If only two battery voltages are used, pins VBATL and VBATH should be connected externally.

[2] Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

8.5 Operating Range SLIC-DC

Table 11 Operating Range SLIC-DC

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Supply voltage	VS	9	40	V	with PMOS switch
		9	20	V	with pnp switch
Generated battery voltage	VN	- 90	- 15	V	
Voltage at pins IT, IL	V_{IT}, V_{IL}	- 0.4	3.5	V	
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	
Ambient temperature	T_{amb}	- 40	85	°C	
Junction temperature	T_J	–	125[1)]	°C	

1) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

8.6 Operating Range SLIC-LCP

Table 12 Operating Range SLIC-LCP

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Battery voltage L[1]	V_{BATL}	- 65	- 15	V	Referred to BGND
Battery voltage H[1]	V_{BATH}	- 70	- 20	V	Referred to BGND
V_{DD} supply voltage	V_{DD}	4.5	5.5	V	Referred to AGND
Voltage at pins IT, IL	V_{IT}, V_{IL}	- 0.4	3.5	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	- 40	85	°C	–
Junction temperature	T_J	–	125[2]	°C	–

1) If the battery switch is not used, pins V_{BATL} and V_{BATH} should be connected externally. In this case the full voltage range of –15 V to –70 V can be used.

2) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

8.7 AC Transmission VINETIC®

The AC and DC parameters in Table 13 and Table 14 are valid for a chip set of a *VINETIC®-x* codec and *x* single-channel (*x*/2 dual-channel) SLIC chips.

Table 13 AC Transmission

Parameter	Symbol	Conditions	Limit Values			Unit
			Min.	**Typ.**	**Max.**	
Transmission Performance (2-wire)						
Return loss	RL	200 - 3600 Hz	26	–	–	dB
Frequency Response according to ITU-T Q.552, G.712 and Telcordia TGR-57 requirements						
Idle Channel Noise according to ITU-T Q.552, G.712 and Telcordia GR-57 requirements						
Distortion according to ITU-T Q.552, G.712 and Telcordia GR-57 requirements (Sinusoidal Test Method)						
Longitudinal Balance according to ITU-T O.9						
Longitudinal conversion loss	L-T	300 - 1000 Hz				
		SLIC-S/-E/-P[1)]	53	58	–	dB
		SLIC-S2/-E2	60	65	–	dB
		3400 Hz				
		SLIC-S/-E/-P	52	55	–	dB
		SLIC-S2/-E2	56	59	–	dB
Input longitudinal interference loss	L-4	300 - 1000 Hz				
		SLIC-S/-E/-P	53	58	–	dB
		SLIC-S2/-E2	60	65	–	dB
		3400 Hz				
		SLIC-S/-E/-P	52	55	–	dB
		SLIC-S2/-E2	56	59	–	dB
TTX Signal Generation						
TTX signal	V_{TTX}	at 200 Ω	–	–	2.5	Vrms

Table 13 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			Min.	Typ.	Max.	
Group Delay (please refer to *Preliminary User's Manual - System Reference*)						

1) SLIC version used in the chip set (system). Also TSLIC-S and TSLIC-E possible.

8.8 DC Characteristics

T_A = –40 °C to 85 °C, unless otherwise stated.

Table 14 DC Characteristics

Parameter	Symbol	Conditions	Limit Values			Unit
			Min.	Typ.	Max.	
Line Termination Tip, Ring						
Sinusoidal Ringing						
Max. ringing voltage	V_{RNG0}	$V_{HR} - V_{BATH}$ = 150 V, V_{DC} = 20 V for ring trip (SLIC-E/-E2)	85	–	–	Vrms
		$-V_{BATR}$ = 150 V, V_{DC} = 20 V for ring trip (SLIC-P)	85	–	–	Vrms
		$V_{HR} - V_{BATH}$ = 85 V, V_{DC} = 15 V for ring trip (SLIC-S/-S2)	45	–	–	Vrms
Trapezoidal Ringing						
Max. ringing voltage (Crest factor = 1.2)	V_{RNG0}	$V_{HR} - V_{BATH}$ = 150 V, V_{DC} = 20 V for ring trip (SLIC-E/-E2)	100	–	–	Vrms
		$-V_{BATR}$ = 150 V, V_{DC} = 20 V for ring trip (SLIC-P)	100	–	–	Vrms
		$V_{HR} - V_{BATH}$ = 85 V, V_{DC} = 15 V for ring trip (SLIC-S/-S2)	52	–	–	Vrms

Table 14 DC Characteristics (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			Min.	Typ.	Max.	
Output impedance	R_{OUT}	SLIC output buffer and R_{STAB}	–	61	–	Ω
Harmonic distortion	THD	–	–	–	5	%
Output current limit	$\|I_{R, max.}\|$, $\|I_{T, max.}\|$	SLIC-E/-E2: Active Modes	80	105	130	mA
		SLIC-S/-S2: Active Modes	75	95	115	mA
		SLIC-P Version 1.2: Active Modes, HIT, HIR (C3 = L)[1]	45	60	75	mA
		SLIC-P Version 1.2: Active Modes, ROR, ROT (C3 = H)[1]	70	90	110	mA
Loop current gain accuracy	–	–	–	–	3	%
Loop current offset error[2]	–	–	–0.75	–	0.75	mA
Loop open resistance TIP to BGND	R_{TG}	Power Down Mode I_T = 2 mA, T_A = 25 °C	–	5	–	kΩ
Loop open resistance RING to V_{BAT}	R_{BG}	Power Down Mode I_R = 2 mA, T_A = 25 °C	–	5	–	kΩ
Ring trip DC voltage	–	SLIC-E/-E2/-S/-S2: SLIC-P: balanced SLIC-P: unbalanced	0 0 –	– – $V_{BATR}/2$	30 30 –	Vdc Vdc Vdc
Ring trip detection time delay	–	Standard ring trip detection DC, AC (RTR-FAST = 0) Fast ring trip detection (RTR-FAST = 1)	– –	– –	2 0.5	cycle cycle
Ring off time delay	–	–	–	–	2	cycle

1) Current limitation controlled at SLIC-P pin C3 by the VINETIC® pin IO0

2) Can be reduced with current offset error compensation.

9 Application Circuits

9.1 Internal Ringing (Balanced/Unbalanced)

Internal balanced ringing is supported up to 85 Vrms for systems with SLIC-E/-E2/-P and up to 45 Vrms for systems with SLIC-S. SLIC-P also allows internal unbalanced ringing up to 50 Vrms without any additional external components.

9.1.1 Application Circuits for Internal Ringing

All application circuits show only one channel (A) for the VINETIC®/SLIC interface and for the ring/tip lines.

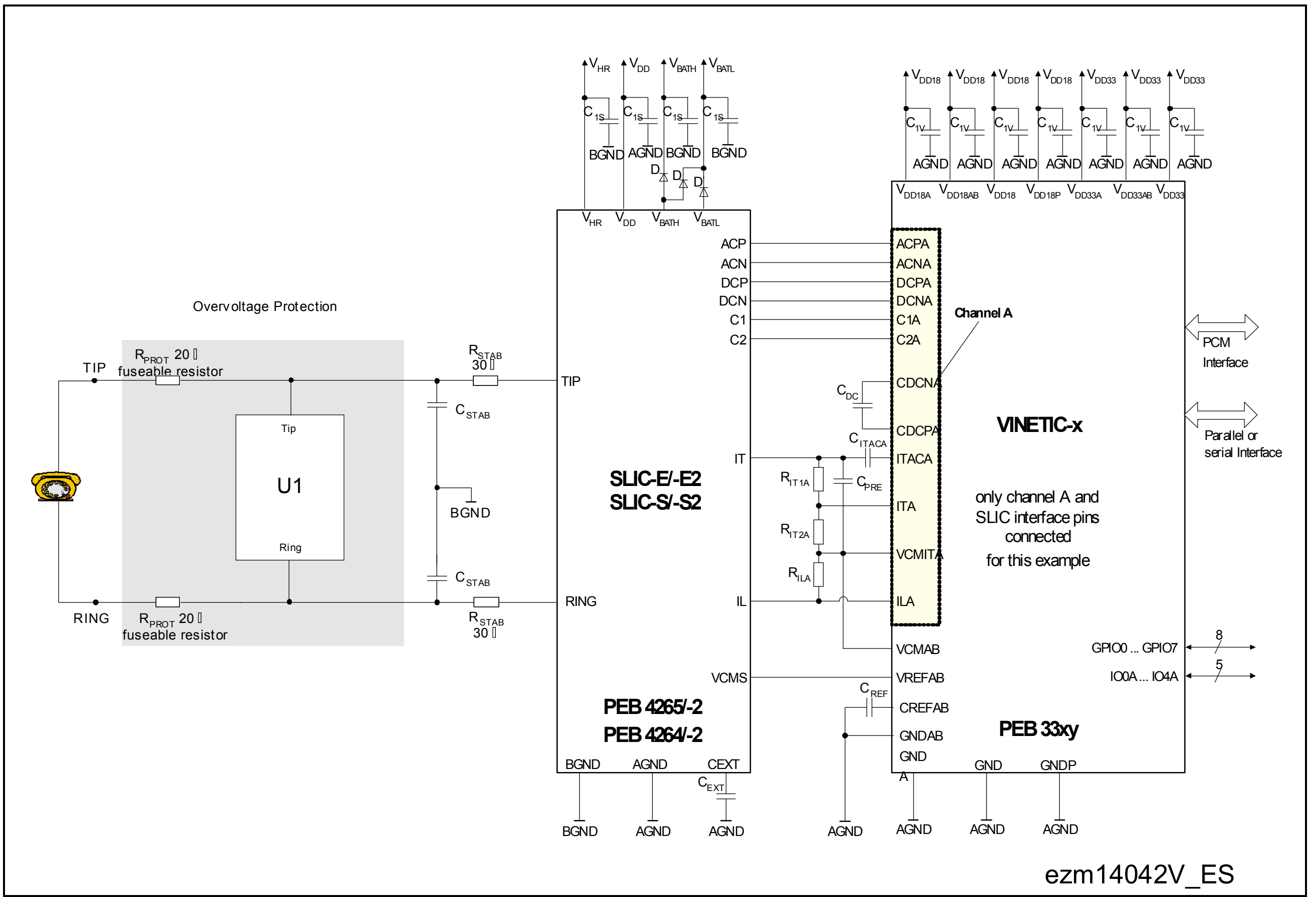


Figure 14 Application Circuit Internal Ringing (balanced) for SLIC-E/-S

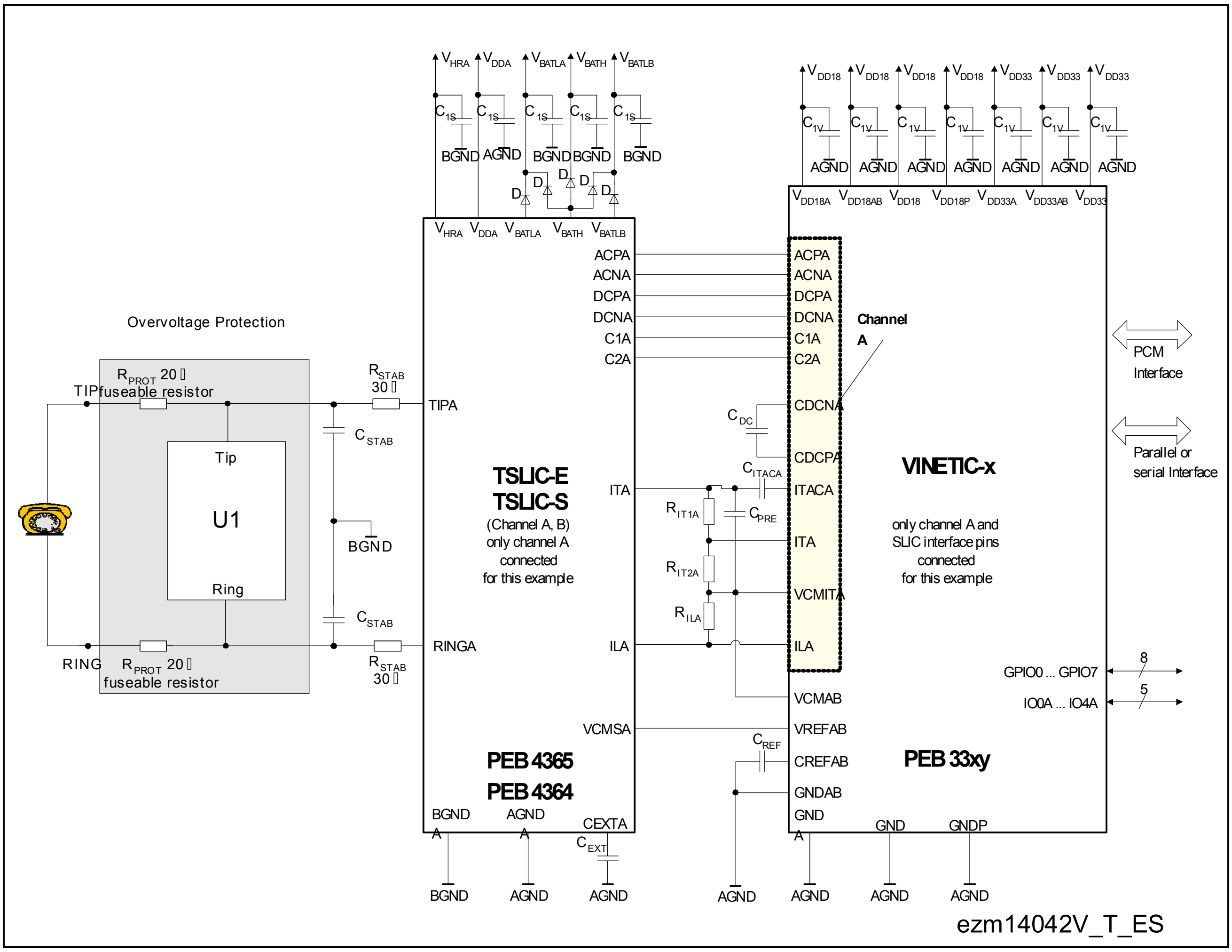


Figure 15 Application Circuit Internal Ringing (balanced) for TSLIC-E/-S

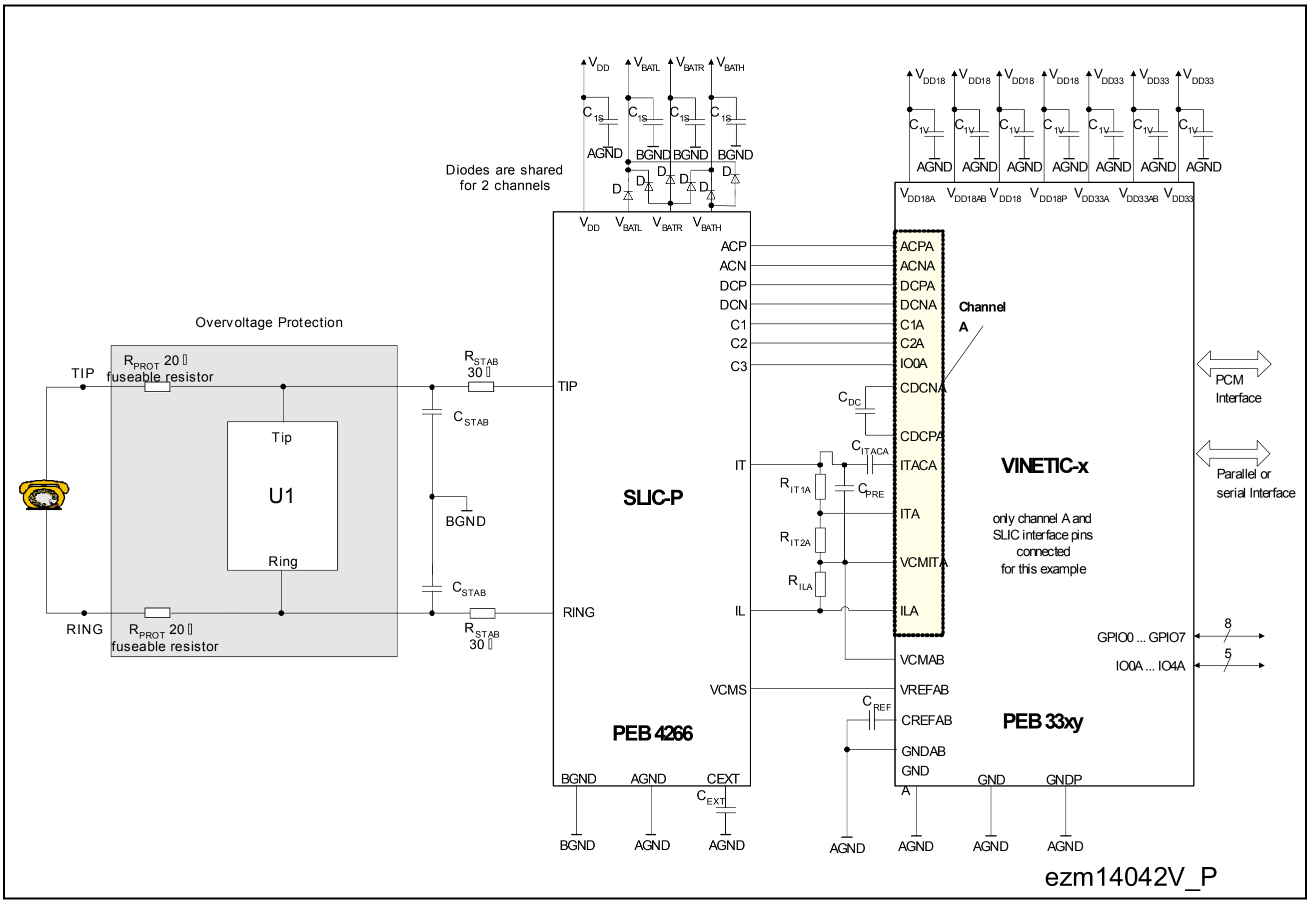


Figure 16 Application Circuit Internal Ringing (bal. & unbal.) for SLIC-P

As **Figure 16** shows, balanced and unbalanced internal ringing use the same line circuit.

9.1.2 Bill of Materials

Table 15 shows the external passive components needed for a complete four channel solution with protection consisting of one VINETIC®-4x and four SLIC-E/-E2/-S/-P or two TSLIC-E/TSLIC-S devices.

Table 15 External Components in Application Circuit for 4 Channels

No.	Symbol	Value	Unit	Tol.	Rating	SLIC-E/-S Systems	TSLIC-E/-S Systems	SLIC-P Systems
4	R_{IT1}	510	Ω	1 %		x	x	x
4	R_{IT2}	680	Ω	1 %		x	x	x
4	R_{IL}	1.6	kΩ	1 %		x	x	x
8	R_{STAB}	30	Ω	1 %[1]		x	x	x
8	R_{PROT}[2]	20	Ω	1 %[1]	see [3]	x	x	x
8	C_{STAB}	15 (typ.)	nF	10 %	see [4]	x	x	x
4	C_{DC}	220	nF	10 %	10 V	x	x	x
4	C_{ITAC}	1	µF	10 %	10 V	x	x	x
2	C_{REF}	68	nF	20 %	10 V	x	x	x
4	C_{EXT}	470	nF	20 %	10 V	x	x	x
4	C_{PRE}	18	nF	5 %	10 V	x	x	x
20	C_{1S}	typ. 100[5]	nF	10 %	see [6]	x	x	x
21	C_{1V}	typ. 100[5]	nF	10 %	10 V	x	x	x
12	D[7]	BAS21	–	–	–	x		x
10	D[7]	BAS21	–	–	–		x	
4	U_1[2]	Overvoltage Element	–	–	–	x	x	x

1) Matching tolerance dependent on longitudinal balance requirements (for details see the Application Note "External Components")

2) For protection see the Application Note *Protection of DuSLIC®/VINETIC® Linecard Chip Sets against Overvoltages and Overcurrents*.

3) Exact value depends on system requirements (e.g. coordination with primary protector)

4) According to the highest used battery voltage $|V_{BATR}|$ for SLIC-P and $|V_{HR}|$ or $|V_{BATH}|$ for SLIC-E/-E2/-S

5) Depends on layout considerations

6) Voltage rating according to the battery voltage V_{HR}, V_{BATL}, V_{BATH}, V_{BATR}

7) only needed when VBATH and VBATL are different voltages; the diodes ensure that V_{BATL} is more positive than V_{BATH} and in case of SLIC-P, V_{BATH} is more positive than V_{BATR}

9.1.3 Application Circuits for Internal Ringing with DC/DC

Figure 17 shows an example for a typical low-cost application of SLIC-DC in the P-DSO-24 package with a pnp-type switching transistor. By using a PMOS switch, efficiency could be slightly improved. The DC/DC part is dimensioned to allow dynamic ring voltage tracking. In **Table 16** typical values of the external components are listed.

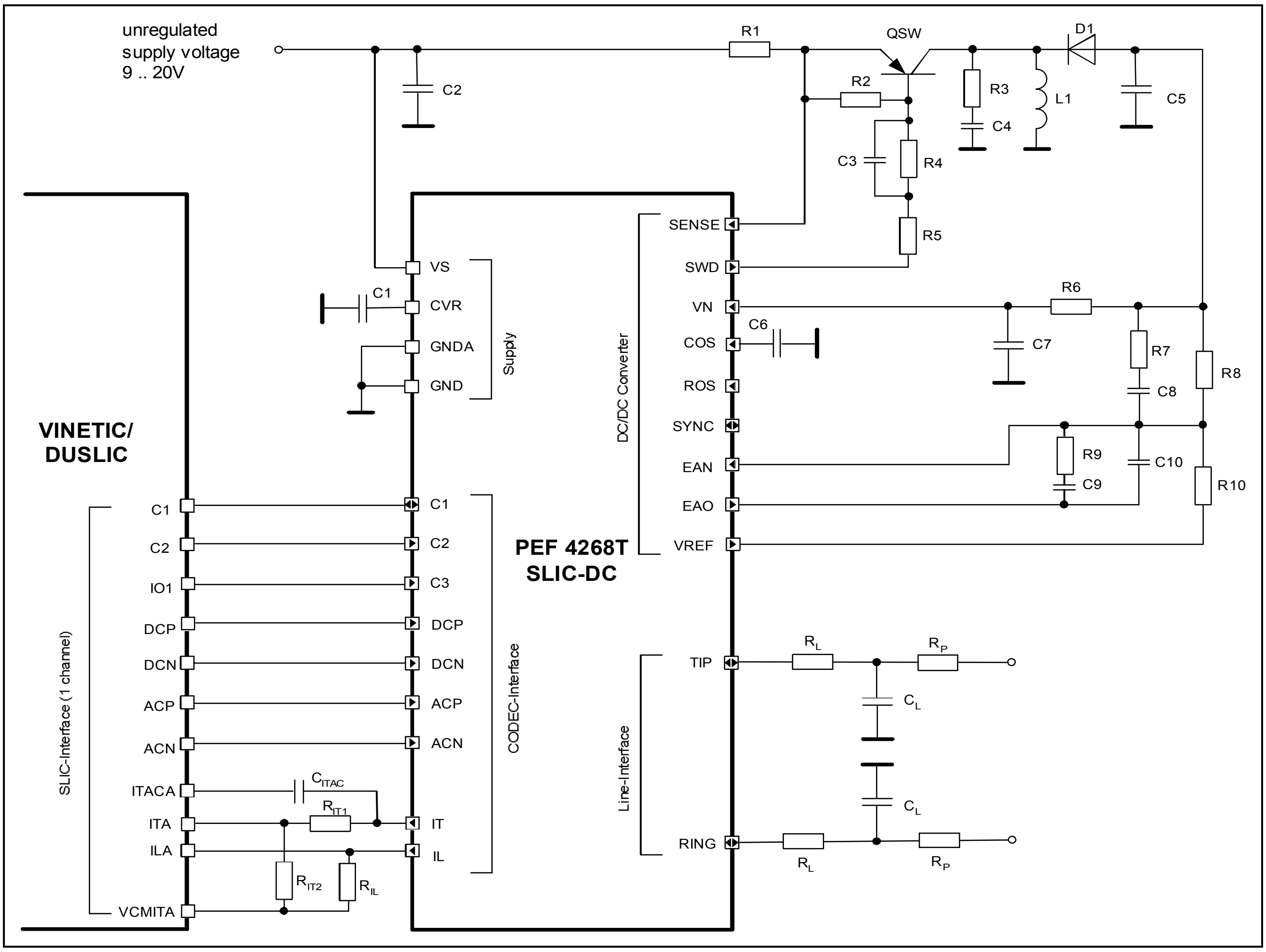


Figure 17 Application Circuit Internal Ringing with DC/DC

Table 16 Components for SLIC-DC Application Circuit

	Symbol	Function	typ. Value	Unit	Tolerance	Rating
2	R_L	overcurrent limitation. stability	20	Ω	1 % (rel.)	
2	C_L	EMC filtering	18	nF	5 % (rel.)	100 V
2	R_P	overcurrent limitation, EMC filtering	20	Ω	1 % (rel.)	
1	R_{IT1}	IT current/voltage conv. AC	510	Ω	1 %	
1	R_{IT2}	IT current/voltage conv. DC	680	Ω	1 %	
1	R_{IL}	IL current/voltage conv.	3.3	kΩ	1 %	

Table 16 Components for SLIC-DC Application Circuit (cont'd)

	Symbol	Function	typ. Value	Unit	Tolerance	Rating
1	C_{ITAC}	AC separation on IT	1	µF	10 %	10 V
1	C1	internal positive supply voltage filtering	47	nF	10 %	10 V
1	C2	VS supply filtering	100	nF	10 %	100 V
1	C6	switching frequency setting	82	pF	5 %	
1	QSW	switching transistor (pnp)				Zetex FZT 955 or equivalent
(1)	QSW	alternative switching transistor (PMOS)				Int. Rectifier IRF 6216 or equivalent
1	R1	current limitation	220	mΩ	5 %	0.5W
1	R2[1)]	base-emitter discharging resistor	180	Ω	5 %	
1	R5	base current limitation	47	Ω	5 %	
1	R4[1)]	DC base current limitation	680	Ω	5 %	
1	C3[1)]	base current highpass filter	33	nF	10 %	
1	R3	damping of overshoots	100	Ω	5 %	1kΩ with PMOS
1	C4	damping of overshoots	330	pF	10 %	
1	L1	DC/DC inductor	33	µH	10 %	I_{peak} = 2A
1	D1	DC/DC diode				150V, 1A, e.g. MURS 120
1	C5	DC/DC capacitance	1	µF	10 %	low ESR
1	R8	output voltage divider	715	kΩ	1 %	
1	R10	output voltage divider	18	kΩ	1 %	
1	R7	smoothing of VN transients	470	kΩ	5 %	
	C8	smoothing of VN transients	22	pF	10 %	
1	R6	VN filtering	20	Ω	5 %	
1	C7	VN filtering	1	µF	10 %	
1	R9	error amplifier loop filter	470	kΩ	5 %	
1	C9	error amplifier loop filter	120	pF	10 %	
1	C10	error amplifier loop filter	82	pF	10 %	

1) with pnp type switch only

9.2 External Ringing

With SLIC-E/-E2/-P external ringing is supported, however for US market with external ringing, the SLIC-LCP is the most suitable device, as it also provides an automatic longitudinal balance adaptation. This reduces BOM cost while maintaining a very good longitudinal balance.

Figure 18 shows a typical line interface with SLIC-LCP. An electronic switch (LCAS, e.g. Clare CPC 75xx) serves as the ring relay. The external components are listed in **Table 17** (for details on overvoltage protection please refer to the respective Application Note).

Note: For stability reasons, PCB must be designed with minimum parasitic capacitances at the TIP-S and RING-S pins; values below 10 pF are recommended.

Table 17 External Components

Quant.	Symbol	Function	Typ. Value	Unit	Tolerance /Matching	Rating
2	R_S	stability, overcurrent limitation	30	Ω	1 %	
2	R_{FB}	longitudinal balance feedback	200	kΩ	5 %	e.g. MELF resistors[1)]
2	C_L	EMC filtering	10	nF	10 %	100 V
2	R_{RT}	Ring trip voltage divider	750	kΩ	1 %	
1	R_{Sense}	Rring current sense resistor	330	Ω	1 %	
1	R_{IT1}	IT current/voltage conv. AC	510	Ω	1 %	
1	R_{IT2}	IT current/voltage conv.	680	Ω	1 %	
1	R_{IL}	IL current/voltage conv. AC	1.6	kΩ	1 %	
1	C_{EXT}	Common mode output voltage filtering	470	nF	20 %	10 V
1	C_{BATL}, C_{BATH}	Supply voltage blocking	100	nF	20 %	100 V
1	C_{ITAC}	AC separation on IT	1	µF	10 %	10 V
1	C_{PRE}	IT lowpass (only necessary with 12/16 kHz metering)	18	nF	5 %	10 V
1	C_{DC}	DC lowpass filtering	220	nF	10 %	10 V
1	C_{REF}		68	nF	20 %	10 V
3	D1, D2, D3	Substrate overvoltage protection	BAS21			
1	LCAS	Linecard Access Switch (electronic ring relay)				e.g. CPC 75xx

Table 17 External Components

Quant.	Symbol	Function	Typ. Value	Unit	Tolerance /Matching	Rating
1	OVP	Overvoltage Protection				e.g. gate triggered thyristor integrated in LCAS)[2]
2	OCP	Overcurrent Protection				e.g. LFR, fuse, PTC[1]

1) depending on overvoltage requirements

2) depending on overvoltage requirements

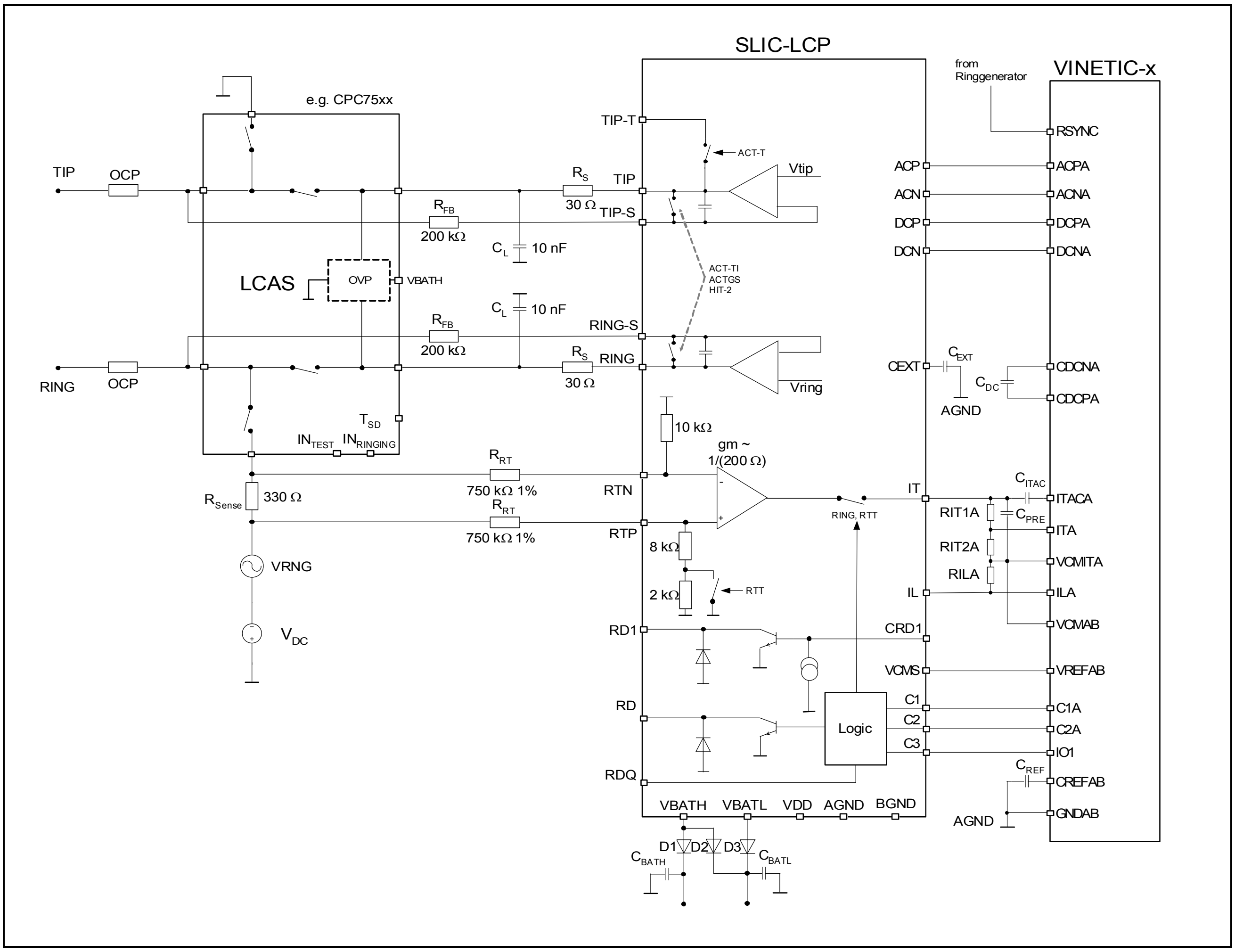


Figure 18 Application Circuit External Ringing for SLIC-LCP

10 Package Outlines

P-DSO-20-5
(Plastic Dual Small Outline)

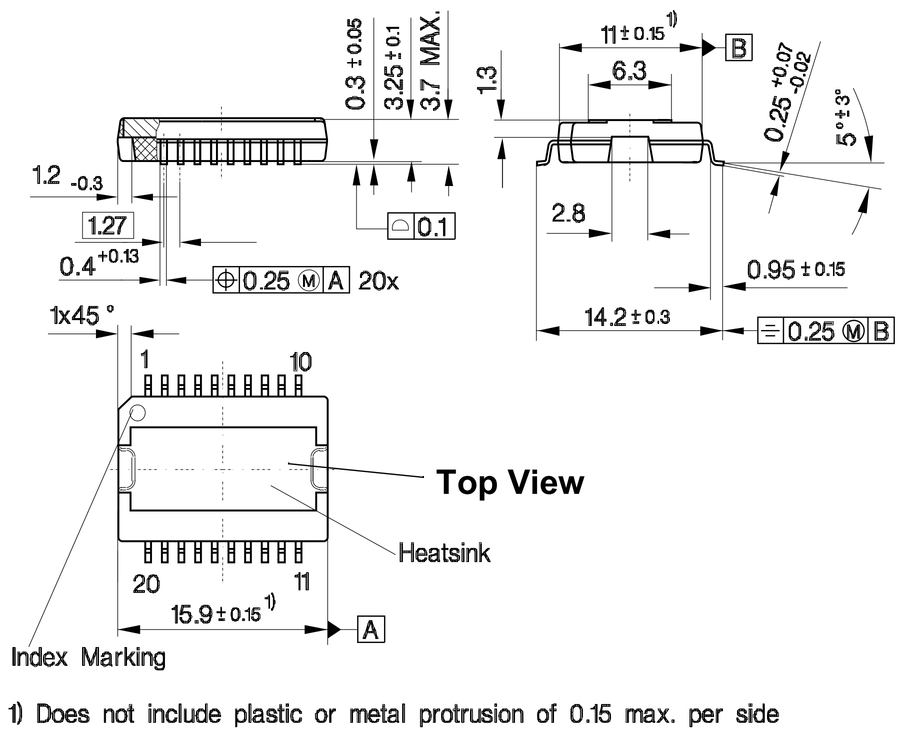


Figure 19 SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB 426x)

Note: The P-DSO-20-5 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).

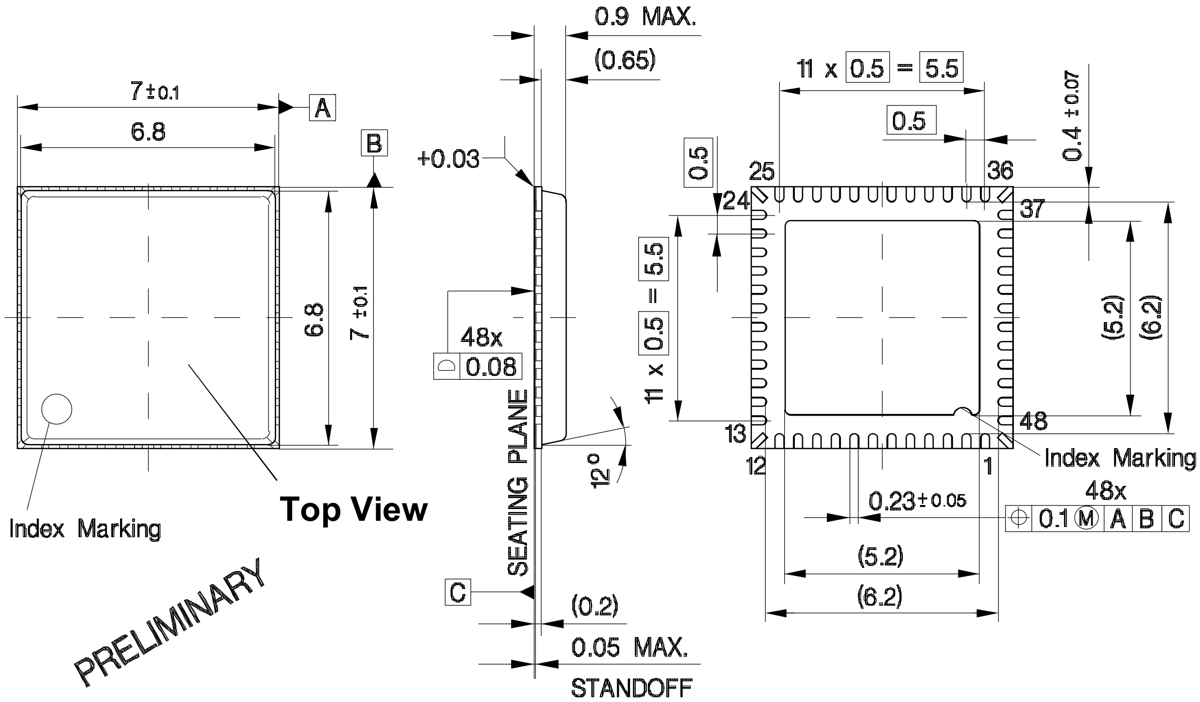
Attention: The heatsink is connected to VBATH (VBATR) via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH (BGND and VBATR), touching of the heatsink or any attached conducting part can be hazardous. It must be electrically insulated from other parts or board connections.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

P-VQFN-48-4
(Plastic Very Thin Profile Quad Flat Non Leaded)



gvq09350

Figure 20 SLIC-S/-S2, SLIC-E/-E2, SLIC-P (PEB426x), SLIC-LCP (PEB 4262)

Note: The P-VQFN-48-4 package is only available with heatsink on bottom.

Attention: The exposed die pad and die pad edges are connected to VBATH (VBATR) via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH (VBATR and BGND), touching of the die pad or any attached conducting part can be hazardous. It must be electrically insulated from other parts or board connections.

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SMD = Surface Mounted Device

Dimensions in mm

P-DSO-36-15
(Plastic Dual Small Outline)

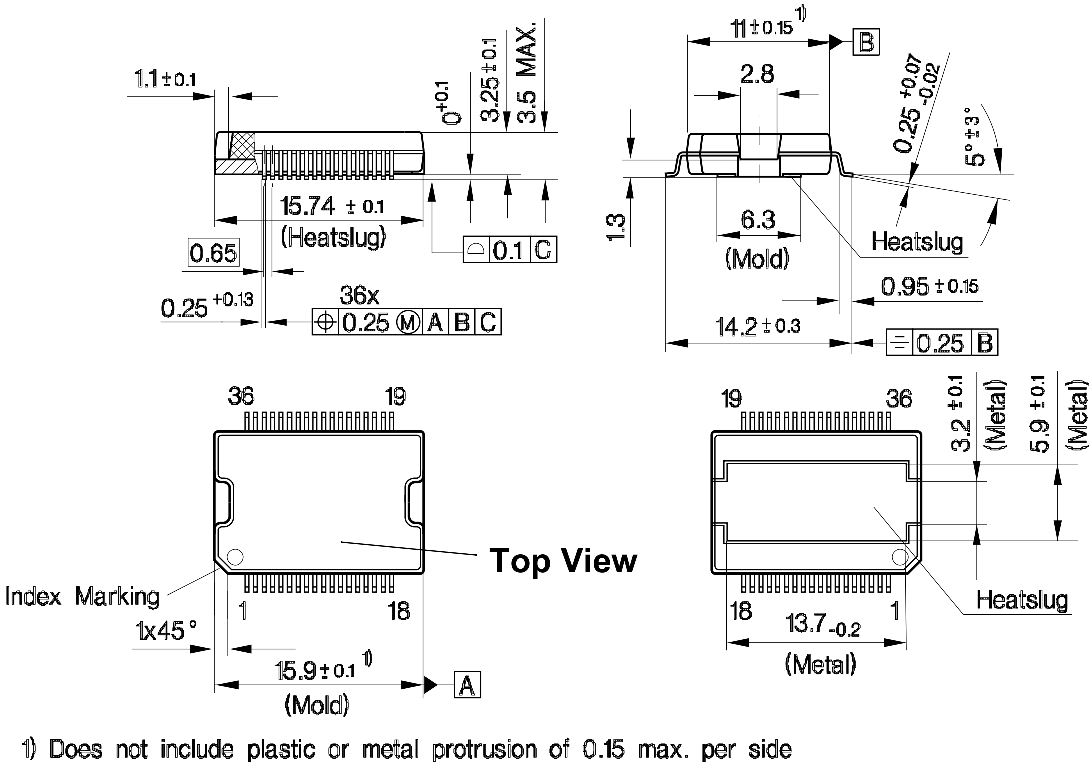

Figure 21 TSLIC-S (PEB 4364), TSLIC-E (PEB 4365)

Note: The P-DSO-36-15 package is available with heatsink on bottom.

Attention: The heatslug is connected to VBATH via the chip substrate. Due to the high voltages of up to 150 V between VHRA (VHRB) and VBATH, touching of the heatslug or any attached conducting part can be hazardous. It must be electrically insulated from other parts or board connections.

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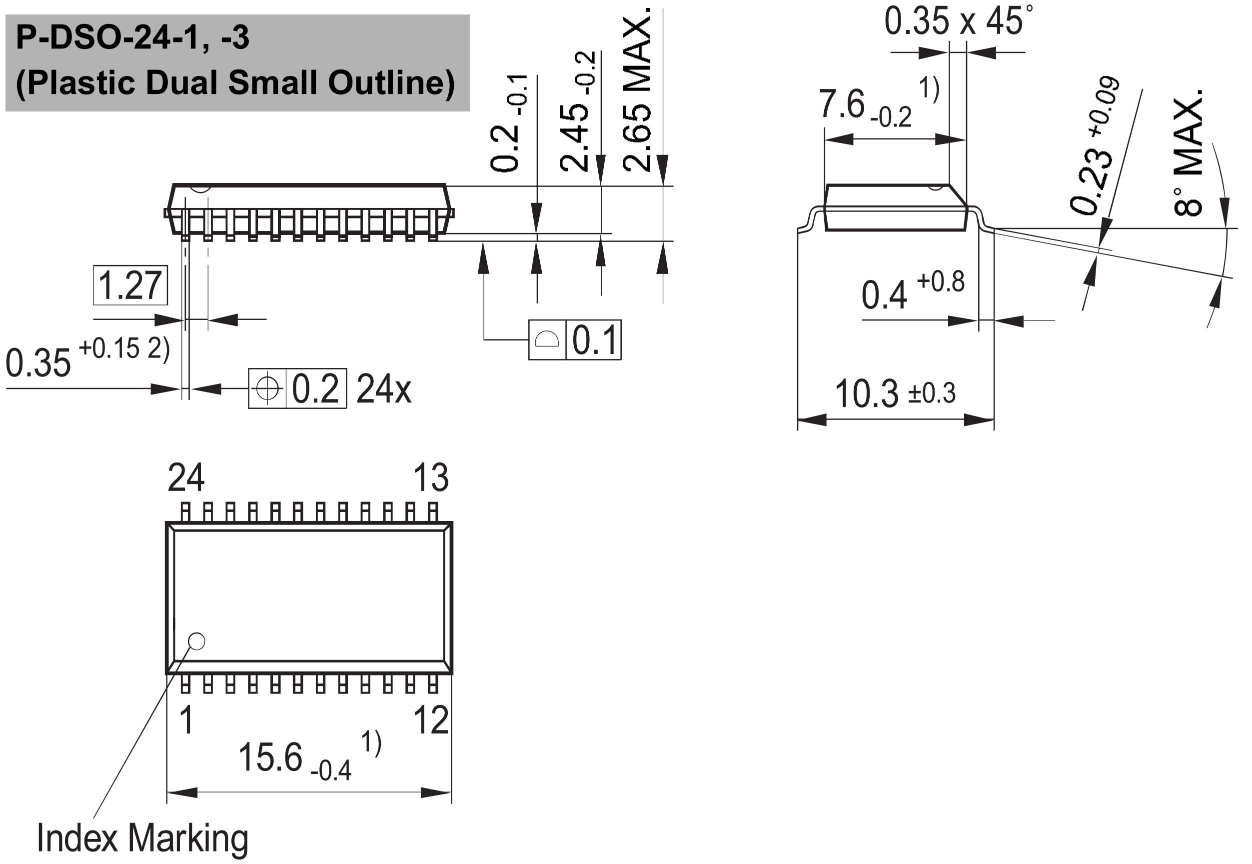
SMD = Surface Mounted Device

Dimensions in mm

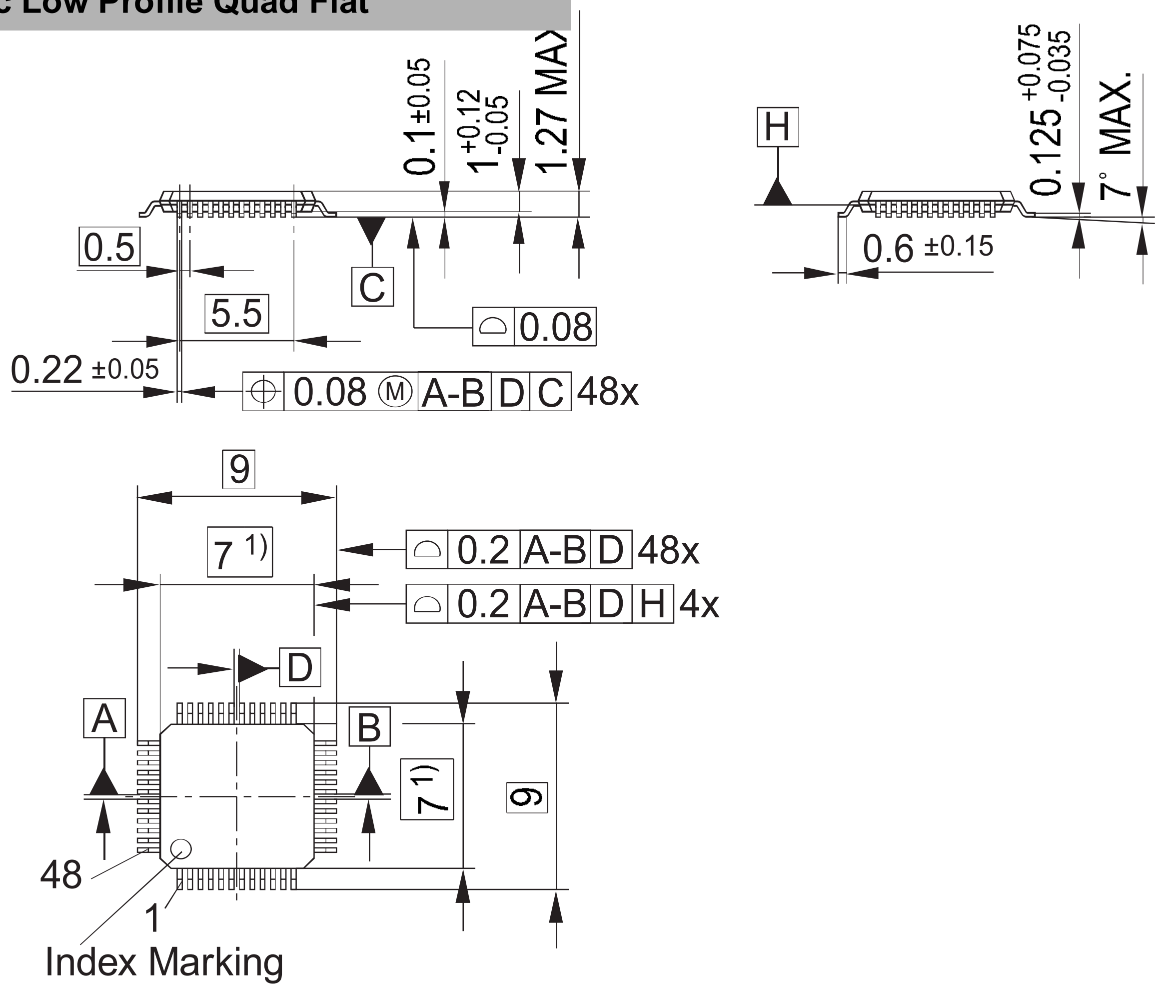
P-DSO-24-1, -3
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

Figure 22 SLIC-DC (PEB 4268)

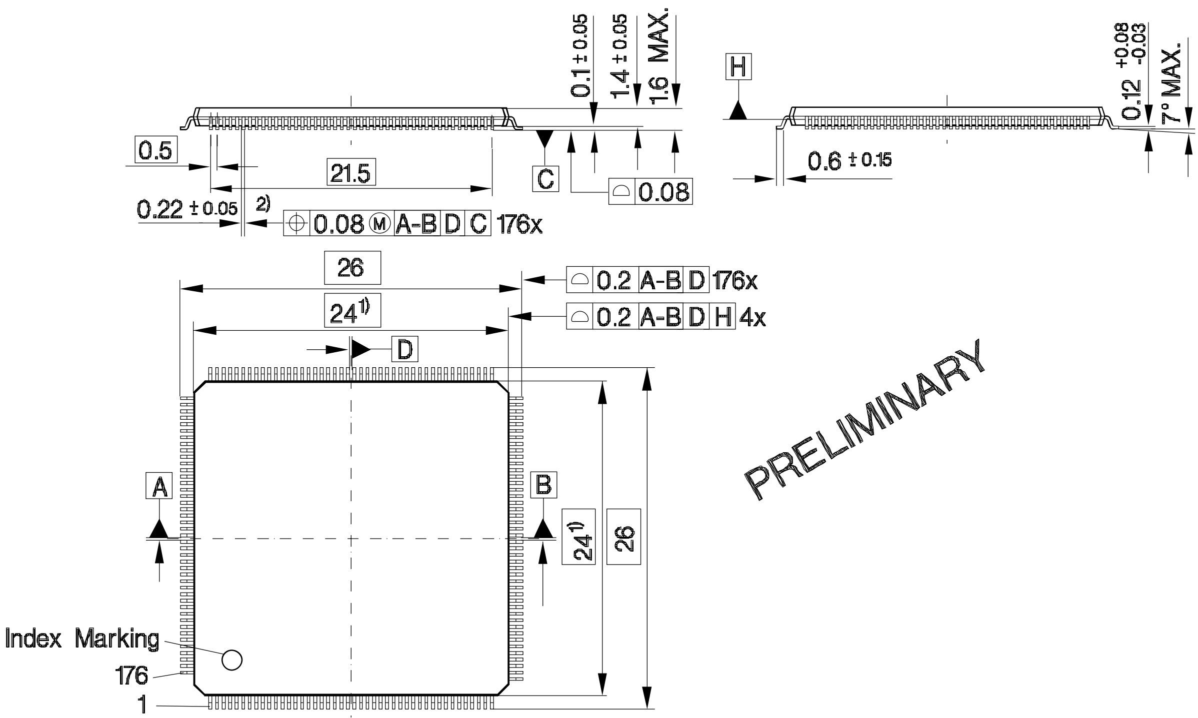
P-TQFP-48-1
(Plastic Low Profile Quad Flat



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 23 SLIC-DC (PEB 4268)

P-LQFP-176-2
(Plastic Low Profile Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPP09451

Figure 24 VINETIC®-4x (PEB33x4HL), VINETIC®-2VIP (PEB 3322HL) and VINETIC®-0 (PEB3320HL)

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SMD = Surface Mounted Device

Dimensions in mm

P-LBGA-176-3
(Plastic Low Profile Pitch Ball Grid Array Package)

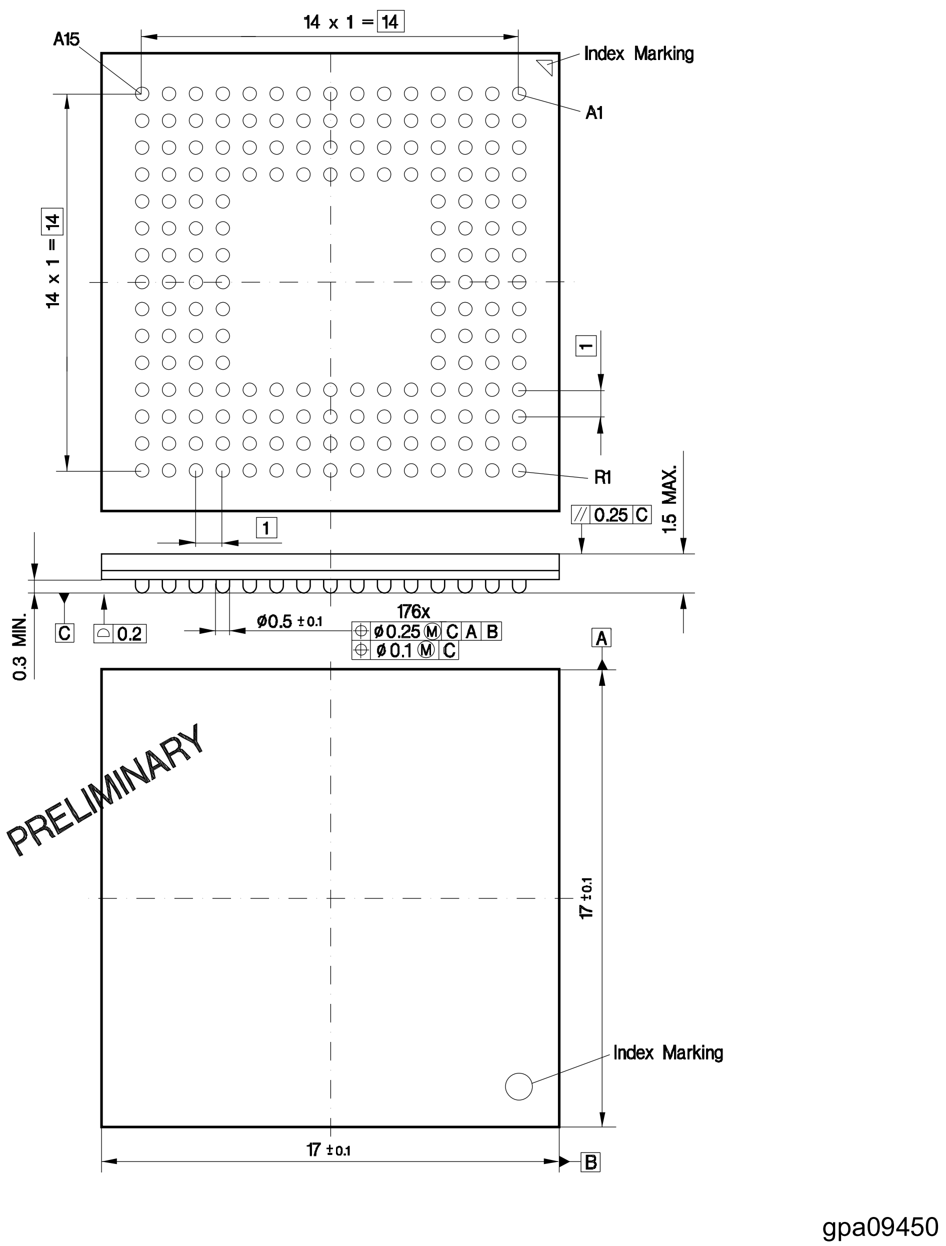

Figure 25 VINETIC®-4x (PEB33x4E), VINETIC®-2VIP (PEB 3322E) and VINETIC®-0 (PEB3320E)

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SMD = Surface Mounted Device

Dimensions in mm

PG-LBGA-144
(Plastic Low Profile Pitch Ball Grid Array Package)

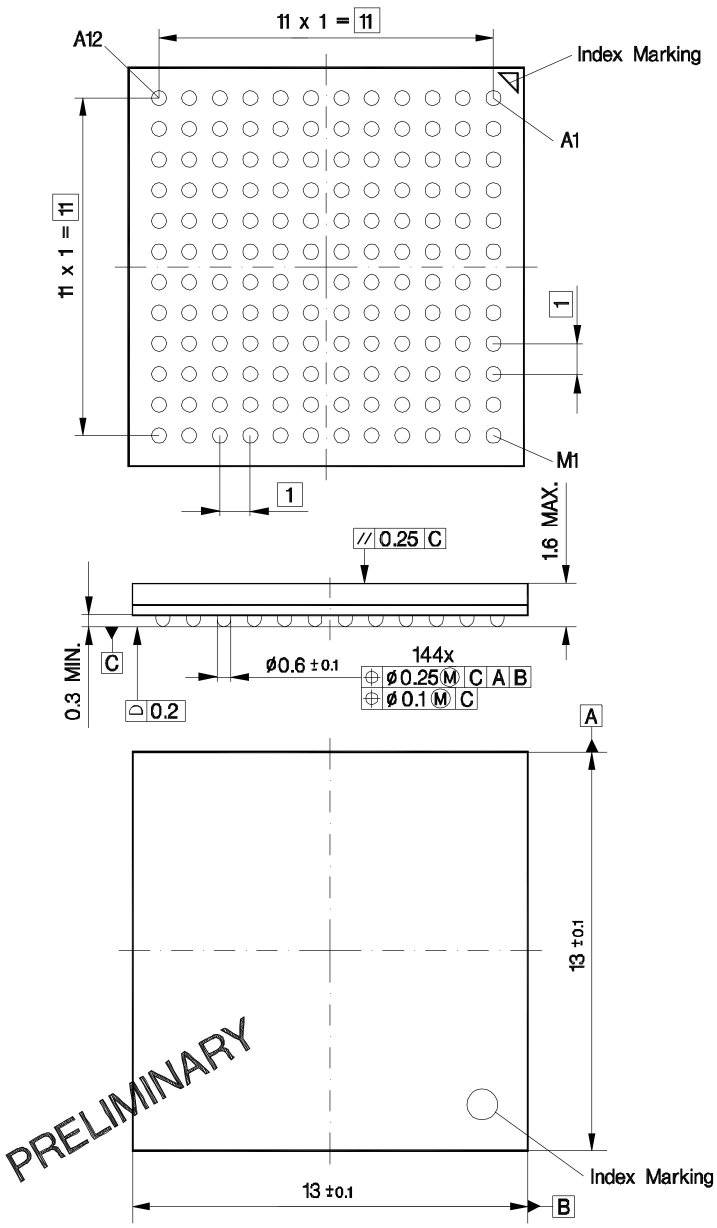

Figure 26 **VINETIC®-2CPE (PEB 3332), VINETIC®-4M (PEB 3314), VINETIC®-4C (PEB 3394), VINETIC®-4S(PEB 3304)**

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SMD = Surface Mounted Device

Dimensions in mm

11 Terminology

A	
A/D	Analog to digital
AAL2	ATM Adaption Layer 2
AC	Alternative Current
ADC	Analog Digital Converter
AITDF	Advanced Integrated Test and Diagnostic Functions
ATD	Answering Tone Detector
ATM	Asynchronous Transfer Mode
C	
CAS	Channel Associated Signaling
CNG	Comfort Noise Generation
Codec	Coder Decoder
CPE	Customer Premises Equipment
D	
DAC	Digital Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency
E	
EDSP	Enhanced Digital Signal Processor
F	
FSK	Frequency Shift Keying
G	
GPIO	General Purpose Input / Output
H	
HW	Hardware
I	
IAD	Integrated Access Device
ITU	International Telecommunication Union
IP	Internet Protocol

ISDN	Integrated Services Digital Network
J	
JTAG	Joint Test Action Group
L	
LSSGR	Local area transport access Switching System Generic Requirements
N	
NG-DLC	Next Generation Digital Loop Carrier
NT	Network Terminal
P	
PBX	Private Branch eXchange
PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
R	
RAM	Random Access Memory
RBS	Robbed Bit Signaling
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
S	
SLIC	Subscriber Line Interface Circuit
T	
TG	Tone Generator
TS	Time Slot
TTX	Teletax
U	
UTD	Universal Tone Detection
V	
VAD	Voice Activity Detection
VINETIC®	Voice and Internet Enhanced Telephony Interface Concept
VINETICOS	Voice and Internet Enhanced Telephony Interface Concept Coefficients Software
VoATM	Voice over ATM
VoDSL	Voice over DSL

VoIP	Voice over IP

X

xDSL	(all flavors of) Digital Subscriber Line

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