# QIHPC
# QUAD ISDN/S(H)DSL High Voltage Power Controller

PEF 2426 Version 1.1

Wired Communications

**Infineon** technologies

N e v e r   s t o p   t h i n k i n g .

# QIHPC

# QUAD ISDN/S(H)DSL High Voltage Power Controller

PEF 2426 Version 1.1

Wired
Communications

Infineon
technologies

N e v e r   s t o p   t h i n k i n g .

**PEF 2426**

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

**Table of Contents** **Page**

## List of Figures                                                        **Page**

**List of Tables**                                                       **Page**

# 1 Overview

The QUAD ISDN/S(H)DSL High Voltage Power Controller provides a power source for up to four U-line interfaces or S-interfaces. The power source to the device is a local battery or a centralized power supply.

Each powered line is individually controlled and monitored by the device interface. Line powering can be switched on or off by command. The QIHPC indicates, when the output current is above a threshold for longer than the programmable time $t_{OC}$. At a second (higher) value the current is limited. The values of the current limitation and the overcurrent indication threshold are defined with external resistors, the overcurrent indication setup delay is selected by external capacitances.

The status information of each line (acknowledge of requested power feed) is returned to the system. The status information enables an easy detection of overloads and faults and a fast localization even on a large system.

The integrated intelligent chip temperature control guards the QIHPC in case of overloads.

Additionally eight drivers for external relays and their control logic are integrated on the QIHPC. These relay drivers provide open collector output stages with high current capability.

# QUAD ISDN/S(H)DSL High Voltage Power Controller    PEF 2426
QIHPC

## 1.1        Features

- Supplies power for up to four ISDN or S(H)DSL transmission lines on Central Office and DSLAM Linecards
- ETSI TS 102 080 compatible
- TS 101 524 and ITU-T G.991.2 Annex B compatible
- Feediing of multiple S/T interfaces in IADs and PBXs.
- Line Feed Supply Voltage up to 130 V

**P-MQFP-44**

- Separate Current Monitoring and Limiting for each line
- Current Limiting Level can be programmed by an external resistor
- Overcurrent indication threshold can be programmed with external resistors independently from the current limitation.
- The overcurrent indication setup delay can be programmed by external capacitors, separately for each line
- Intelligent Chip Temperature Control
- Automatically switching off lines in current limitation when expecting over temperature problems
- Automatically switching off all four lines in case of real overtemperature
- Integrated Relay Drivers and Relay Driver Controlling for eight relays
- Optimized for working in conjunction with PEB/F 24901 (DFE-T) and PEB/F 24911 (DFE-Q).
- Small P-MQFP-44 Package
- Reliable 170 V Smart Power Technology
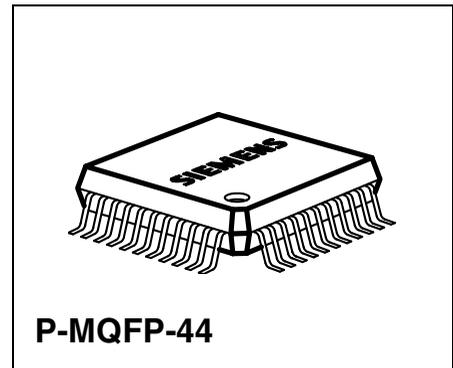
| Type | Package |
|------|---------|
| PEF 2426 | P-MQFP-44 |

## 1.2 Logic Symbol
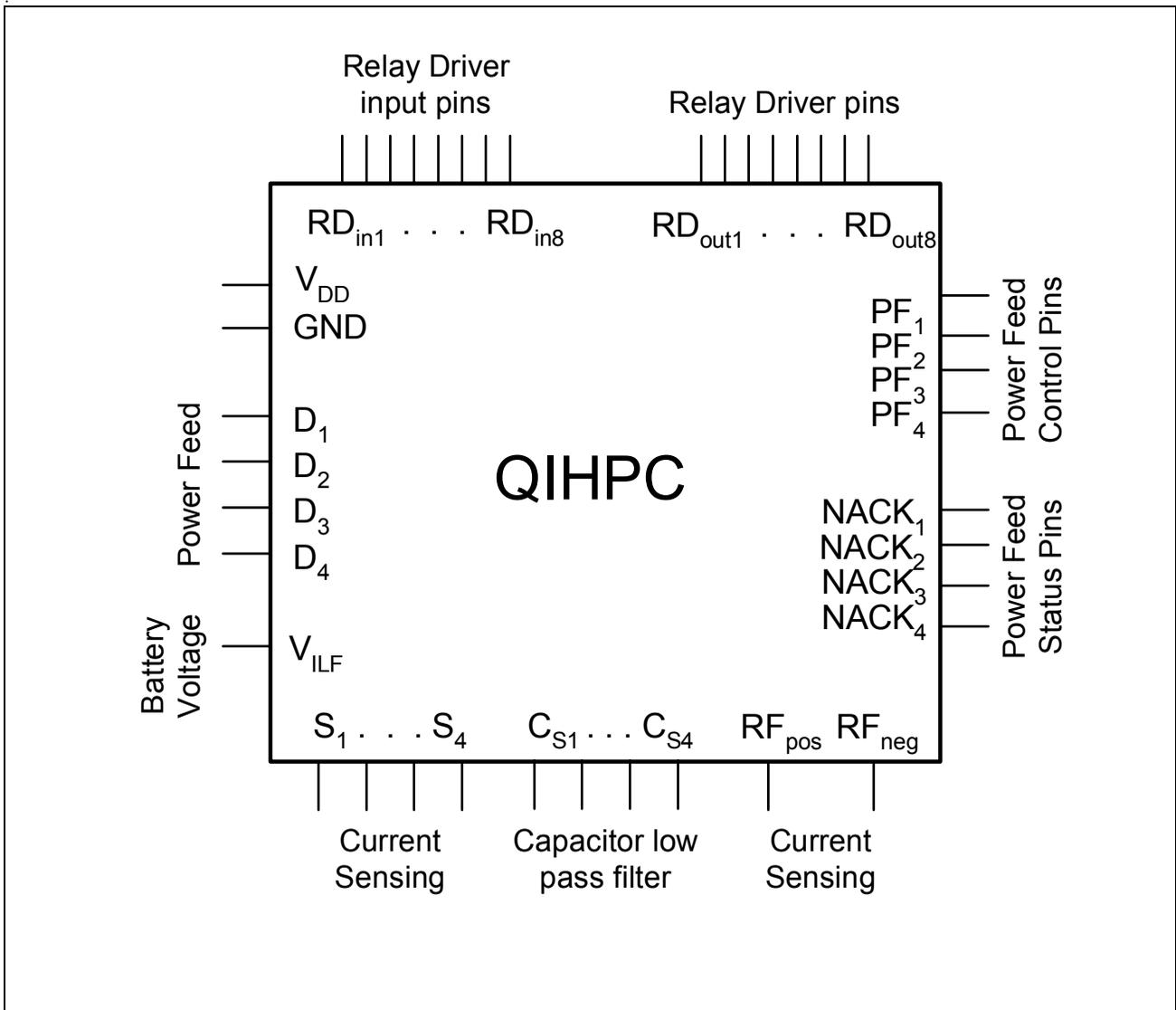


**Figure 1    Logic Symbol**

## 1.3 Typical Applications

The QIHPC is an integrated power controller especially designed for feeding two-wire ISDN/S(H)DSL-transmission lines. Four U interface lines can be powered by one QIHPC.
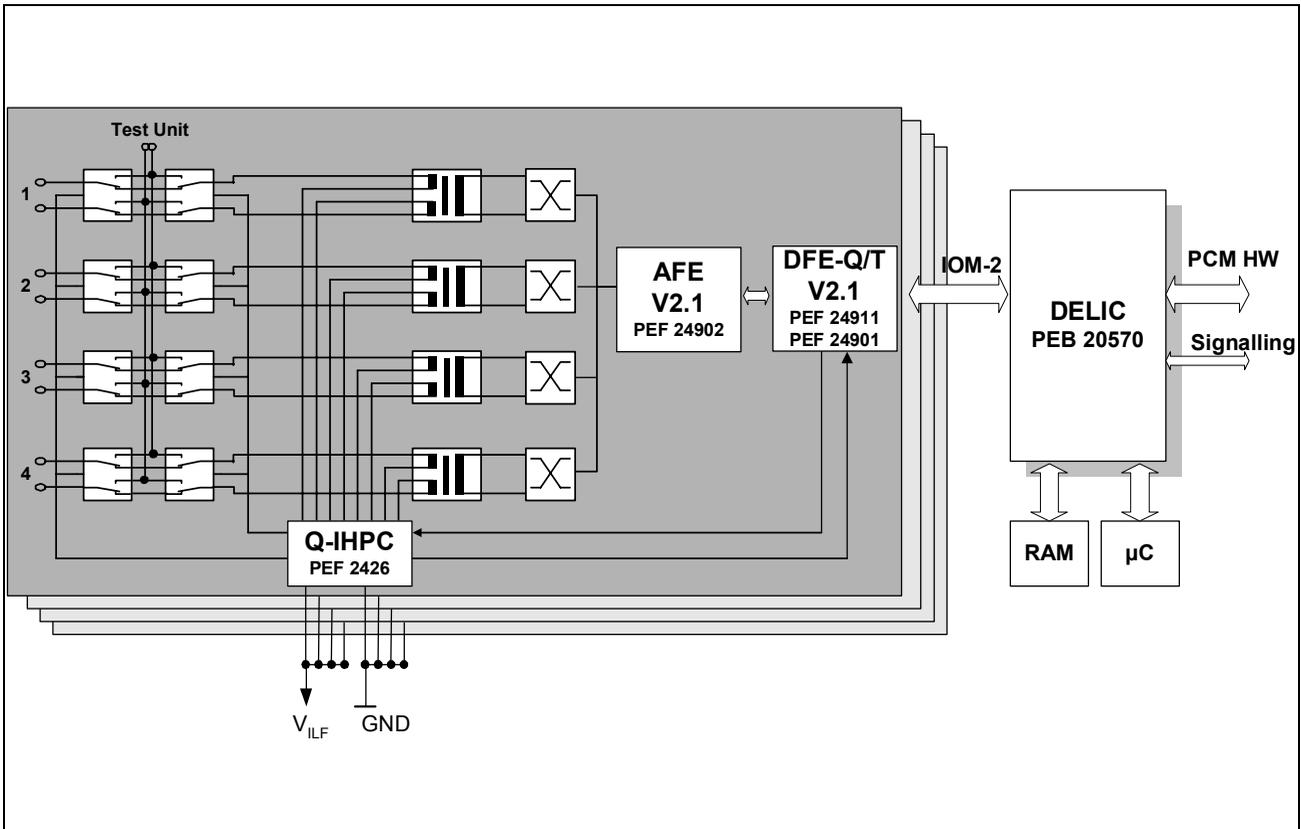


**Figure 2    16-Line Card Application with DELIC, DFE-Q/T and AFE**
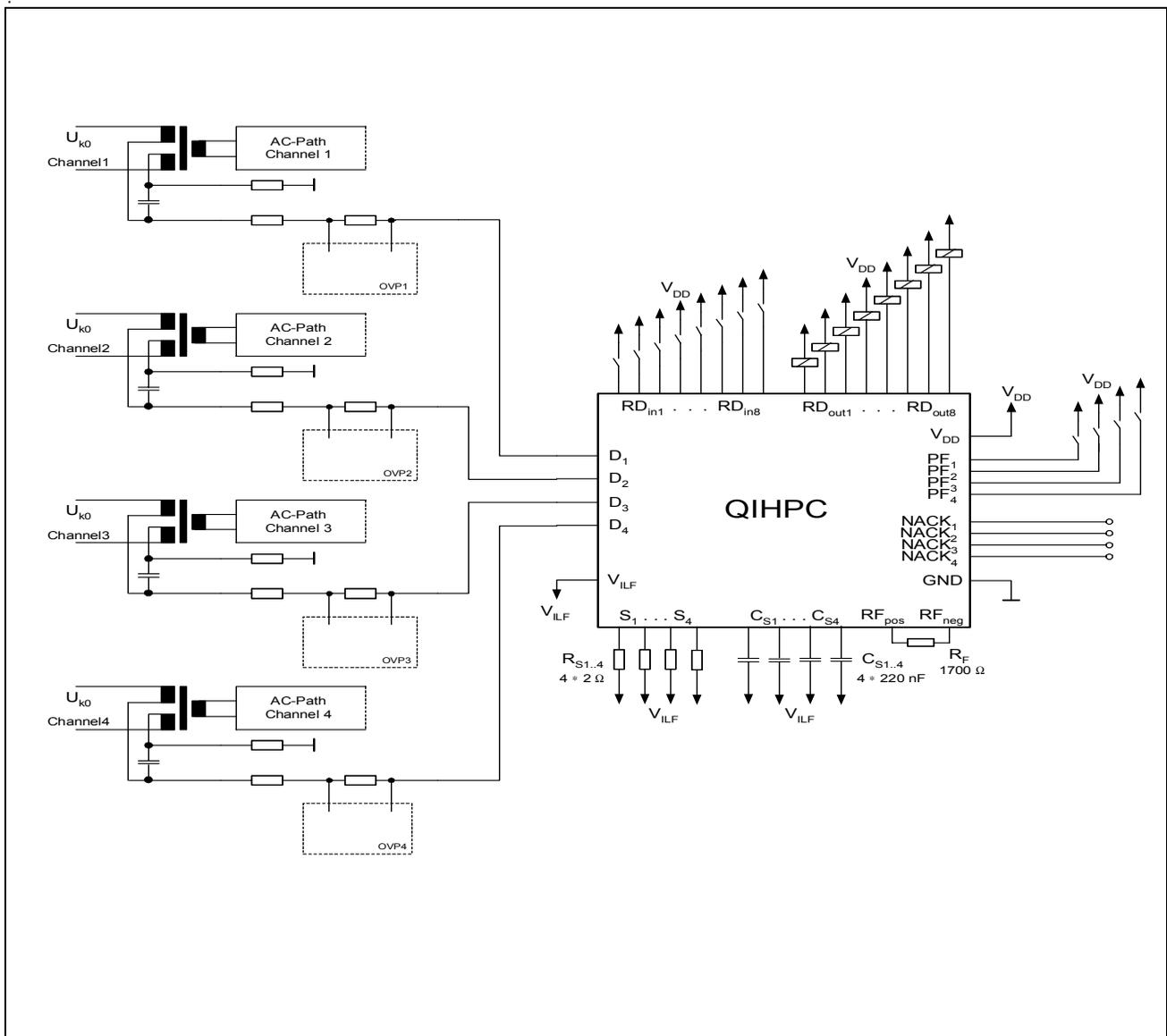
**Figure 3      System integration**

**Figure 3** gives general overview of the system integration of the QIHPC.

Due to the integrated "pull-down current-sinks" on the input pins $PF_{1..4}$ and $RD_{in1..8}$ only connections to $V_{DD}$ are necessary to switch on power feeding to the lines or to switch on the relay drivers. When power feeding to a line is switched on, and this line is in a normal feeding condition (current less than the current limiting level), then the QIHPC shows a resistive connection from $D_x$ to $S_x$. $D_x$ and $S_x$ are the drain and source of the integrated DMOS-transistor of channel x. The resistance value (DMOS-$R_{on}$) is typically 1.4 $\Omega$ with a total tolerance of about +/- 0.35 $\Omega$.

## 1.4 S/T-Feeding

Due to its functional similarity to the PEB 2025 IEPC, the QIHPC can be used as a replacement for  the PEB 2025 in applications such as current feeding at multiple S interfaces:

.

**Table 1      Comparing the Power Feeeding IC's: IEPC vs. QIHPC**

|  | **PEB 2025 IEPC** | **PEF 2426 QIHPC** |
|---|---|---|
| Vbat Range | -60V to -12V | -130V to - 30V |
| Channels | 4 | 4 |
| Vbat supply current (excl. Line feeding currents) | 0.2mA max. | 1mA max |
| Dig. supply voltage | 4.75V to 5.25V | +3V to +6V |
| Dig. supply current (@ 5V) | 5mA typ.; 10mA max. | 0.7mA typ.; 1.5mA max. |
| Feeding current control | System controlled turn-on; automatic turn-off | Automatic current limitation; system controlled turn-off |
| Specified feeding current control settings | 75mA; 152mA (approx. $\pm$25%) | 67 up to 150mA ($\pm$12%) possible |
| Turn-on resistance | 7Ohm typ., 9 Ohm max. | 1.4 Ohm typ., 2 Ohm max. |
| System interface | Parallel µP i/f  (9 pins) | 8 I/O pins |
| Relay drivers integrated | None | 8 |
| Operating temperature range | 0 to 70 °C | -40 to +85°C (PEF) |
| Package | P-LCC-28; P-DIP-22 | P-MQFP-44 |

# 2 Pin Descriptions

## 2.1 Pin Configuration
(top view)
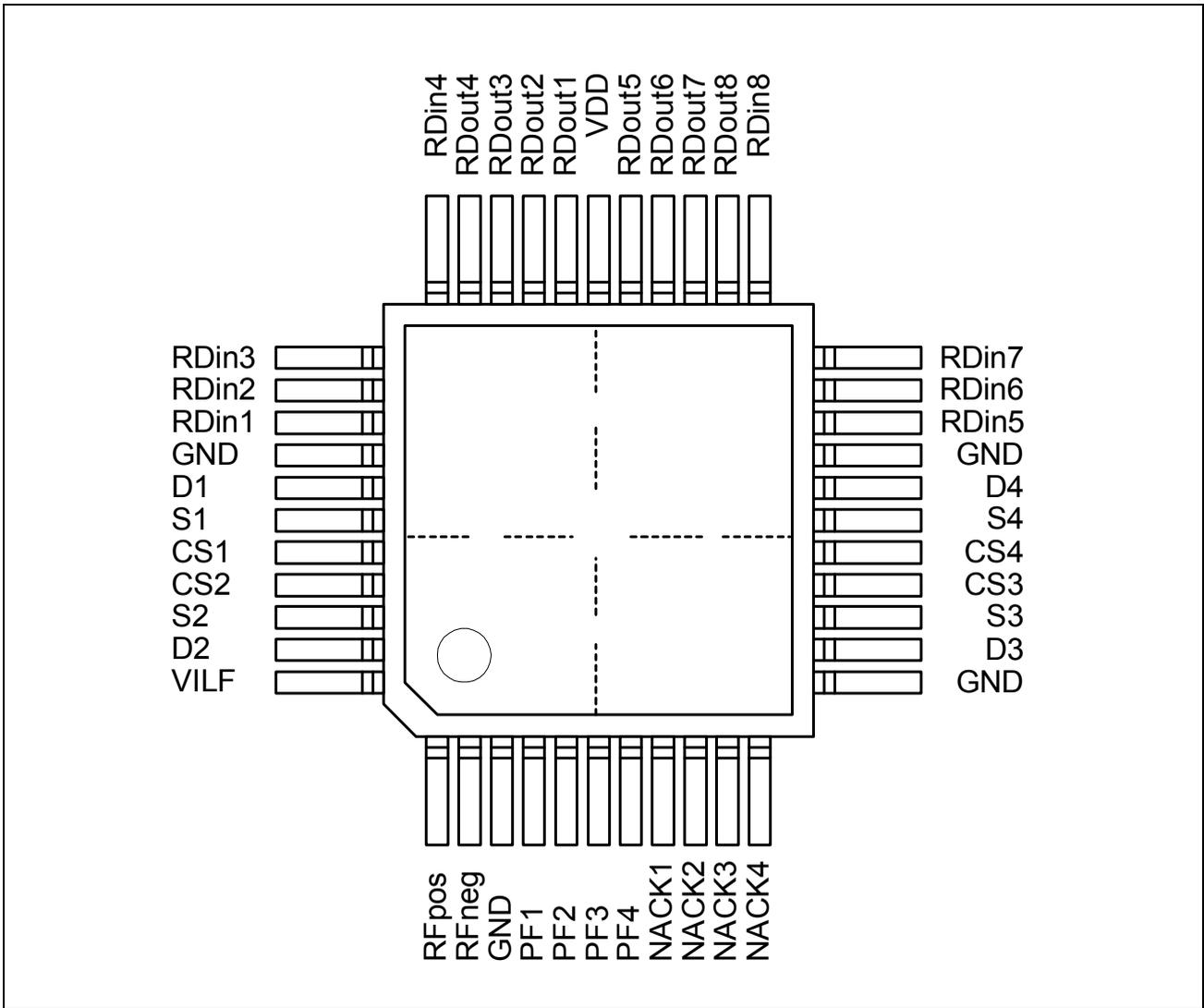


**Figure 4      Pin Configuration**

## 2.2 Pin Definitions and Functions

.

**Table 2 Pin Definitions and Functions**

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 28 | $V_{DD}$ | Supply | **Positive Supply Voltage, referred to GND.** Operating Voltage Range from 3.0 V to 6.0 V. |
| 3 12 19 37 | GND | Supply | Ground |
| 44 | $V_{ILF}$ | Supply | **Line Feed Voltage, referred to GND.** Operating Voltage Range from -130 V to -30 V. |
| 38 43 13 18 | $D_1$ $D_2$ $D_3$ $D_4$ | O | **Drain Connections of the Output Transistors of Channels 1..4.** These pins have to be connected (via external resistors) to ISDN/S(H)DSL lines a (ring) of channels 1..4. |
| 1 2 | $RF_{pos}$ $RF_{neg}$ | O | **Current limitation of Channels 1..4.** These pins have to be connected to an external resistor $R_F$. $R_F$ and $R_{S1..4}$ are defining the output current limit for all four lines. |
| 39 42 14 17 | $S_1$ $S_2$ $S_3$ $S_4$ | O | **Overcurrent indication threshold.** These pins have to be connected via external resistors $R_{S1..4}$ to $V_{ILF}$ defining the overcurrent indication threshold of each line individually. |
| 40 41 15 16 | $C_{s1}$ $C_{s2}$ $C_{s3}$ $C_{s4}$ | O | **External capacitors defining $t_{OC}$-delays of Channels 1..4.** These pins have to be connected via external capacitors to $V_{ILF}$ defining the overcurrent indication delay. |
| 4 5 6 7 | $PF_1$ $PF_2$ $PF_3$ $PF_4$ | PD | **Power Feed Signal of Channels 1..4.** Logic high on $PF_{1..4}$ switches on the power feeding to the line of channel 1..4. |

**Table 2** **Pin Definitions and Functions** (Continued)

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---------|--------|---------------------|----------|
| 8<br>9<br>10<br>11 | $NACK_1$<br>$NACK_2$<br>$NACK_3$<br>$NACK_4$ | O | **Not Acknowledged Signal of Channels 1..4.**<br>Logic low on $NACK_{1..4}$ signals that either the ISDN/S(H)DSL line of channel 1..4 is powered and in a normal power on condition or that power feed is not requested.. |
| 36<br>35<br>34<br>33<br>20<br>21<br>22<br>23 | $RD_{in1}$<br>$RD_{in2}$<br>$RD_{in3}$<br>$RD_{in4}$<br>$RD_{in5}$<br>$RD_{in6}$<br>$RD_{in7}$<br>$RD_{in8}$ | PD | **Switch-On-Signal of Relay-Channels 1..8.**<br>Logic high on $R_{in1..8}$ switches on the relay driver npn-transistor of channel 1..8. |
| 29<br>30<br>31<br>32<br>27<br>26<br>25<br>24 | $RD_{out1}$<br>$RD_{out2}$<br>$RD_{out3}$<br>$RD_{out4}$<br>$RD_{out5}$<br>$RD_{out6}$<br>$RD_{out7}$<br>$RD_{out8}$ | O | **Open Collector Output of Relay-Channels 1..8.**<br>When the relay driver npn-transistor of channel 1..8 is switched on, than this pin sinks a current of up to 40 mA.<br>An integrated zener diode guards the QIHPC against inductive voltage peaks from the relay coil. |

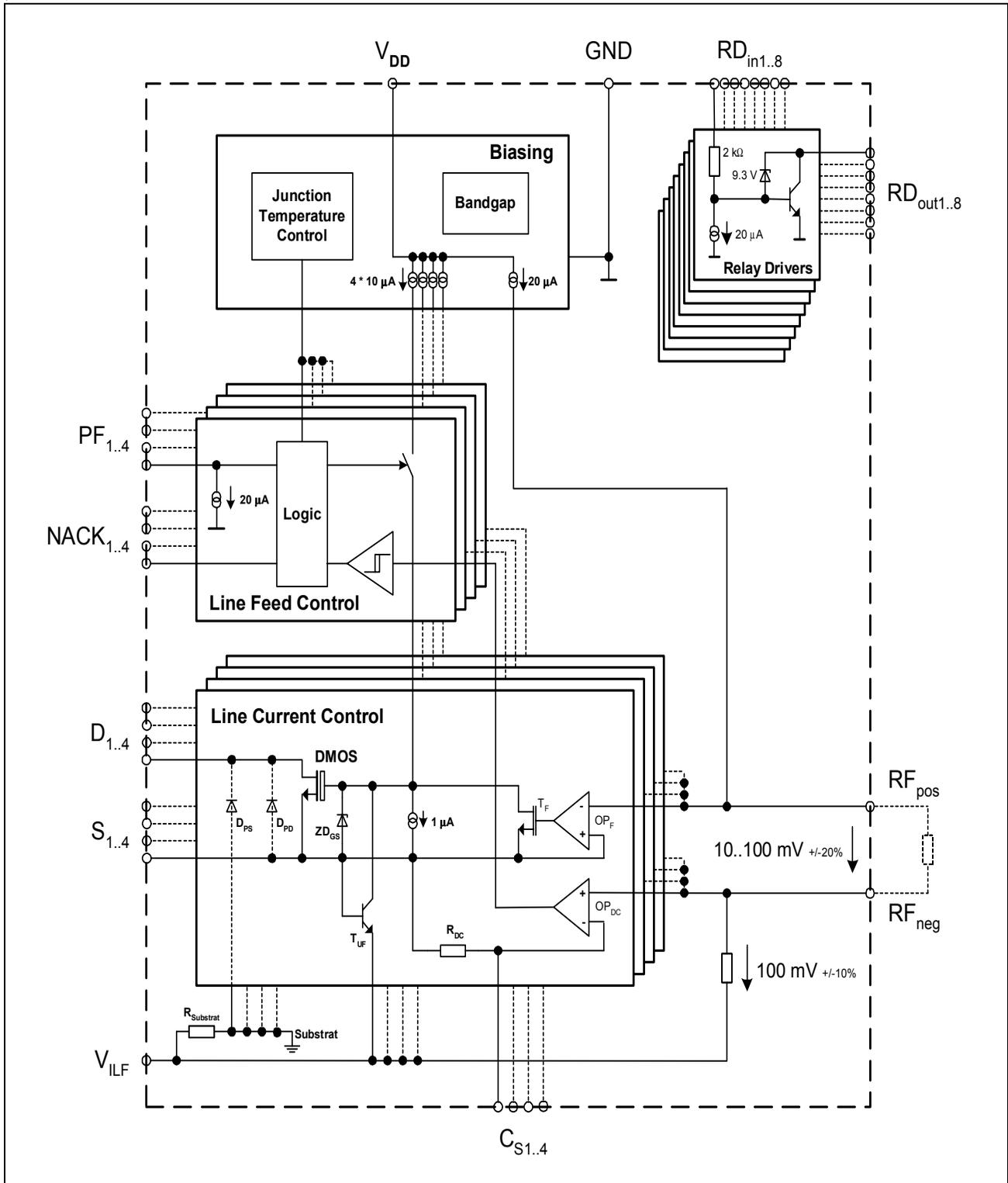# 3 Functional Description

## 3.1 Functional Block Diagram



**Figure 5    Functional Block Diagram**

In the Functional Block Diagram, **Figure 5**, we can see four different types of circuit blocks: one biasing circuit, four line feed control circuits, four line current control circuits and eight relay driver circuits.

## 3.2 Biasing Circuit

The bandgap circuit generates a constant voltage with respect to GND. This reference voltage is converted into a current of about 20 $\mu$A which is necessary for level shifting. This current is converted back into 100 mV and 10..100 mV (depending on the value of the external resistor $R_F$) reference voltages with respect to $V_{ILF}$. These reference voltages and the external resistors connected between pins $S_{1..4}$ and $V_{ILF}$ defines the line current limit and the overcurrent indication threshold.

Currents of about 10 $\mu$A are used for level shifting the power feed information. In the biasing block also all other biasing currents used on the chip are generated.

Intelligent junction temperature control in coordination with line current limiting protects the QIHPC against overloads. Also a fault condition on one line shall under no circumstance disturb a connection on another line. Therefore a junction temperature control circuit is necessary.

The junction temperature of the QIHPC will be monitored by an integrated thermal detector with three threshold levels, as defined in **Table 3**

**Table 3        Thermal Detector Threshold Levels**

| Symbol | Parameter Description | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{j1}$ | 130 °C Thermal Detector threshold | guaranteed by design | 120 | 130 | 140 | °C |
| $T_{h1}$ | 130 °C Thermal Detector hysteresis | guaranteed by design | | 10 | | °C |
| $T_{j2}$ | 170 °C Thermal Detector threshold | guaranteed by design | 160 | 170 | 180 | °C |
| $T_{h2}$ | 170 °C Thermal Detector hysteresis | guaranteed by design | | 10 | | °C |
| $T_{j3}$ | 190 °C Thermal Detector threshold | guaranteed by design | 180 | 190 | 200 | °C |
| $T_{h3}$ | 190 °C Thermal Detector hysteresis | guaranteed by design | | 10 | | °C |

Power on requests will only be executed if the junction temperature is below $T_{j1}$ (typical 130 °C) and if no other line is in overcurrent condition. If the device junction temperature reaches the second threshold $T_{j2}$ (typical 170 °C), then all the line drivers in the current-

overload condition will be switched off by the QIHPC. If the device junction temperature then still continues to increase to $T_{j3}$ (typical 190 °C), all the line drivers will be turned off by the QIHPC.

The line(s) in current overload will be switched off sufficiently fast once the second threshold $T_{j2}$ is reached, i.e. before the $T_{j3}$ threshold is reached. This guarantees a disturbance free operation on lines not affected by a fault condition. Once a line had been switched off the relevant PF-pin has to be set to low and subsequently to high, for attempting to power this line again.

The internal protection mechanisms (current limiting and junction temperature control) already provide full protection of the $D_{1..4}$ outputs against short circuits to a voltage between GND and $V_{ILF}$.

Note: The thermal protection mechanism of the QIHPC is a protection against instant damages due to overload at the outputs. Continuous high temperatures during operation, however, will reduce the life time of the QIHPC. Measures have to be taken to switch off the QIHPC in case of a short-circuit. E.g. if pin $NACK_x$ indicates an current overload condition, the QIHPC should be deactivated after few seconds using pin $PF_x$.

## 3.3 Line Feed Control Circuit

The QIHPC can supply the power for up to four transmission lines simultaneously. The exchange of activation commands and status information with the QIHPC will occur via a parallel interface, consisting of one input (PF) and one output (NACK) per line. The power switch can be controlled (PF) for each line individually. The status information (NACK) can be monitored for each line separately.

Integrated "pull-down current-sinks" are connected to the input pins $PF_{1..4}$. If one of these pins is not connected externally, the logic level at this pin is "0".

Logic level "0" means that the voltage on this pin is about 0 and logic level "1" means that the voltage level on this pin is about $V_{DD}$.

A diagnostic of possible fault conditions is available on the status information pins (NACK) for each line separately.

The NACK pin is set to "1" when PF="1" and:
- Current on the line reaches the overcurrent indication threshold for longer than $t_{OC}$.
- Over temperature ($T_j > T_{j3}$) is detected.
- Power feed setting is not acknowledged by the QIHPC.

See also **Table 4**.

**Table 4        Function Table for Controlling One Line**

| PF | current (other channels) | current (this channel) | $T_j$ | NACK | Comment |
|---|---|---|---|---|---|
| 0 | don't care | don't care | don't care | 0 | line feeding not requested |
| $0 \rightarrow 1$ | at least one above indication threshold | don't care | don't care | 1 | power feeding not acknowledged and the line is not powered as long as an other line is in overcurrent condition |
| $0 \rightarrow 1$ | don't care | don't care | $> T_{j1}$ | 1 | power feeding not acknowledged and the line is not powered, as long as the junction temperature is to high |
| 1 | don't care | above indication threshold | $< T_{j2}$ | 1 | feeding: this line is in over current condition |
| 1 | don't care | below indication threshold | $< T_{j3}$ | 0 | normal line feeding |
| 1 | don't care | don't care | $> T_{j3}$ | 1 | overtemperature condition, feeding is switched off |

In case of simultaneous power up requests ($PF_{1..4}$) the QIHPC take care of a proper start-up sequencing. The four channels have different priority. First priority for channel 1, second priority for channel 2 etc.

By simultaneous power up requests on more than one channel, the channel with the highest priority will be powered first, and will normally start with current limiting condition. When this channel is powered up and the drawn current drops below the current indication level, the next channel will be powered. And so on (see also figure 6 and table 3).

## 3.4        Line Current Control Circuit

Two different current limiting circuits are integrated to control the DMOS power switch. An ultrafast and a fast current limiting circuit. See also **Figure 5**.

The ultrafast current limiting circuit consists of a bipolar npn-transistor $T_{UF}$. Note that bipolar npn-transistors are the fastest devices from the used technology. If the voltage

between $S_{1..4}$ and $V_{ILF}$ exceeds about 0.7 V the DMOS is switched off as fast as possible. 0.7 V divided by $R_{S1..4} = 2 \, \Omega$ results in an ultrafast current limiting level of about 350 mA. This level has a strong temperature dependence (-40 °C junction temperature gives about 420 mA and +120 °C results in about 300 mA). The ultrafast current limiting circuit protects the QIHPC against short circuit on the line side with a resulting current rising as fast as 2 A/100 nsec.

The fast current limiting circuit keeps the voltage between $S_{1..4}$ and $V_{ILF}$ below a programmable voltage level. This results in a current limitation.

Zener diode $ZD_{GS}$ protects the DMOS-gate.

Diodes $D_{PD}$ and $D_{PS}$ are the parasitic drain-bulk-diode and drain-substrate-diode of the DMOS transistor (junction isolated technology). The diodes do not provide overvoltage protection, negative surges would pass through to $S_{1..4}$ and $V_{ILF}$ affecting the battery voltage. Extra overvoltage protection circuitry is necessary to conduct voltage surges form the line to ground, and to prevent that any current can flow into Diodes $D_{PD}$ and $D_{PS}$.

Typical value of DMOS-on-resistance including internal wiring-resistance to the pins $D_{1..4}$ and $S_{1..4}$ is 1.4 $\Omega$.

To identify overcurrent, the voltage between $S_{1..4}$ and $V_{ILF}$ is compared to 100 mV. If the voltage exceeds this level, this is indicated to the line current control circuits. A resistor and the external capacitor $C_S$ define a lowpass filter (time delay) to suppress the changes on NACK due to short overcurrent surges. This enables to filter the effects of longitudinal AC current.

An external capacitor with a value of about 220 nF results in a delay time ($t_{OC}$) of about 25 msec.

## 3.5 Relays Driver Circuit

The output transistor is a bipolar npn. The maximal collector current should not exceed 40 mA. When switching off an inductive load, zener diode and npn clamps the voltage level on pin $RD_{out1..8}$ at about 10 V. The 2 k$\Omega$ resistor limits the input current on pin $RD_{in1..8}$ and additionally the npn collector current.

If a pin $RD_{in1..8}$ is not connected, the integrated "pull-down current-sink" holds the respective relay driver in switched-off condition.

# 4 Application Hints

## 4.1 Resistor $R_{S1..4}$

The value of this resistor defines the overcurrent indication level. Note, that the value of this resistor must be considered for line symmetry. The typical overcurrent indication level $I_{ind}$ can be programmed by using the following formula.

.

$$I_{ind} = \frac{100\,mV}{R_{S1...4}}$$

If for any reason one or more ports of the QIHPC shall remain unused, the respective resistor $R_{Sx}$ has to provided anyway. Pin $D_x$, however, can be left unconnected.

## 4.2 Resistor $R_F$

The values of resistors $R_F$ and $R_{S1..4}$ define the current limiting level. The typical overcurrent limitation level $I_{lim}$ can be programmed by using the following formula.

.

$$I_{lim} = \frac{100\,mV + R_F \cdot 20\,\mu A}{R_{S1...4}}$$

## 4.3 Capacitor $C_{S1..4}$

The value of this capacitor define the resulting delay time $t_{OC}$ for the overcurrent indication. For typical values of $t_{OC}$ as a function of $C_{S1..4}$ see **Figure 6**.
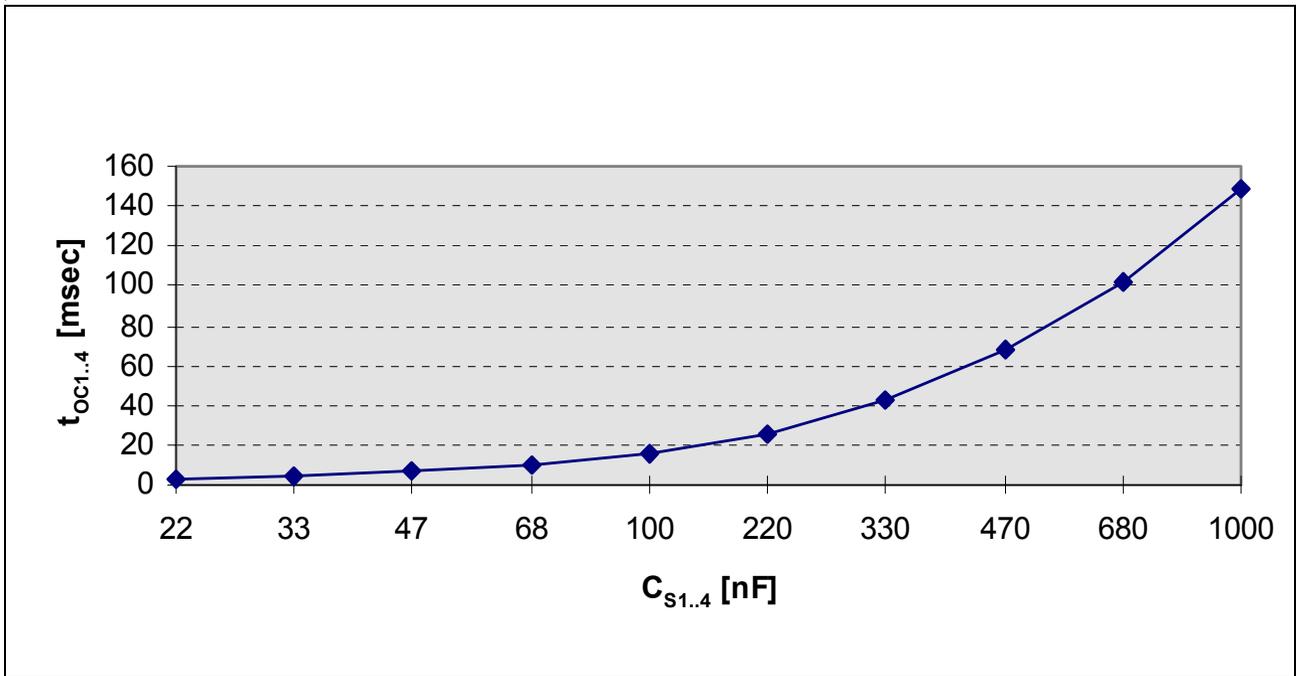
**Figure 6**   Delay time $t_{OC}$ as a function of the value of $C_{S1..4}$ (typical values)

## 4.4 Protection Circuitry
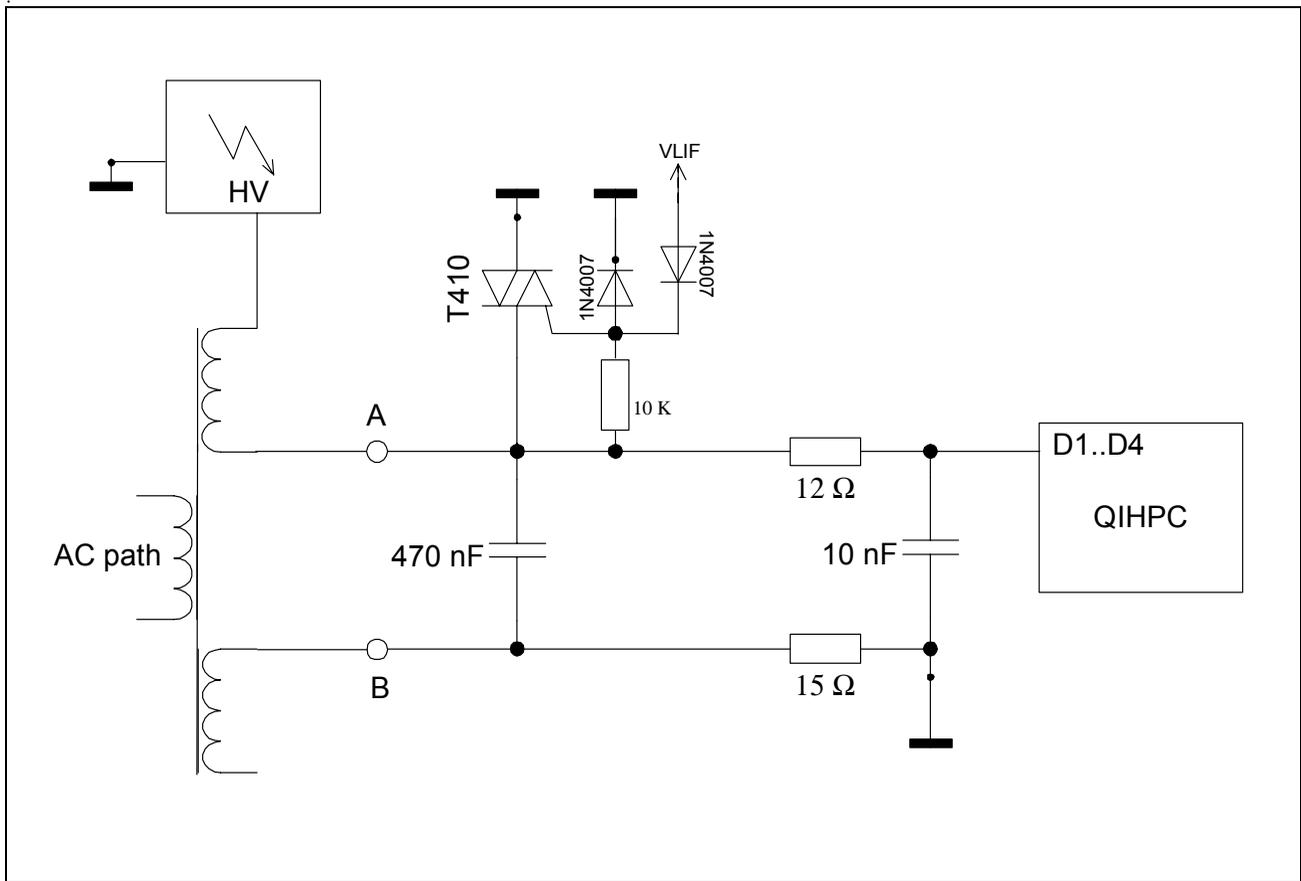


**Figure 7    Proposal for a Protection Circuitry**

An external circuitry is needed to protect the QIHPC against damages due to high voltages from the line. High voltages can be caused by lightning surges or foreign voltage contact.

The protection element in this scheme is a Triac (T410). With positive going surges, the Triac will fire through a gate current flowing via diode 1N4107 to ground. With negative going surges, the gate current is supplied by VILF via the second 1N4007 diode.This circuit is capable to protect the QIHPC against damage with surges up to +/- 3kV (1.2/50µs and 10/700 µs pulse shape).

Shorting of voltage surges to GND is sensed by the QIHPC in the same way as a short-circuit at the line. It will react according to the programmed overcurrent indication and overcurrent limitation.

# 5 Operational Description

The QIHPC is compliant to the ETSI TS 102 080 "Dynamic power feeding requirements" using the LT power test load (see **Figure 8**). There is no requirement for the order of powering up the lines, or for dependencies of controlling between the lines.
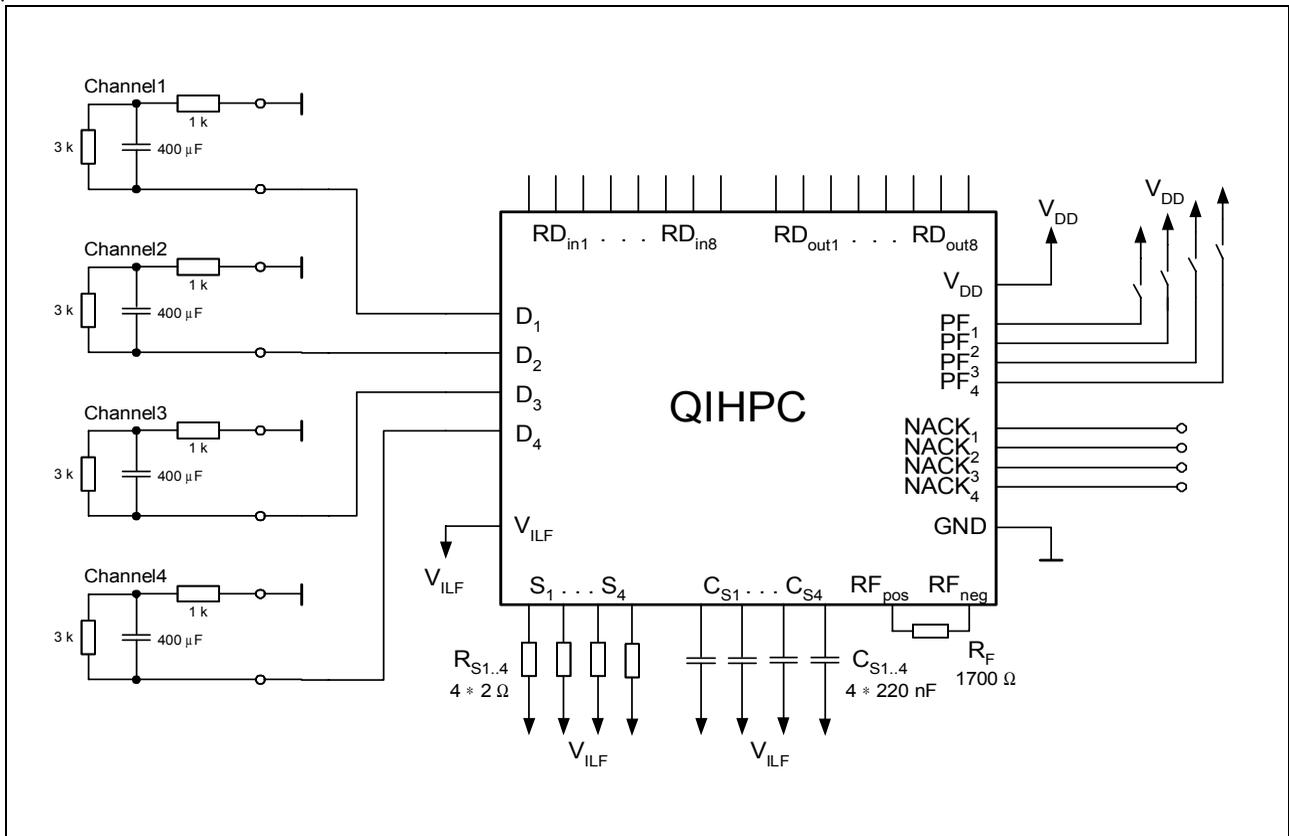


**Figure 8      Circuit with "LT Power Source Test Loads"**

With the LT power source test load from TS 102 080 the QIHPC can power up four U line interfaces within about 2 seconds "quasi simultaneous". The input sequence and expected output sequence with power dissipation diagram is shown in **Figure 9**. The power dissipation in the chip is quite small.

A fault condition (short circuit) on one line does not affect the power up of the other lines.

**Example:**

Assumed a short circuit on line 3. A simultaneous power up request is applied to the QIHPC. The power up of lines 1 and 2 will proceed as expected. When powering up line 3, the chip temperature control ($T_{j2}$) will switch off this line. Lines 1 and 2 are still powered and remain in normal power on condition. When the junction temperature is decreased to $T_{j1}$ the QIHPC will try to power up line 4. If there is no fault condition on line 4 the lines 1, 2 and 4 are finally in a normal power on condition. Line 3 is still in power off. To to repeat the trial to powering up line 3, the input signal $PF_3$ must set to "0" and "1" again.
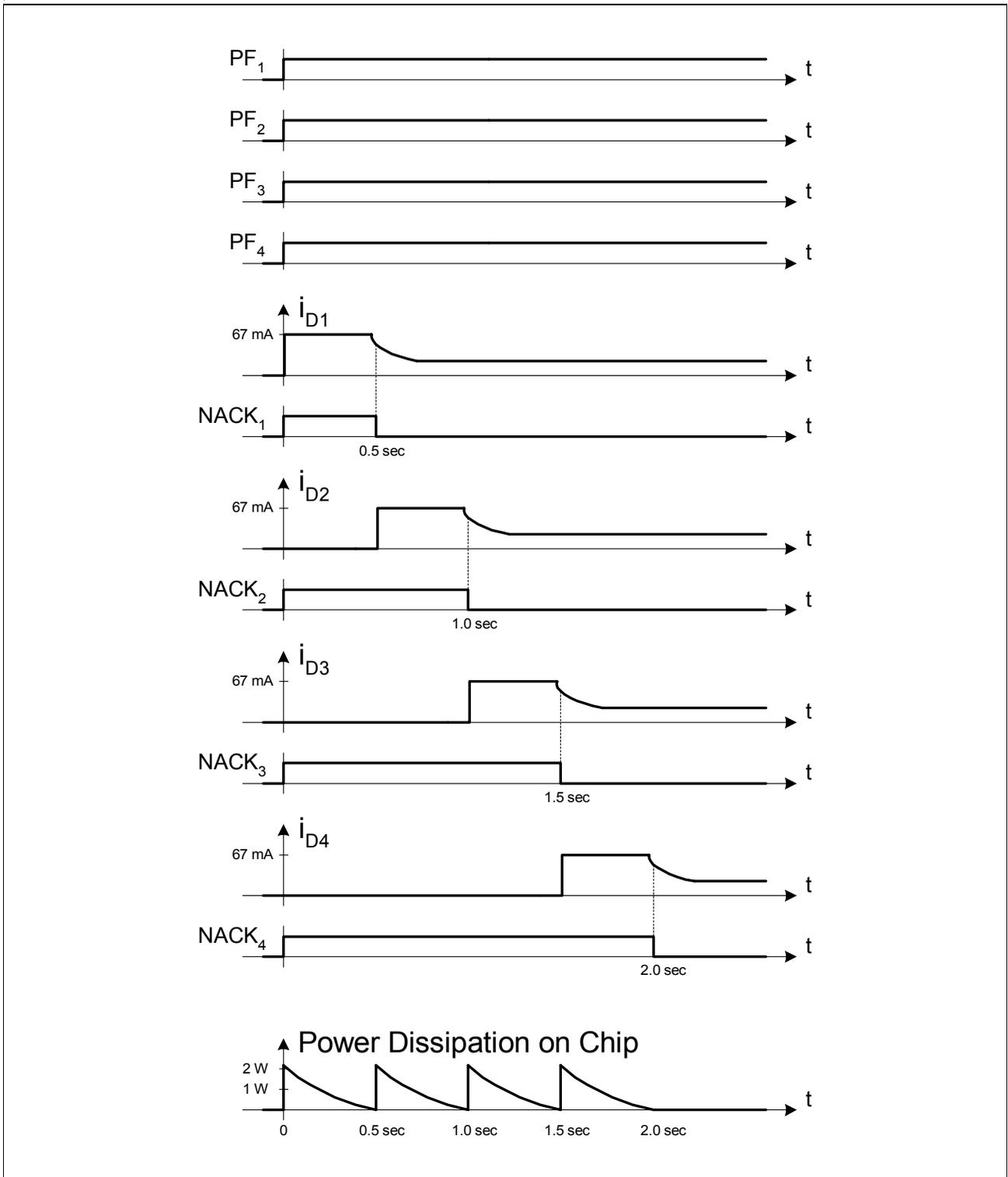
**Figure 9      Simultaneous Power Up Sequence**

# 6 Electrical Characteristics

## 6.1 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | Unit |
|---|---|---|---|
| Operating ambient temperature range: | $T_A$ | – 40 to 85 | °C |
| Storage temperature range | $T_{stg}$ | – 65 to 125 | °C |
| Voltage on pin $V_{DD}$ with respect to ground | $V_{DDmax}$ | – 0.4 to + 8 | V |
| Voltage on pin $V_{ILF}$ with respect to ground | $V_{ILFmax}$ | – 140 to $V_{DD}$ + 0.4 | V |
| Voltages on pins $D_{1..4}$ with respect to $V_{ILF}$ | $V_{D1..4max}$ | – 0.4 to + 150 | V |
| Voltages on pins $D_{1..4}$ with respect to $V_{ILF}$ with series resistor $R_S$ = 5 Ω /figure 15 | $V_{D1..4maxRs}$ | – 3 to + 150 | V |
| Pulse voltages on pins $D_{1..4}$ with respect to $V_{ILF}$ with series resistor $R_S$ = 5 Ω /figure 15: t = 200 msec / f = 50 Hz or t = 50 msec / f = 16.7 Hz | $V_{D1..4pulse}$ | – 3 to + 150 | $V_P$ |
| Impulse voltages on pins $D_{1..4}$ with respect to $V_{ILF}$ with series resistor $R_S$ = 5 Ω /figure 15: $T_{dur}$ = 20 μsec / $T_{rise}$ = 25 nsec / non repetitive | $V_{D1..4impulse}$ | – 5 to + 160 | $V_P$ |
| Voltages on pins $S_{1..4}$ with respect to $V_{ILF}$ | $V_{S1..4max}$ | – 0.4 to + 8 | V |
| Voltages on pins $D_{1..4}$ with respect to voltages on pins $S_{1..4}$ | $V_{DS1..4max}$ | – 0.4 to + 140 | V |
| Voltages on pins $C_{S1..4}$ with respect to $V_{ILF}$ | $V_{CS1..4max}$ | – 0.4 to + 8 | V |
| Voltages on pins $PF_{1..4}$ with respect to ground | $V_{PF1..4max}$ | – 0.4 to $V_{DD}$ + 0.4 | V |
| Voltages on pins $NACK_{1..4}$ with respect to ground | $V_{NA1..4max}$ | – 0.4 to $V_{DD}$ + 0.4 | V |
| Voltages on pins $R_{in1..4}$ with respect to ground | $V_{Ri1..4max}$ | – 0.4 to $V_{DD}$ + 0.4 | V |
| Voltages on pins $R_{out1..4}$ with respect to ground | $V_{Ro1..4max}$ | – 0.4 to $V_{DD}$ + 0.4 | V |
| ESD-voltage, all pins (Human body model) | $V_{ESD-HBM}$ | - 1 to + 1 | kV |

**Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**
**Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

## 6.2 Operating Range

| Parameter | Symbol | Limit Values | Unit |
|---|---|---|---|
| V$_{DD}$ supply voltage | $V_{DD}$ | + 3.0 to + 6.0 | V |
| V$_{ILF}$ supply voltage | $V_{ILF}$ | - 130 to - 30 | V |

Note: In the operating range the functions given in the circuit description are fulfilled.

## 6.3 Static Thermal Resistance

| Parameter | Symbol | Limit Values | Unit |
|---|---|---|---|
| Junction to ambient | $R_{th, jA}$ | < 62.9 | K/W |
| Junction to case | $R_{th, jC}$ | < 14.6 | K/W |

## 6.4 AC/DC-Characteristics

**General Test Conditions (if not indicated otherwise):**

$R_{S1..4} = $ 2 Ω   $\pm$ 0.1 %        $C_{S1..4} =$ 220 nF   $\pm$ 1 %(63 V)
$R_F$   =   1700 Ω   $\pm$ 0.1 %

**Supply voltages for typical characteristics:**

$V_{DD}$   =   5 V   $\pm$ 1 %        $V_{ILF}$   =−100 V   $\pm$ 1 %

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A$ = 25 °C and the given supply voltage

**Table 5     DC Characteristics**

| No. | Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Fig. |
|---|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | | |
| **Supply Currents** | | | | | | | | |
| 1 | $V_{DD}$ current | $I_{DD}$ | | 0.7 | 1.5 | mA | | 10 |
| 2 | $V_{ILF}$ current | $I_{ILF}$ | | 0.4 | 1 | mA | excluding line currents | 10 |
| **Line Currents, Delay Time $t_{OC}$ and DMOS-$R_{ON}$ resistance** | | | | | | | | |
| 3 | Overcurrent Indication Level | $I_{maxOC1..4}$ | 45 | 50 | 55 | mA | $PF_{1..4}$ = "1" | 11 |
| 4 | Current Limiting Level | $I_{maxL1..4}$ | 59 | 67 | 75.5 | mA | $PF_{1..4}$ = "1" | 11 |
| 5 | Line Current in "on"-condition | $I_{maxON1..4}$ | | | 168 | mA | $PF_{1..4}$ = "1" if $I_{maxL1..4} > I_{maxON1..4}$ | 11 |
| 6 | Line Current in "off"-condition | $I_{maxOFF1..4}$ | | 0 | 10 | µA | $PF_{1..4}$ = "0" | 11 |
| 7 | Delay Time $t_{OC}$ | $t_{OC1..4}$ | 10 | 25 | 40 | msec | $PF_{1..4}$ = "1", $I_{Line}$ >= 55 mA | 11 |
| 8 | DMOS-$R_{ON}$ resistance | $R_{ON1..4}$ | 0.8 | 1.4 | 2.0 | Ω | $PF_{1..4}$ = "1", $I_{Line}$ = 25 mA | 12 |
| **$PF_{1..4}$, Logic Input Levels** | | | | | | | | |
| 9 | "1" - Input Voltage | $V_{HPF1..4}$ | 2 | | | V | | 13 |
| 10 | "0" - Input Voltage | $V_{LPF1..4}$ | | | 0.8 | V | | 13 |
| 11 | pull down Input Current | $I_{PF1..4}$ | 10 | 20 | 30 | µA | 0.8 V < $V_{PF1..4}$ < $V_{DD}$ | 13 |
| **$NACK_{1..4}$, Logic Output Levels** | | | | | | | | |
| 12 | "1" - Output Voltage | $V_{HNACK1..4}$ | $V_{DD}$ − 0.4 | | | V | $I_{Source1..4}$ = 100 µA | 13 |
| 13 | "0" - Output Voltage | $V_{LNACK1..4}$ | | | 0.4 | V | $I_{Sink1..4}$ = 100 µA | 13 |

**Table 5     DC Characteristics** (Continued)

| No. | Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Fig. |
|-----|-----------|--------|------|------|------|------|----------------|-----------|
| | | | min. | typ. | max. | | | |
| **RD$_{in1..8}$, Relay Driver Inputs** | | | | | | | | |
| 14 | "ON" - Input Voltage | $V_{on,RDin1..8}$ | 2.0 | | $V_{DD}$ | V | | 14 |
| 15 | "OFF" - Input Voltage | $V_{off,RDin1..8}$ | | | 0.4 | V | | 14 |
| 16 | pull down Input Current | $I_{pd,RDin1..8}$ | | 20 | 30 | μA | $0 < V_{RDin1..8} < 0.4$ V | 14 |
| **RD$_{out1..8}$, Relay Driver Outputs** | | | | | | | | |
| 17 | Saturation Voltage | $V_{sat1,RD1..8}$ | | 0.25 | 0.4 | V | $V_{RDin1..8} = 2,4$ V, $I_{RDout1..8} = 33$ mA | 14 |
| 18 | Saturation Voltage | $V_{sat2,RD1..8}$ | 0.2 | 0.4 | 0,5 | V | $V_{RDin1..8} = 2,4$ V, $I_{RDout1..8} = 40$ mA | 14 |
| 19 | Current in "off"- condition | $I_{off,RD1..8}$ | | 0 | 20 | μA | $V_{RDin1..8} = 0.4$ V | 14 |

## 6.5     Testing the Electrical Parameters
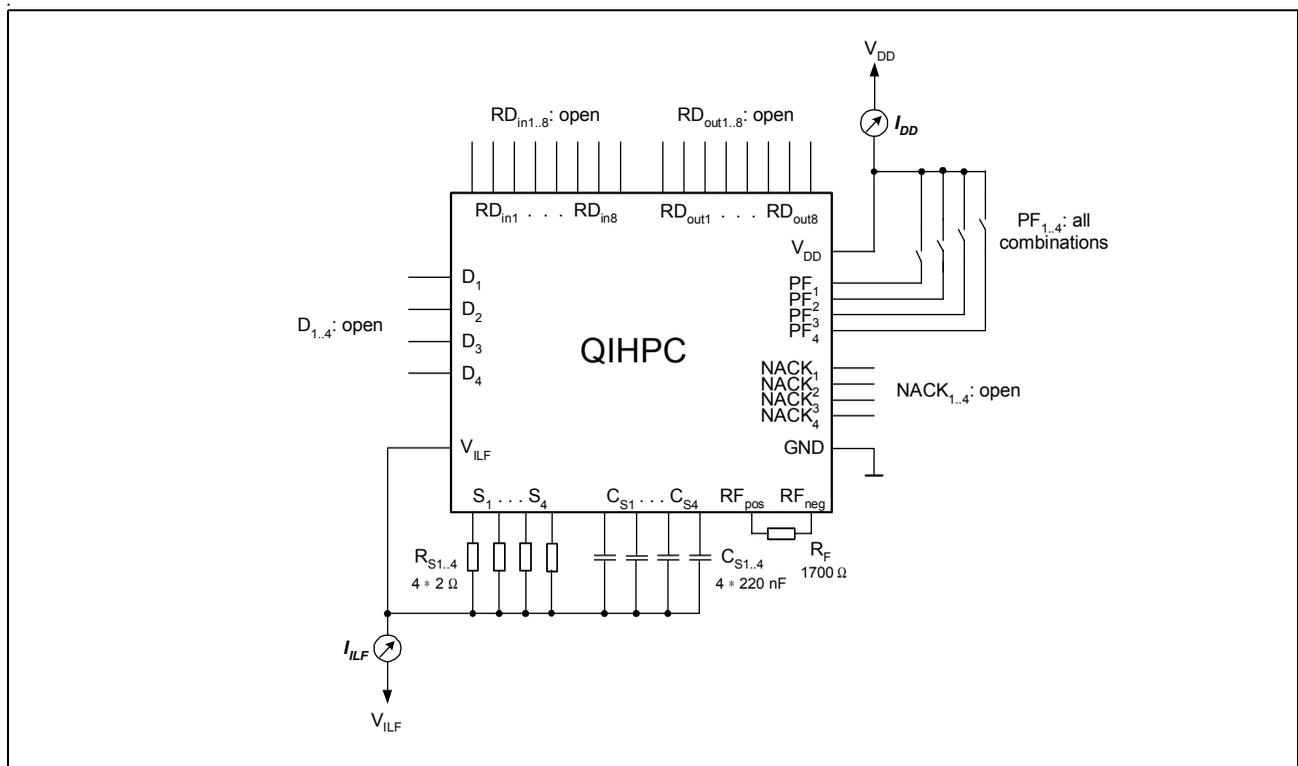


**Figure 10     Supply Currents**
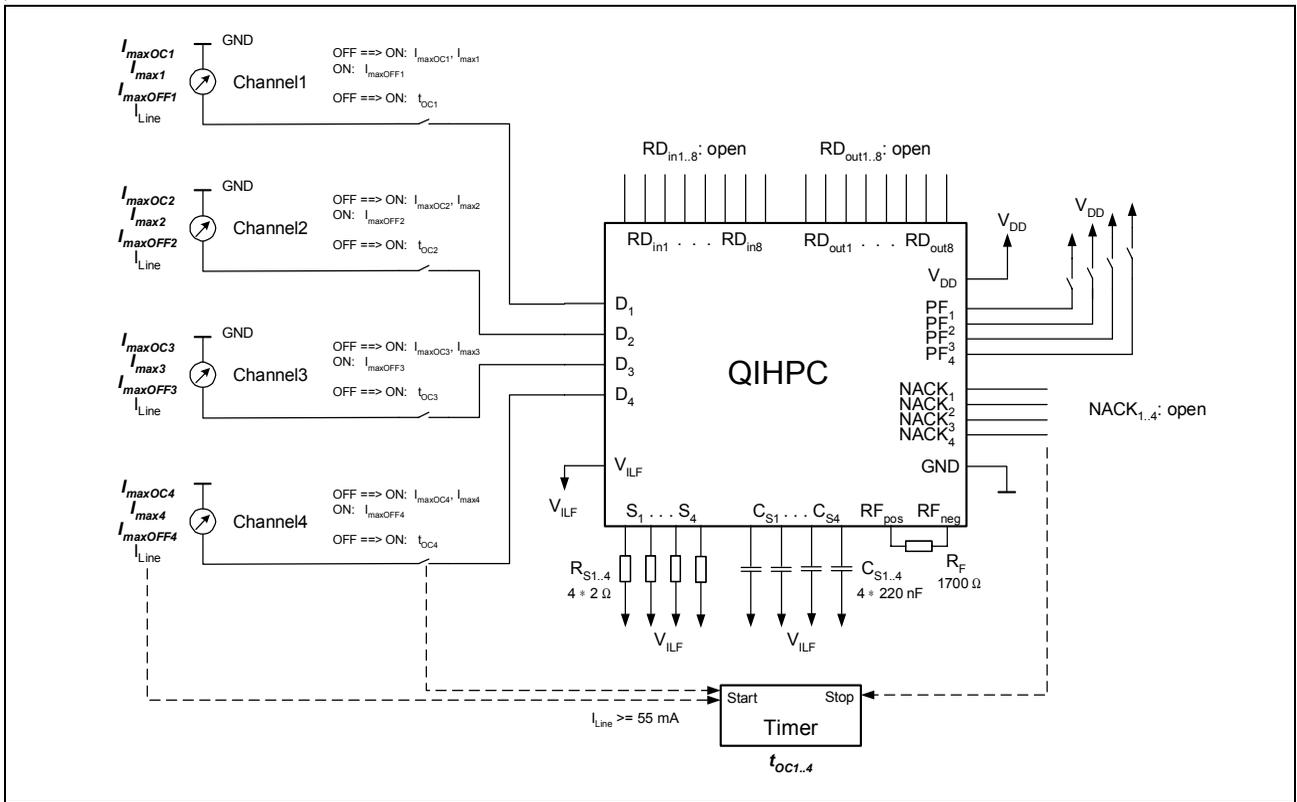
**Figure 11    Line Currents and Delay Time $t_{OC}$**
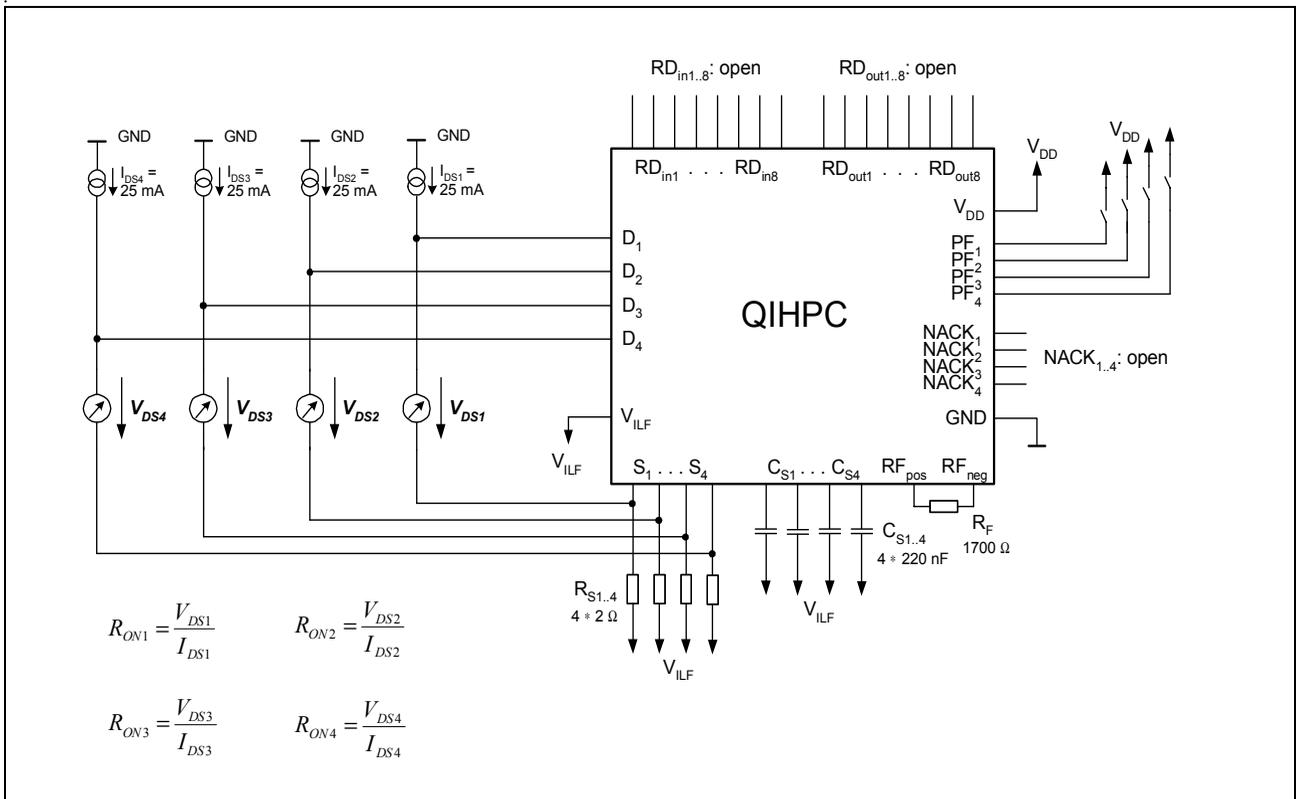


$$R_{ON1} = \frac{V_{DS1}}{I_{DS1}} \qquad R_{ON2} = \frac{V_{DS2}}{I_{DS2}}$$

$$R_{ON3} = \frac{V_{DS3}}{I_{DS3}} \qquad R_{ON4} = \frac{V_{DS4}}{I_{DS4}}$$

**Figure 12    DMOS-$R_{ON}$ resistance**

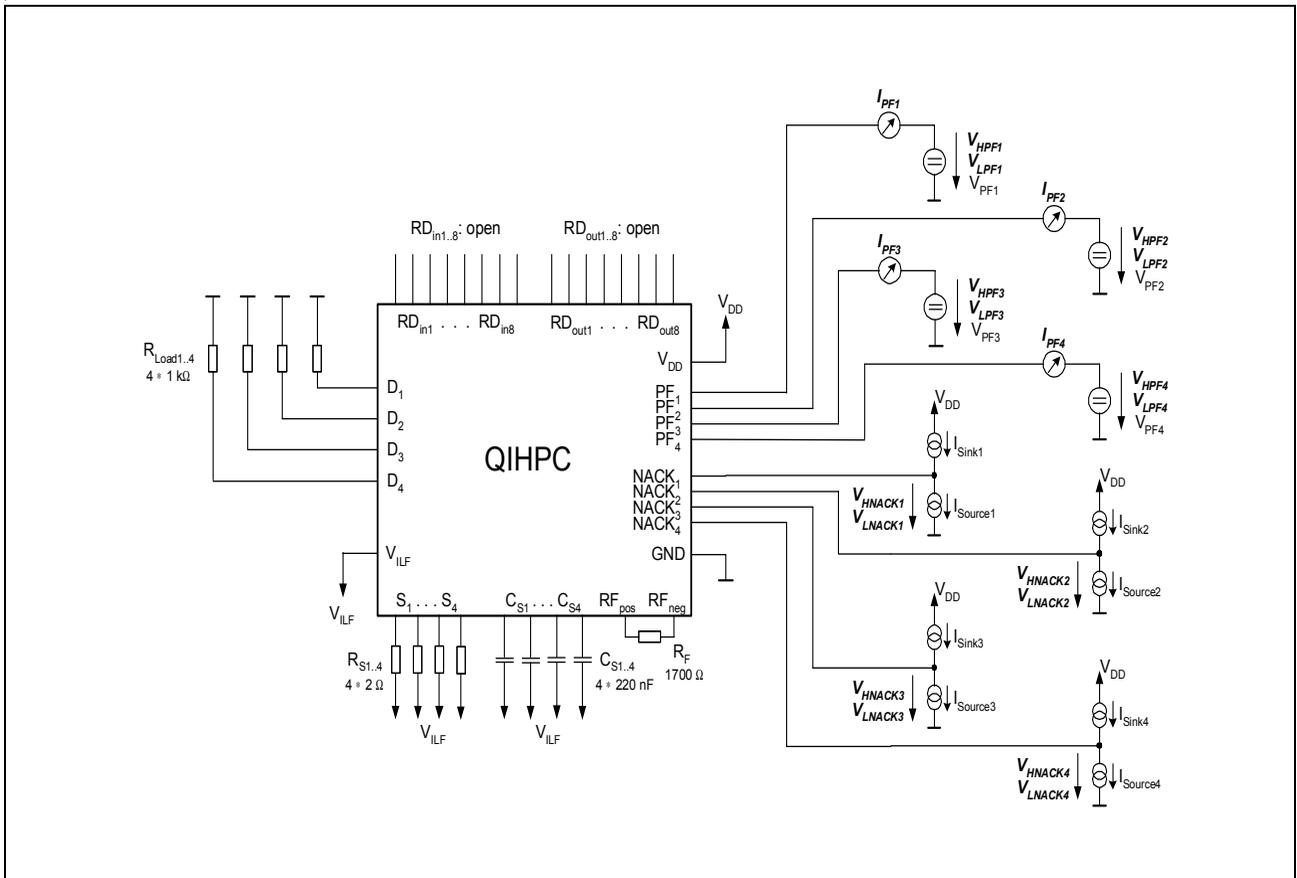**Figure 13    PF$_{1..4}$, Logic Input Levels and NACK$_{1..4}$, Logic Output Levels**
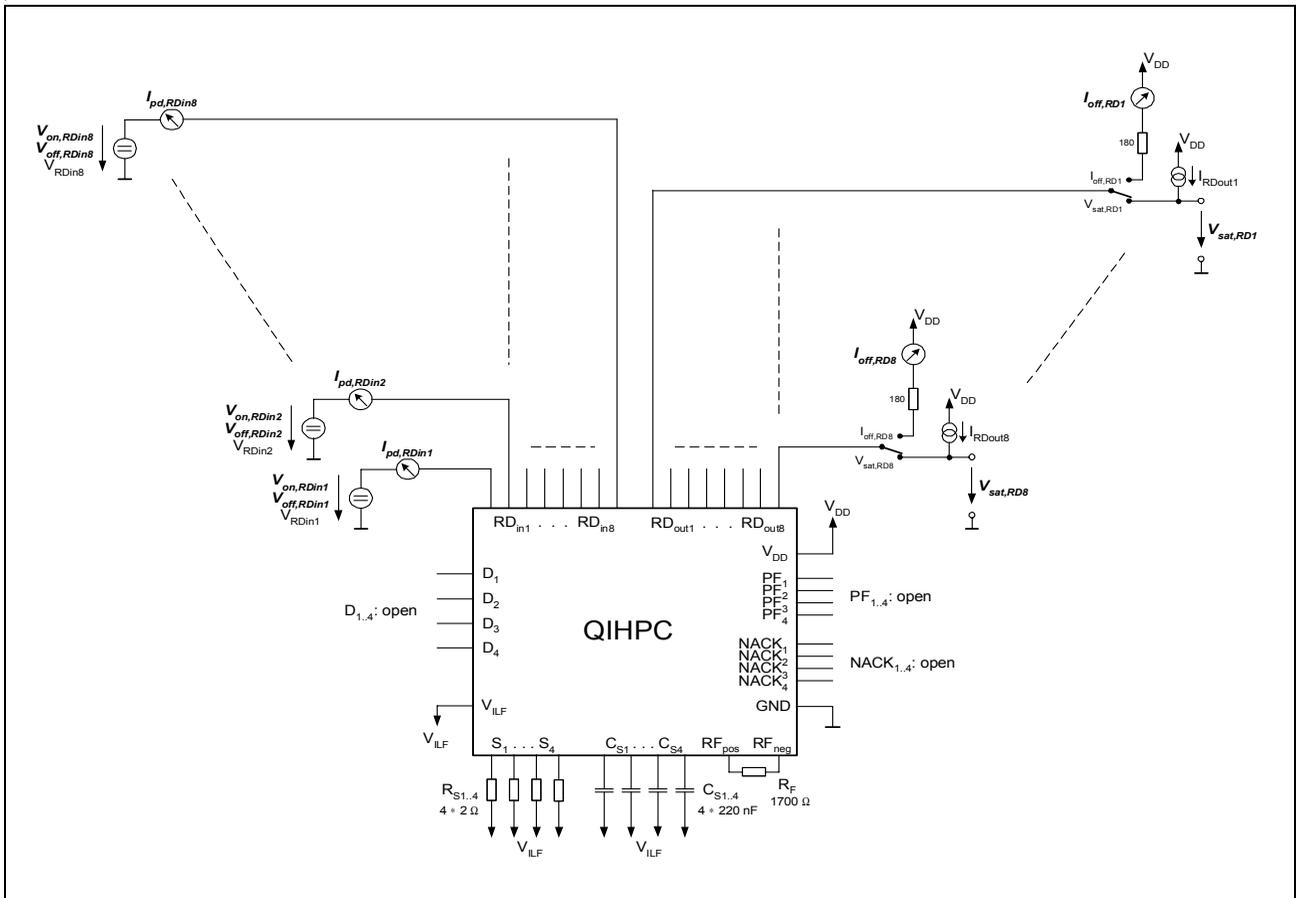
**Figure 14** RD$_{in1..8}$, **Relay Driver Inputs and RD$_{out1..8}$ Relay Driver Outputs**



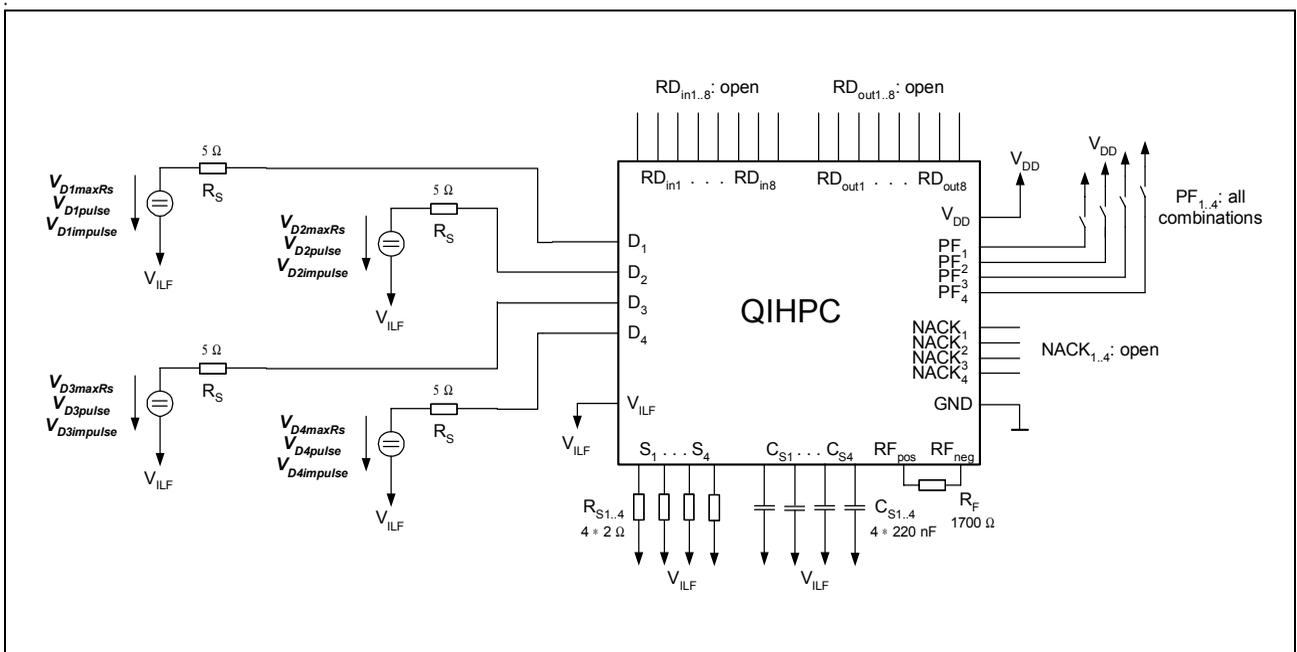**Figure 15** **Test circuit for maximum DC-voltages, pulse voltages and impulse voltages on pins D$_{1..4}$**

# 7 Package Outlines

**P-MQFP-44**

(Plastic Metric Quad Flat Package)



Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

# Infineon goes for Business Excellence

"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction."

Dr. Ulrich Schumacher