



PESD12VA-SF

Ultra small 12 V ESD protection device

11 June 2019

Product data sheet

1. General description

Bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small DSN0603-2 (SOD962) Surface-Mounted Device (SMD) package.

2. Features and benefits

- Bidirectional ESD protection of one line
- High reverse standoff voltage $V_{RWM} = 12\text{ V}$
- High surge robustness; $I_{PP} = 7\text{ A}$ for 8/20 μs pulse (average measured)

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Portable electronics

4. Quick reference data

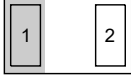
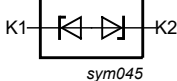
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	12	V
I_{PPM}	rated peak pulse current	$t_p = 8/20\text{ }\mu\text{s}$	[1]	-	-	6.1	A
V_{CL}	clamping voltage	$I_{PPM} = 6.1\text{ A}; 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	27	30	V

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>Transparent top view</p> <p>DSN0603-2 (SOD962)</p>	 <p>sym045</p>
2	K	cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD12VA-SF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 x 0.3 x 0.3 mm body	SOD962

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD12VA-SF	C9

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1]	-	6.1	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	30	kV
		air discharge	[2]	-	30	V

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.



Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

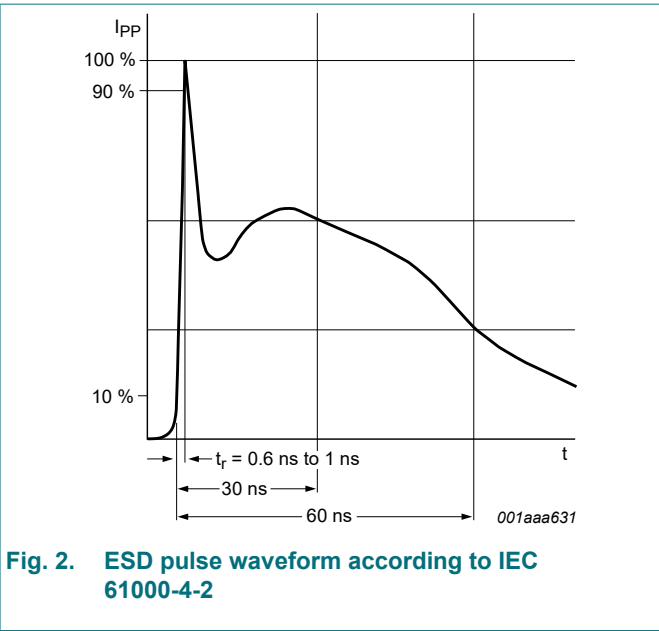


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25 \text{ }^\circ\text{C}$	-	-	12	V
V_{BR}	breakdown voltage	$I_R = 0.1 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$	14	15.1	16.4	V
I_{RM}	reverse leakage current	$V_{RWM} = 12 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	1	50	nA
C_d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	17	19	pF
V_{CL}	clamping voltage	$I_{PP} = 1 \text{ A}; 8/20 \mu\text{s}; T_{amb} = 25 \text{ }^\circ\text{C}$ [1]	-	16.5	-	V
		$I_{PPM} = 6.1 \text{ A}; 8/20 \mu\text{s}; T_{amb} = 25 \text{ }^\circ\text{C}$ [1]	-	27	30	V
		$I_{PP} = 16 \text{ A}; t_p = \text{TLP}; T_{amb} = 25 \text{ }^\circ\text{C}$ [2]	-	26	-	V
R_{dyn}	dynamic resistance	$I_R = 10 \text{ A}; T_{amb} = 25 \text{ }^\circ\text{C}$ [2]	-	0.7	-	Ω

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

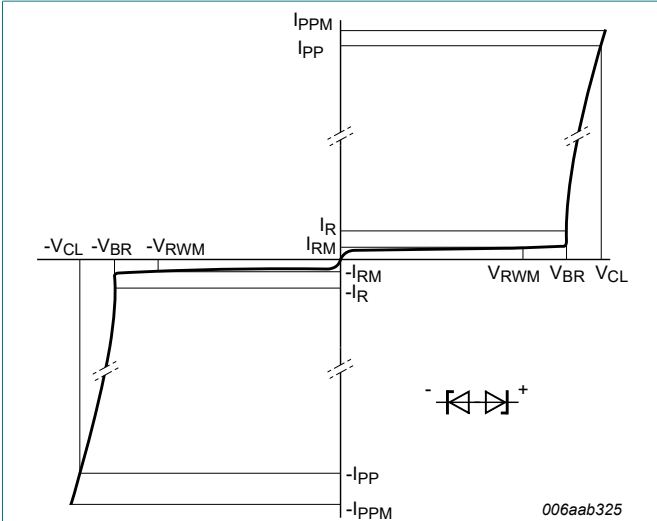


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

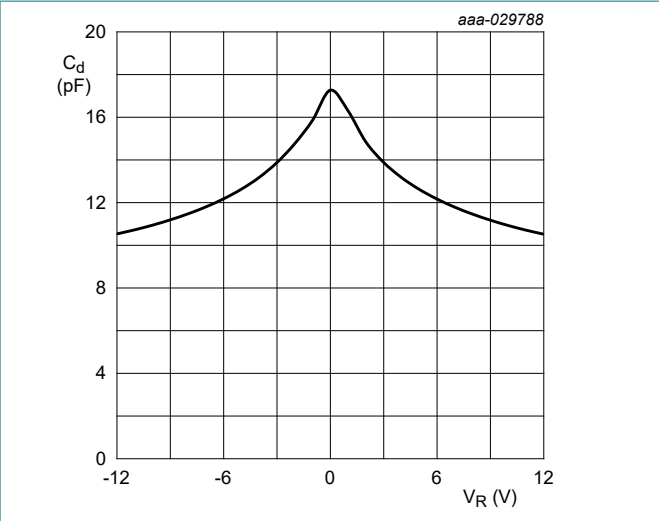


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

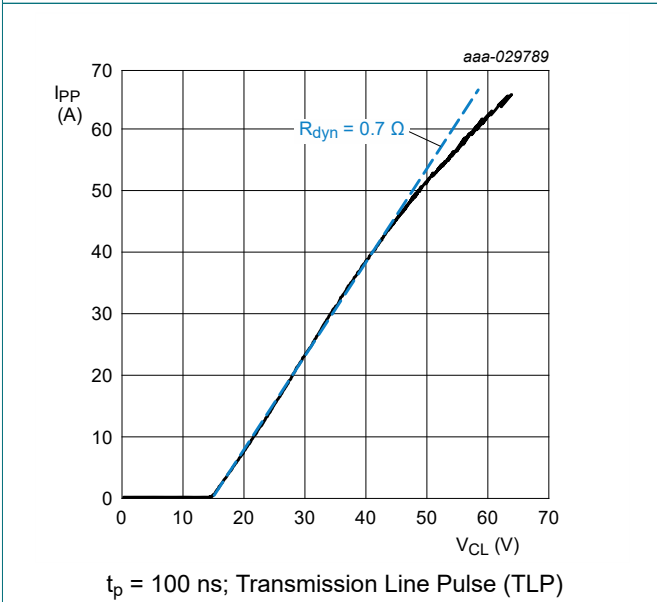


Fig. 5. Positive clamping voltage (TLP); typical values

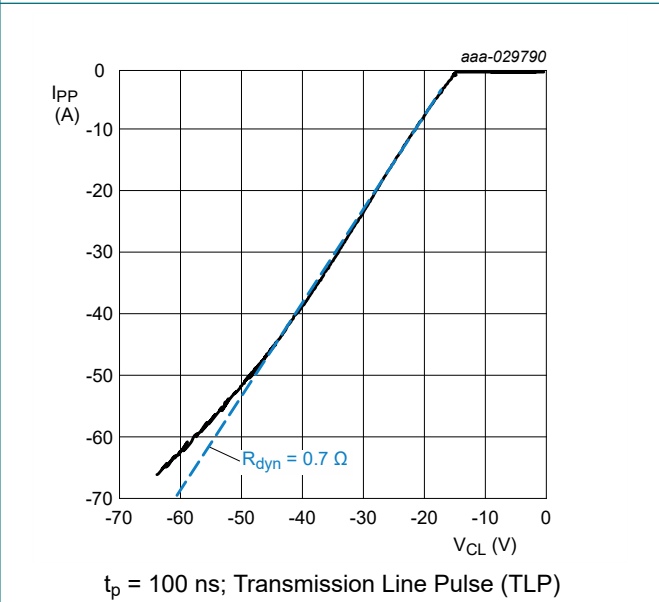
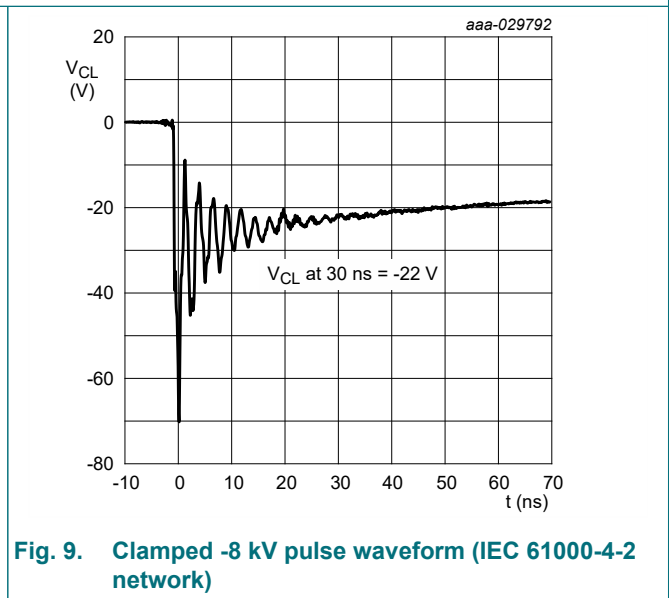
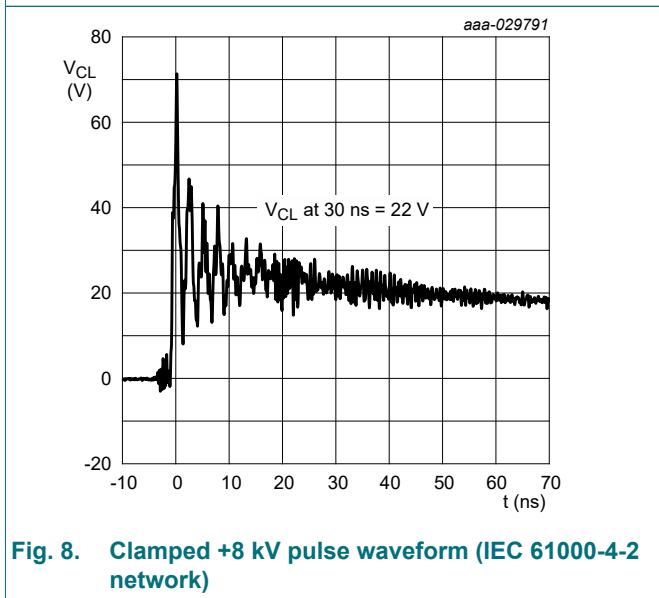


Fig. 6. Negative clamping voltage (TLP); typical values



Fig. 7. ESD clamping test setup and waveforms



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

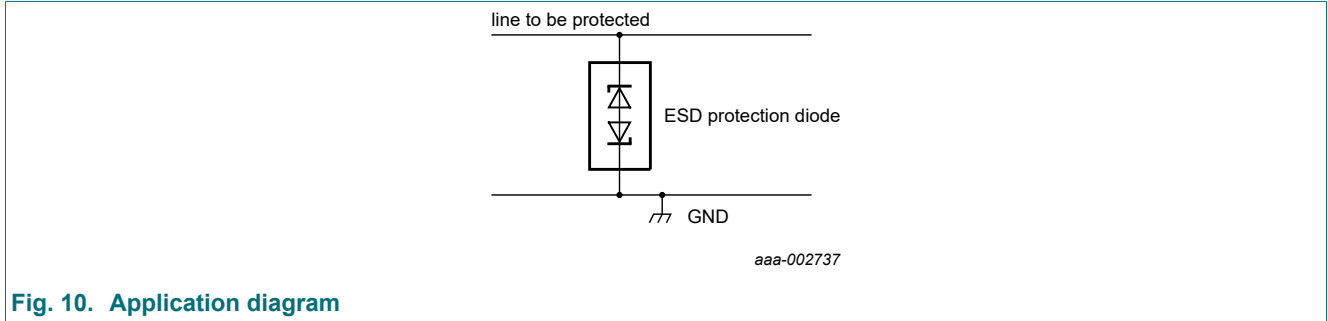


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

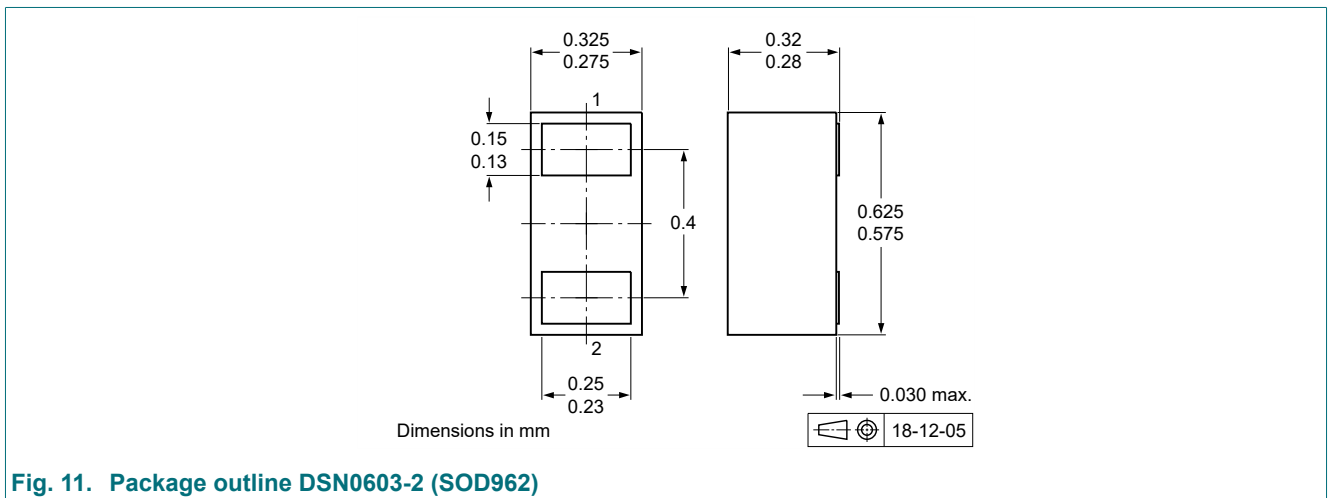
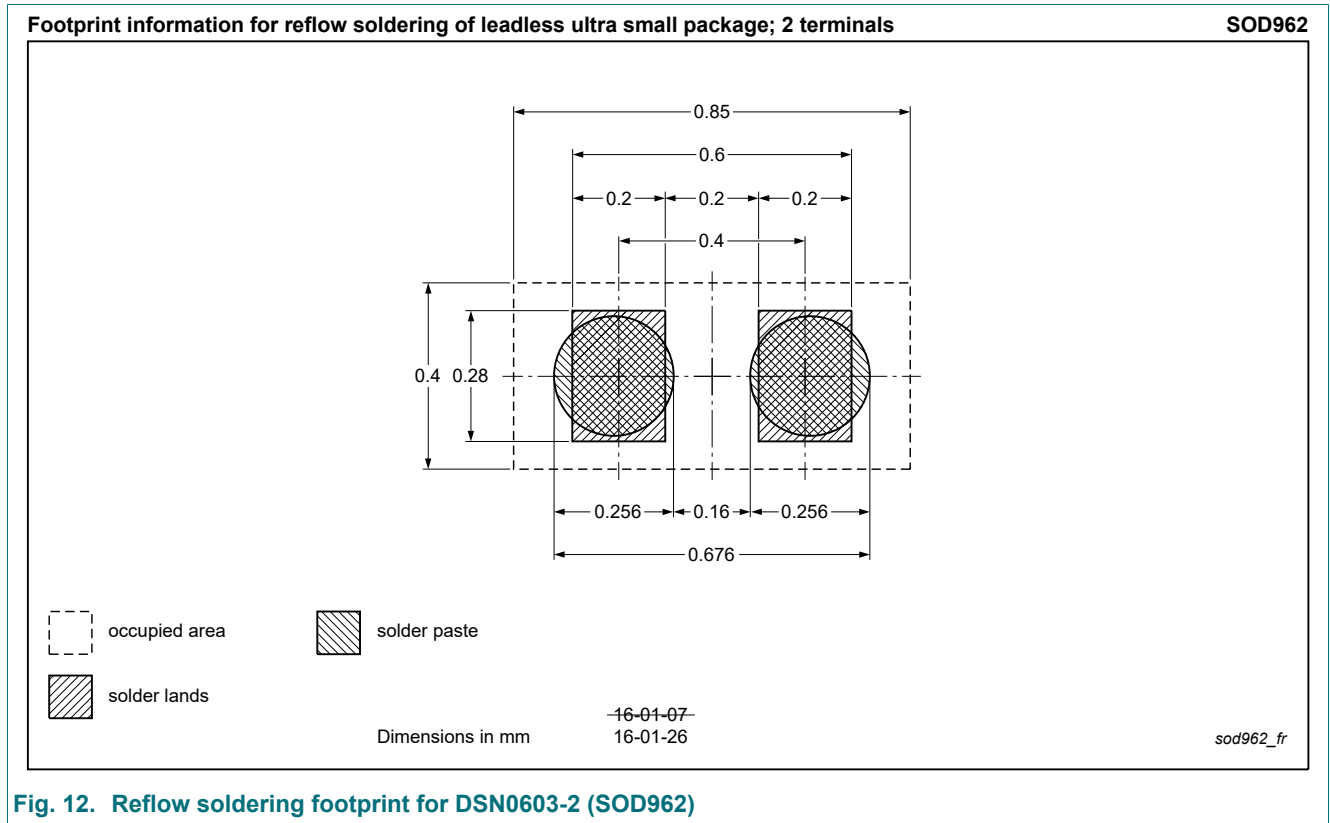


Fig. 11. Package outline DSN0603-2 (SOD962)

12. Soldering



13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD12VA-SF v.1	20190611	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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