PESD24VF1BL

Ultra low capacitance bidirectional ESD protection diode

14 February 2014 Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006-2 (SOD882) ultra small and leadless Surface-Mounted Device (SMD) plastic package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Ultra low diode capacitance C_d = 0.30 pF
- High reverse standoff voltage V_{RWM} = 24 V
- Ultra low leakage current: I_{RM} = 1 nA
- ESD protection up to 10 kV; IEC 61000-4-2
- AEC-Q101 qualified

3. Applications

- NFC antenna protection
- Protection of high-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	[1]	0.23	0.3	0.45	pF
V_{RWM}	reverse standoff voltage			-	-	24	V

[1] Measured from pin 1 to pin 2.

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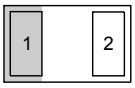
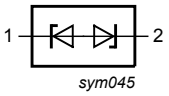
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DFN1006-2 (SOD882)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD24VF1BL	DFN1006-2	DFN1006-2: leadless ultra small plastic package; 2 terminals	SOD882

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD24VF1BL	7L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	peak pulse current	t_p = 8/20 µs	[1][2]	-	1	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (air discharge)	[1][3]	-	15	kV
		IEC 61000-4-2 (contact discharge)	[1][3]	-	10	kV
		MIL-STD-883 (human body model)	[1]	-	10	kV

[1] Measured from pin 1 to pin 2.
[2] According to IEC 61000-4-5 and IEC 61643-321.
[3] Device stressed with ten non-repetitive ESD pulses.

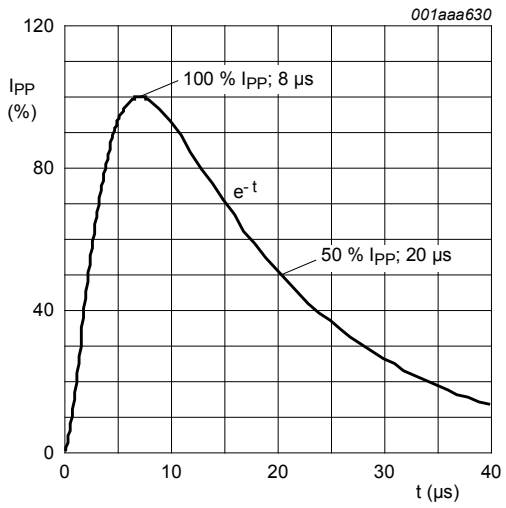


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

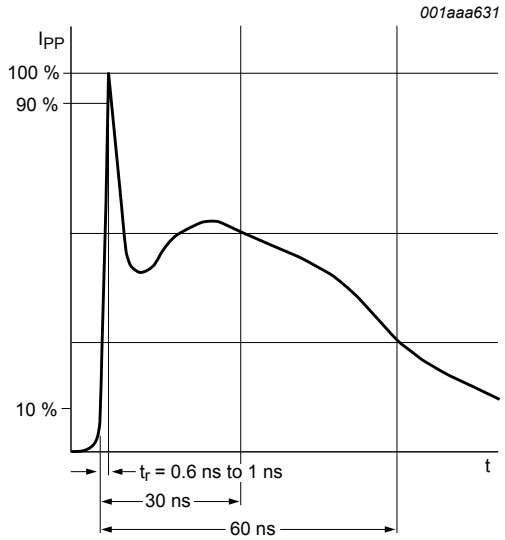


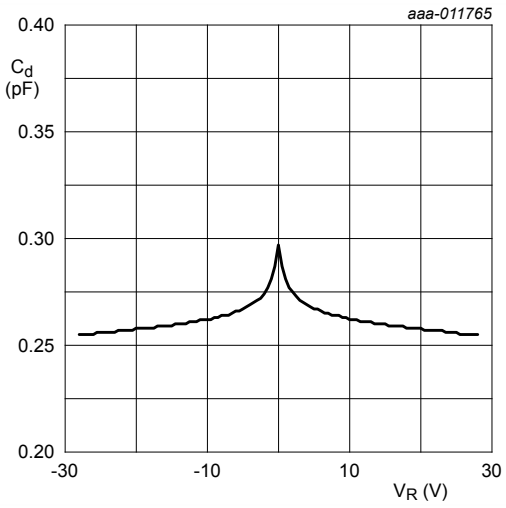
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-	-	24	V
I_{RM}	reverse leakage current	V_R = 24 V	[1]	-	1	30	nA
V_{CL}	clamping voltage	I_{PP} = 1 A	[1][2]	-	-	17	V
V_{BR}	breakdown voltage	I_R = 10 mA	[1]	24.5	28	31.5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	[1]	0.23	0.3	0.45	pF
R_{dyn}	dynamic resistance	I_R = 7.5 A	[3][1]	-	0.8	-	Ω

[1] Measured from pin 1 to pin 2.
[2] According to IEC 61000-4-5 and IEC 61643-321.
[3] Non-repetitive current pulse; Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.



f = 1 MHz; T_{amb} = 25 °C

Fig. 3. Diode capacitance as a function of reverse voltage; typical values

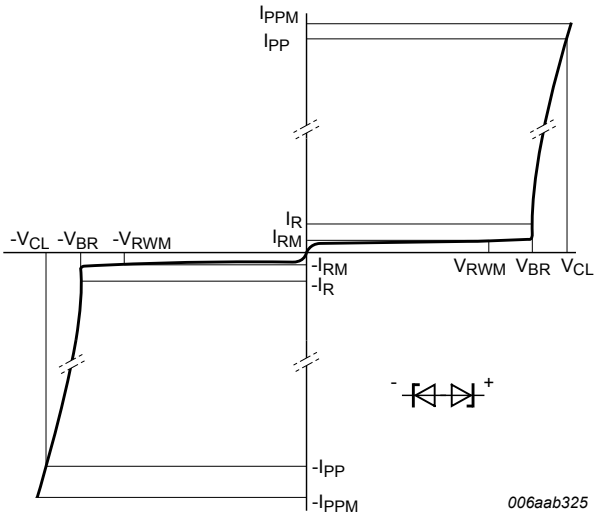
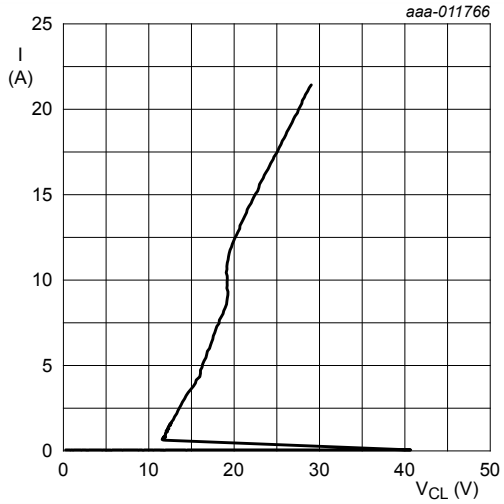


Fig. 4. V-I characteristics for a bidirectional ESD protection diode



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 5. Dynamic resistance

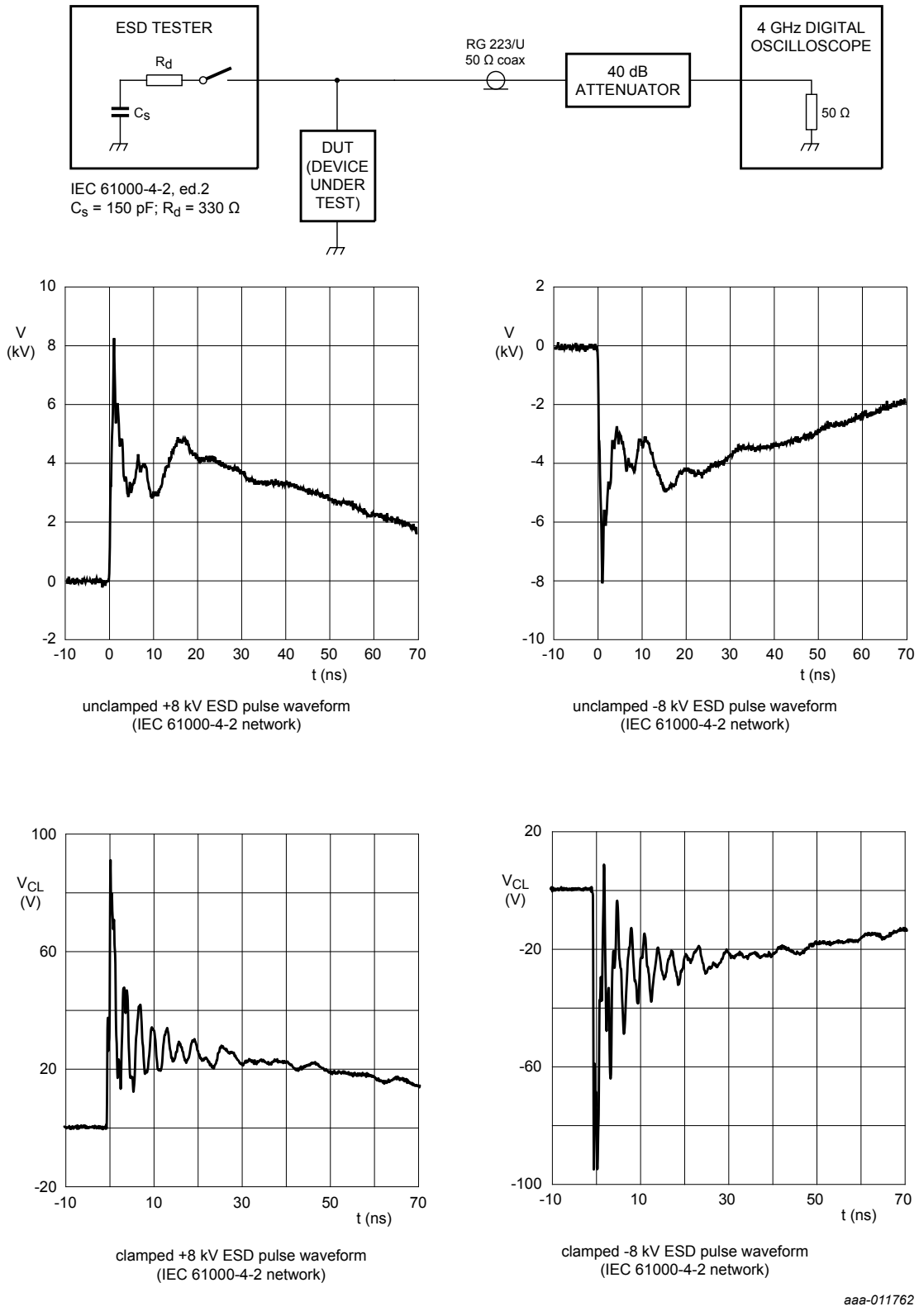


Fig. 6. ESD clamping test setup and waveforms

10. Test information

10.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

11. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

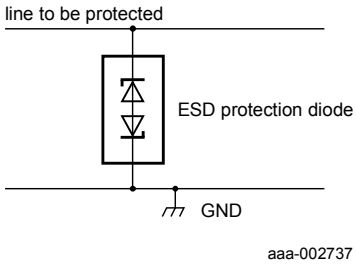


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

12. Package outline

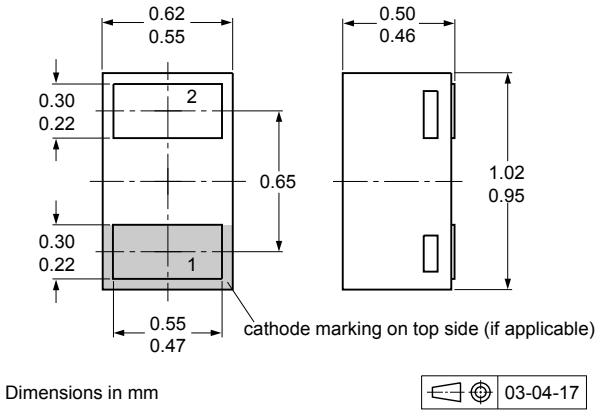


Fig. 8. Package outline DFN1006-2 (SOD882)

13. Soldering

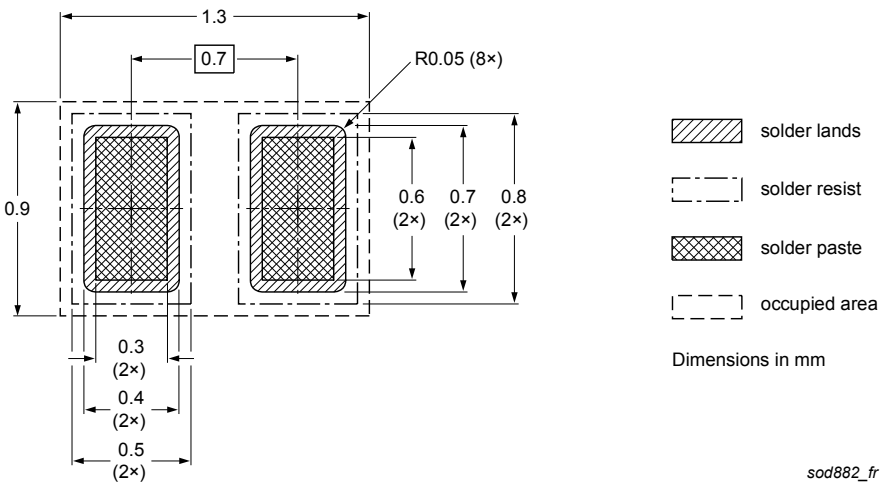


Fig. 9. Reflow soldering footprint for DFN1006-2 (SOD882)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD24VF1BL v.1	20140214	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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