PESD2ETH-AX

Ultra low capacitance double rail-to-rail ESD protection diode

28 September 2018 **Product data sheet**

1. General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT143B Surface-Mounted Device (SMD) plastic package.

The device is designed to protect two high-speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

The device integrates two ultra low capacitance rail-to-rail diodes and one additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

2. Features and benefits

- ESD protection of two high-speed data lines
- Ultra low capacitance: C_d = 1.8 pF
- IEC 61000-4-2 up to 12 kV
- ISO 10605 (330 pF, 2 kΩ) up to 15 kV
- Very low reverse current
- AEC-Q101 qualified

3. Applications

- 100BASE-T1 / OPEN Alliance BroadR-Reach automotive Ethernet
- Low-Voltage Differential Signaling (LVDS) automotive
- USB 2.0 automotive

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Zener diode							
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	16	-	pF
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
Per channel							
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[2]	-	1.8	-	pF

[1] Measured from pin 4 to ground.
[2] Measured from pin 2 and 3 to ground.

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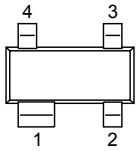
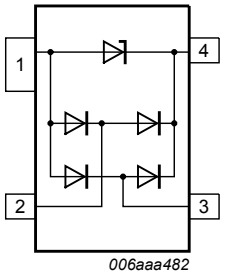
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND	ground	 SOT143B	
2	I/O 1	input/output 1		
3	I/O 2	input/output 2		
4	V_{CC}	supply line		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2ETH-AX	SOT143B	plastic surface-mounted package; 4 leads	SOT143B

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD2ETH-AX	2A%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; level 4; contact discharge		-	12	kV

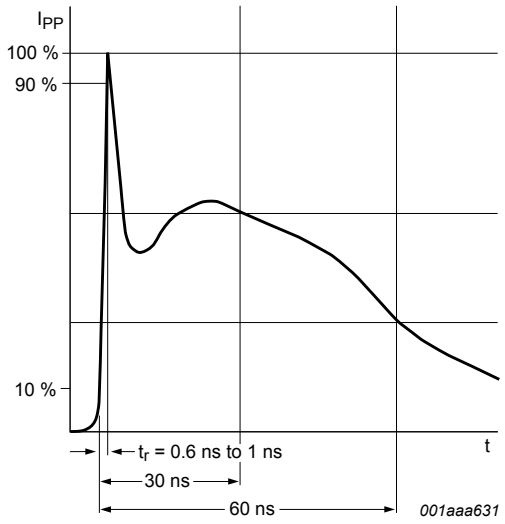


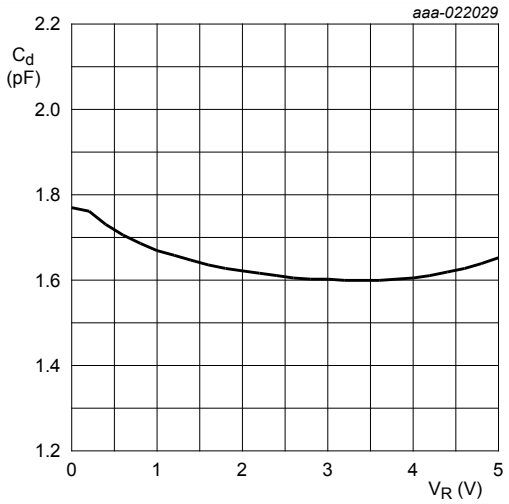
Fig. 1. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Zener diode							
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5.5	V
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25 °C	[1]	6	-	9	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	16	-	pF
Per channel							
V_F	forward voltage	I_F = 1 mA; T_{amb} = 25 °C	[2]	-	0.7	-	V
I_R	reverse current	V_R = 3 V; T_{amb} = 25 °C	[3]	-	1	100	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[2]	-	1.8	-	pF

[1] Measured from pin 4 to ground.
[2] Measured from pin 2 and 3 to ground.
[3] Measured from pin 2, 3 and 4 to ground.



f = 1 MHz; T_{amb} = 25 °C
Measured from pin 2 and 3 to ground.

Fig. 2. Diode capacitance as a function of reverse voltage; typical values

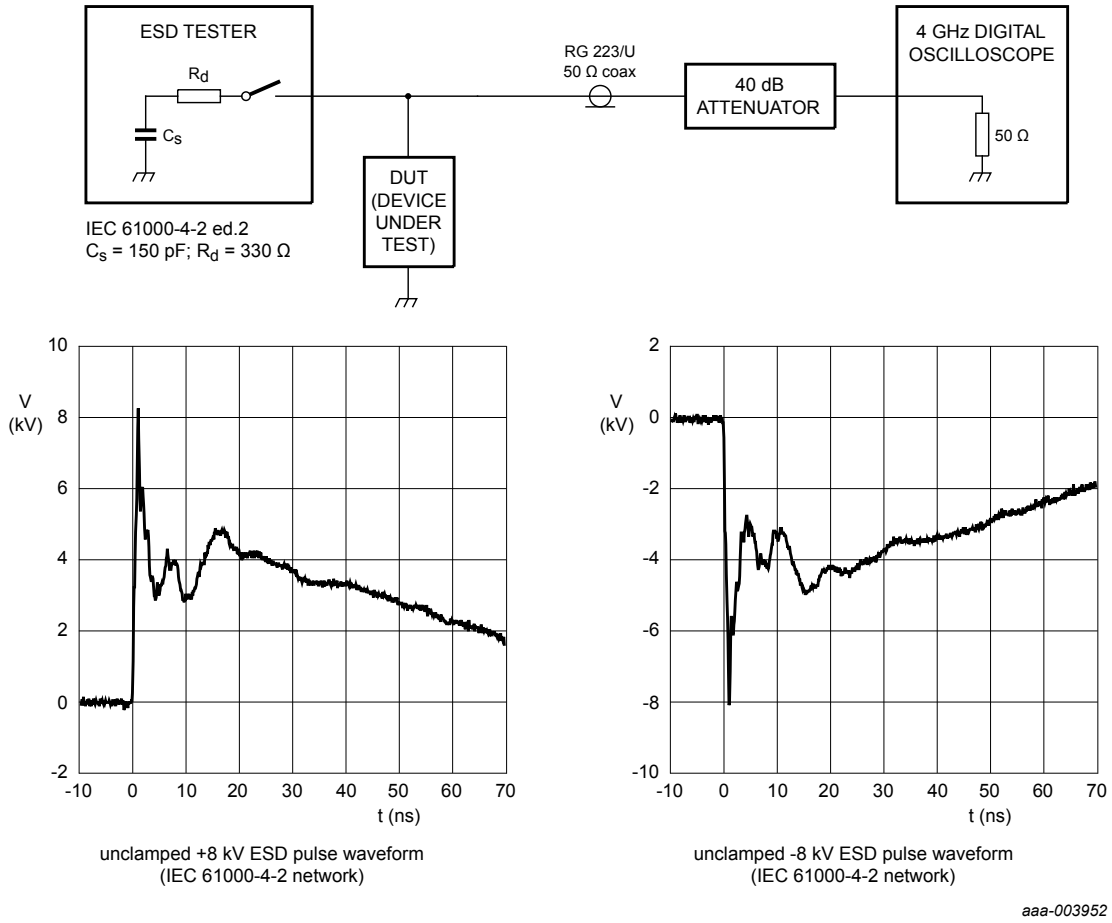


Fig. 3. ESD clamping test setup and waveforms

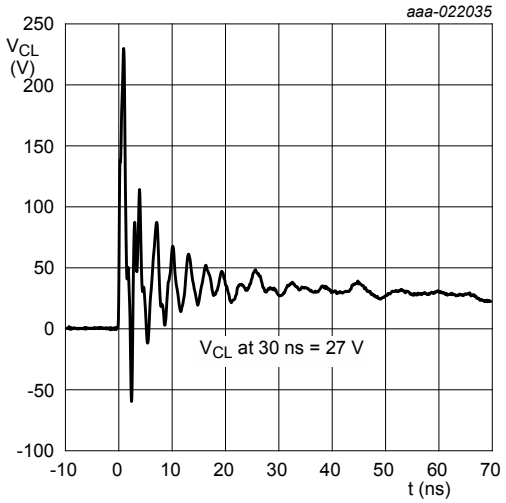


Fig. 4. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

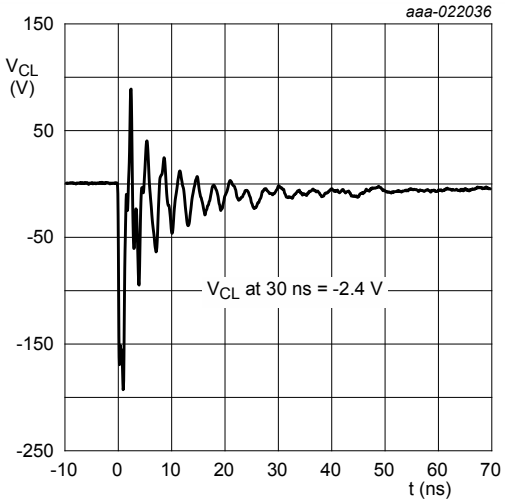


Fig. 5. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

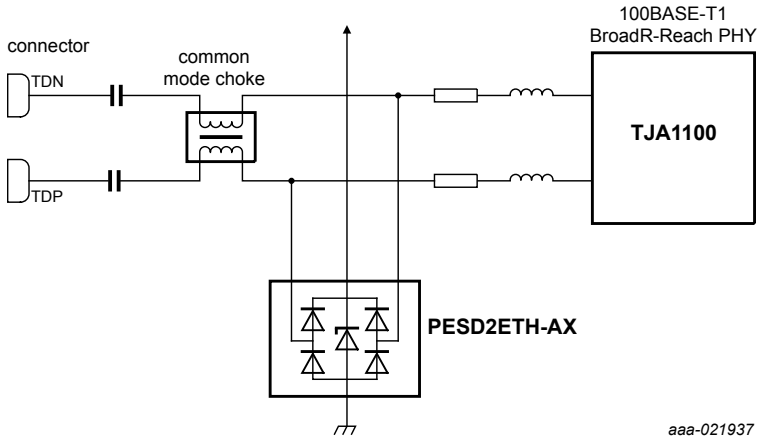


Fig. 6. Application diagram: BroadR-Reach PHY / 100BASE-T1

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

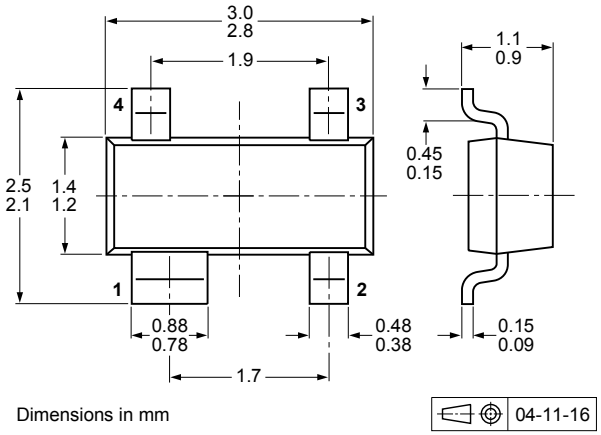


Fig. 7. Package outline SOT143B

13. Soldering

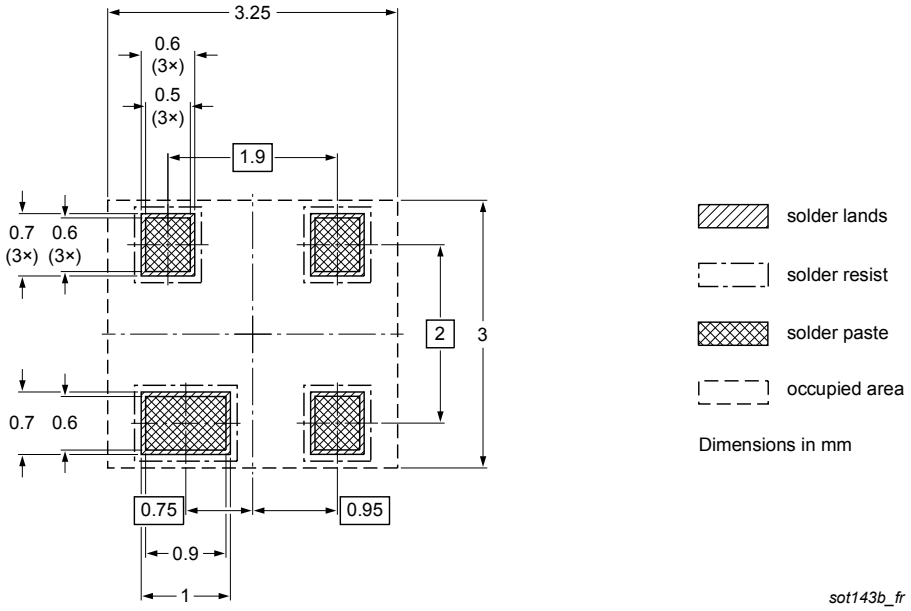


Fig. 8. Reflow soldering footprint for SOT143B

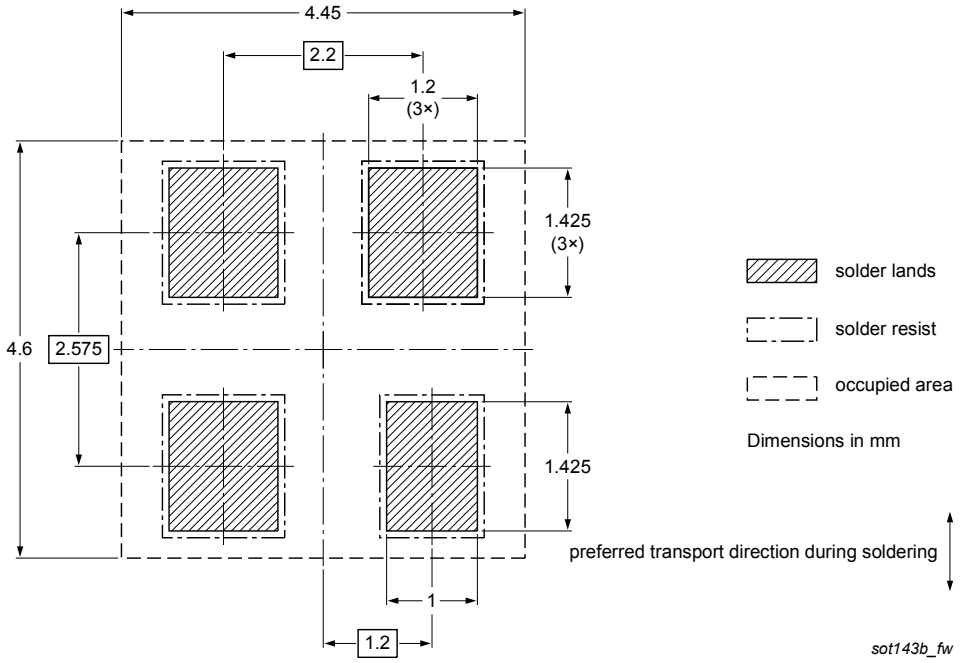


Fig. 9. Wave soldering footprint for SOT143B

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2ETH-AX v.2	20180928	Product data sheet	-	PESD2ETH-AX v.1
Modifications:	• Limiting values: Updated ambient temperature and storage temperature.			
PESD2ETH-AX v.1	20160224	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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