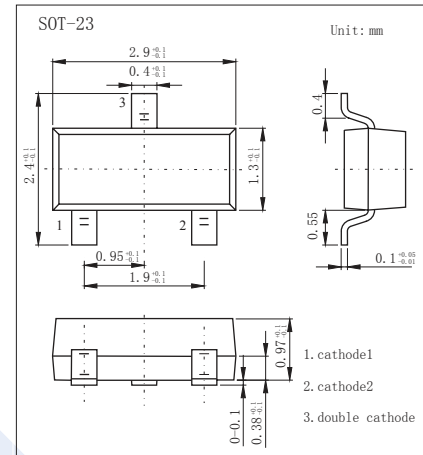
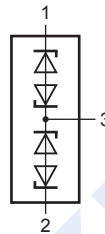


ESD Protection Diodes

PESDxL2BT series

■ Features

- ESD protection of two lines
- Max. peak pulse power: $P_{PP}=350W$
- Low clamping voltage: $V_{CL}=26V$
- Small SMD plastic package
- Ultra low leakage current: $I_{RM}<90nA$
- ESD protection up to 23 kV
- IEC61000-4-2, level4 (ESD)
- IEC61000-4-5 (surge); $I_{PP}=15A$



■ Absolute Maximum Ratings

Parameter		Symbol	PESD 3V3L2BT	PESD 5V0L2BT	PESD 12VL2BT	PESD 15VL2BT	PESD 24VL2BT	Unit
Electrostatic discharge voltage	IEC61000-4-2 (Note 2,3) (contact discharge)	V_{ESD}	30				23	KV
	HBM MIL-STD883		10					
Peak pulse power $t_p=8/20 \mu s$ (Note 1,2)		P_{PP}	350		200			W
Peak pulse current $t_p=8/20 \mu s$ (Note 1,2)		I_{PP}	15	13	5	3		A
Junction temperature		T_j	150					°C
Ambient temperature		T_{amb}	-65 to +150					
Storage temperature		T_{stg}	-65 to +150					

Note 1: Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5.

Note 2: Measured from pin 1 to 3 or 2 to 3.

Note 3: Device stressed with ten non-repetitive ESD pulses.

ESD Protection Diodes

PESDxL2BT series

■ Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse standoff voltage PESD3V3L2BT PESD5V0L2BT PESD12VL2BT PESD15VL2BT PESD24VL2BT	V _{RWM}				3.3 5.0 12 15 24	V V V V V
Reverse leakage current PESD3V3L2BT PESD5V0L2BT PESD12VL2BT PESD15VL2BT PESD24VL2BT		V _{RWM} =3.3V V _{RWM} =5.0V V _{RWM} =12V V _{RWM} =15V V _{RWM} =24V			2 1 50 50 50	μA μA nA nA nA
Breakdown voltage PESD3V3L2BT PESD5V0L2BT PESD12VL2BT PESD15VL2BT PESD24VL2BT	V _{BR}	I _R =5mA	5.8 7.0 14.2 17.1 25.4	6.4 7.6 15.8 18.8 27.8	6.9 8.2 16.7 20.3 30.3	V V V V V
Diode capacitance PESD3V3L2BT PESD5V0L2BT PESD12VL2BT PESD15VL2BT PESD24VL2BT		V _R =0V; f=1MHz			101 75 19 16 11	pF pF pF pF pF
Clamping voltage (Note 1,2) PESD3V3L2BT PESD5V0L2BT PESD12VL2BT PESD15VL2BT PESD24VL2BT	V _{CL}	I _{PP} =1A I _{PP} =15A I _{PP} =1A I _{PP} =13A I _{PP} =1A I _{PP} =5A I _{PP} =1A I _{PP} =5A I _{PP} =1A I _{PP} =3A			8 26 10 28 20 37 25 44 40 70	V V V V V V V V V V
Differential resistance PESD3V3L2BT PESD5V0L2BT PESD12VL2BT PESD15VL2BT PESD24VL2BT		I _R =1mA			400 80 200 225 300	Ω Ω Ω Ω Ω

Note 1: Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5.

Note 2: Measured from pin 1 to 3 or 2 to 3.

■ Marking

Type	PESD3V3L2BT	PESD5V0L2BT	PESD12VL2BT	PESD15VL2BT	PESD24VL2BT
Marking	V3W	V4W	V5W	V6W	V7W

ESD Protection Diodes

PESDxL2BT series

■ Typical Characteristics

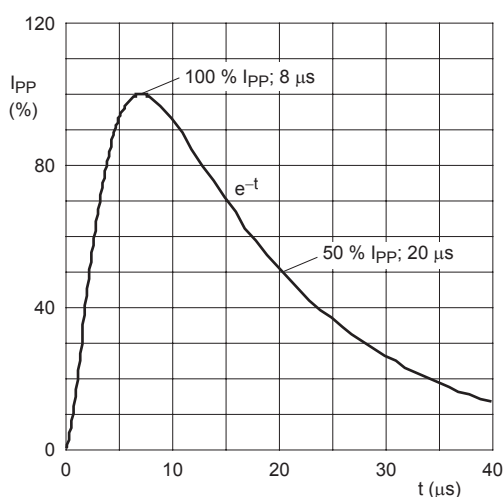


Fig 1. 8/20 μs pulse waveform according to IEC 61000-4-5

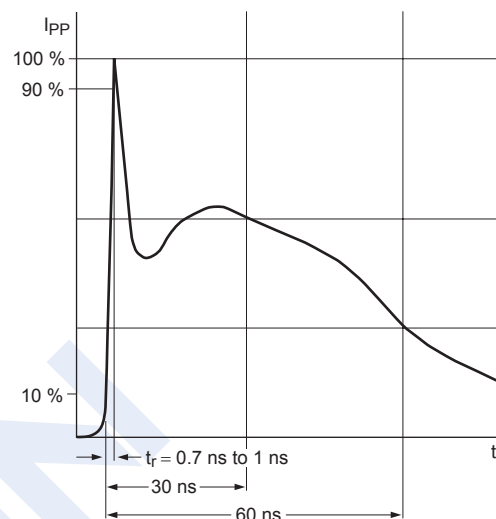
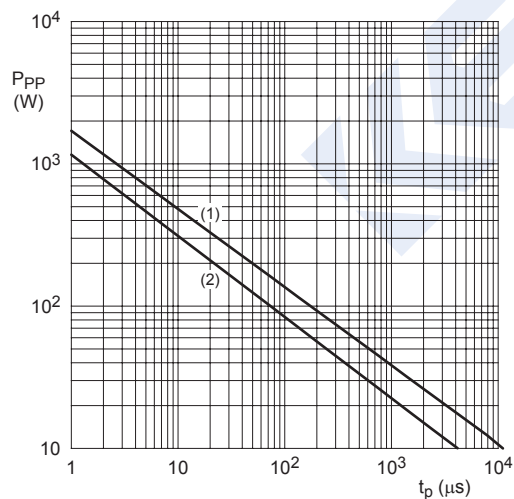


Fig 2. ESD pulse waveform according to IEC 61000-4-2



$T_{amb} = 25$ °C

- (1) PESD3V3L2BT and PESD5V0L2BT
(2) PESD12VL2BT, PESD15VL2BT, PESD24VL2BT

Fig 3. Peak pulse power as a function of exponential pulse duration t_p ; typical values

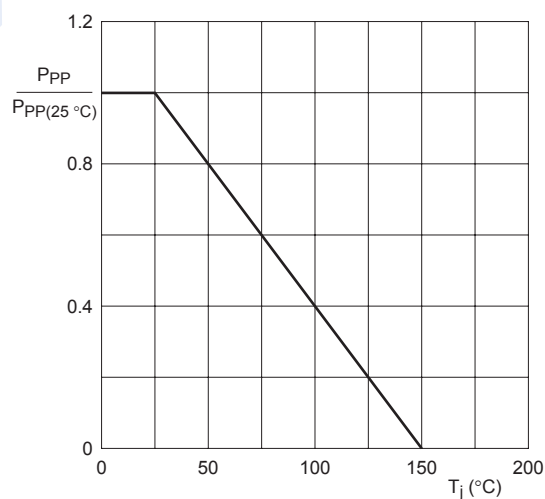
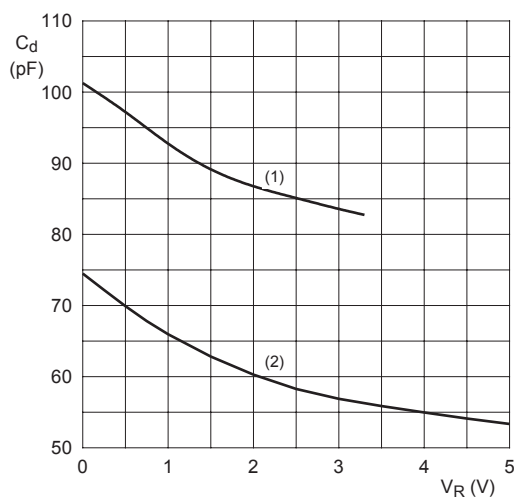


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values

ESD Protection Diodes

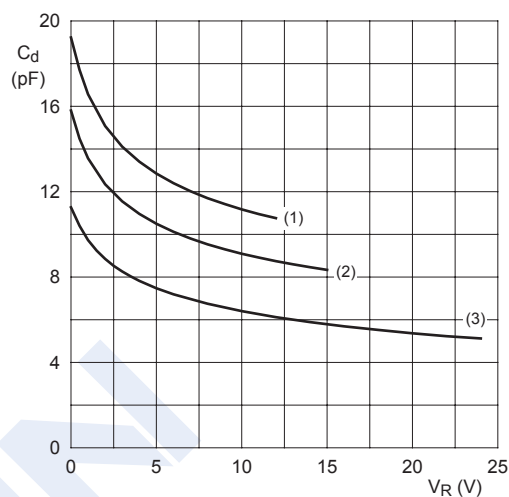
PESDxL2BT series



$T_{amb} = 25\text{ }^{\circ}\text{C}$; $f = 1\text{ MHz}$

- (1) PESD3V3L2BT
(2) PESD5V0L2BT

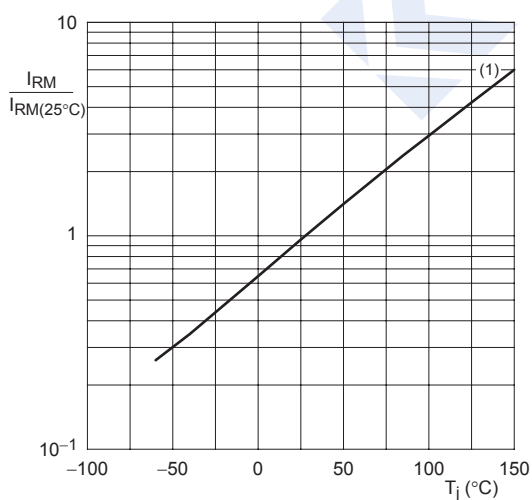
Fig 5. Diode capacitance as a function of reverse voltage; typical values



$T_{amb} = 25\text{ }^{\circ}\text{C}$; $f = 1\text{ MHz}$

- (1) PESD12VL2BT
(2) PESD15VL2BT
(3) PESD24VL2BT

Fig 6. Diode capacitance as a function of reverse voltage; typical values



- (1) PESD3V3L2BT, PESD5V0L2BT
PESD12VL2BT, PESD15VL2BT and
PESD24VL2BT: $I_{RM} < 20\text{ nA}$; $T_j = 150\text{ }^{\circ}\text{C}$

Fig 7. Relative variation of reverse leakage current as a function of junction temperature; typical values

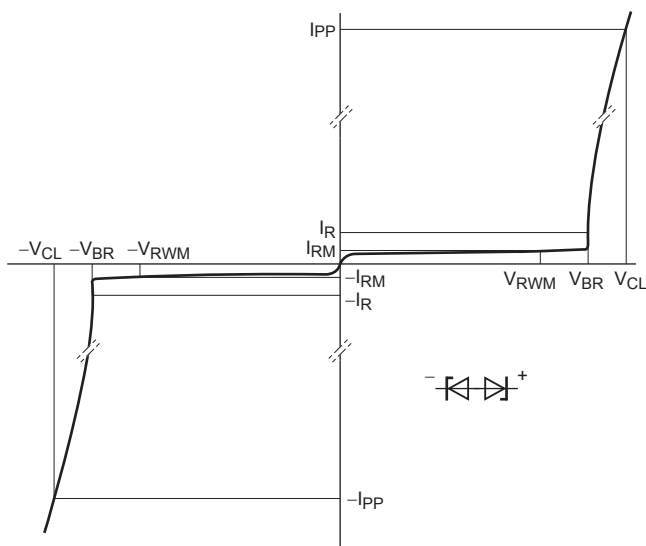


Fig 8. V-I characteristics for a bidirectional ESD protection diode

ESD Protection Diodes

PESDxL2BT series

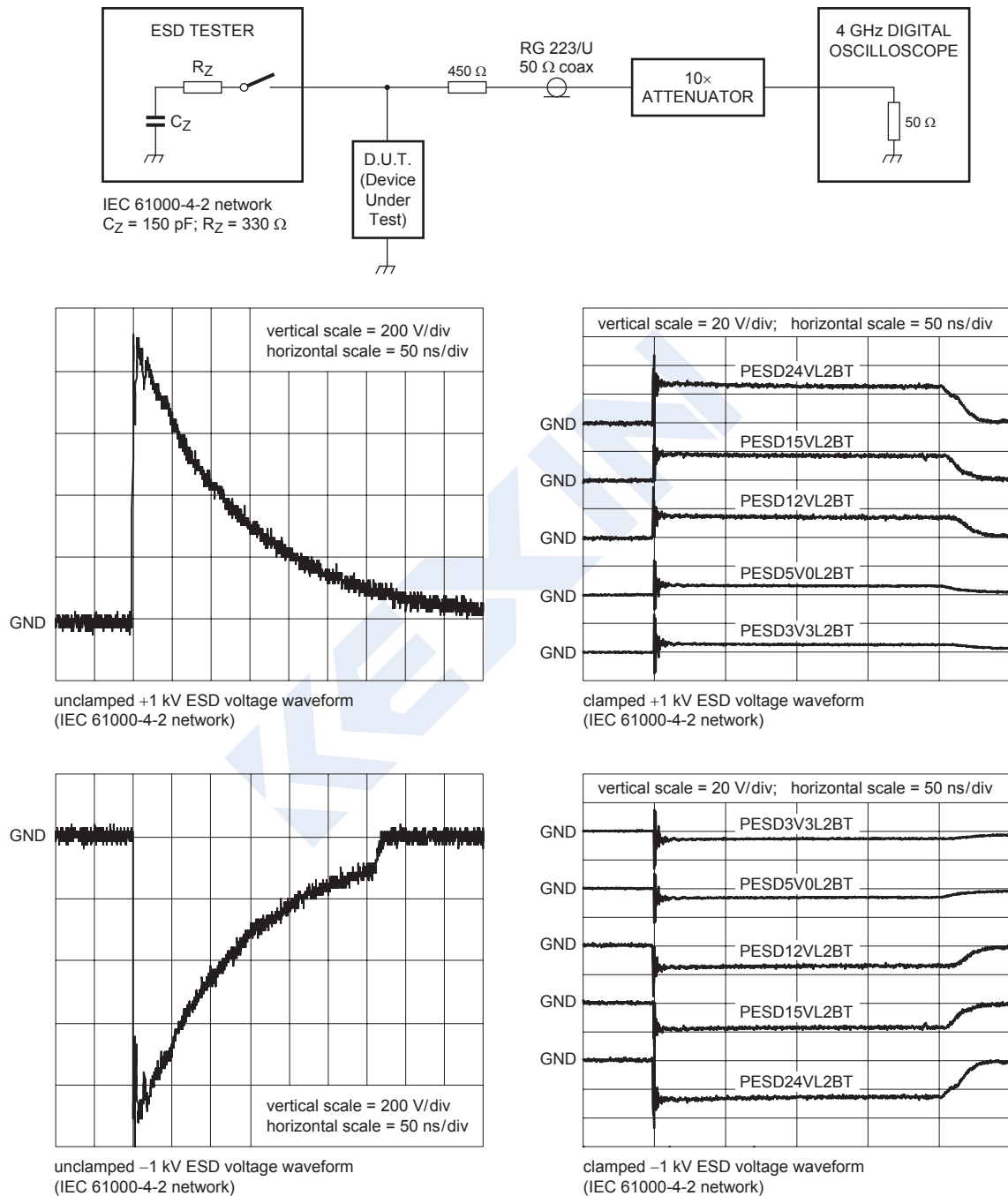


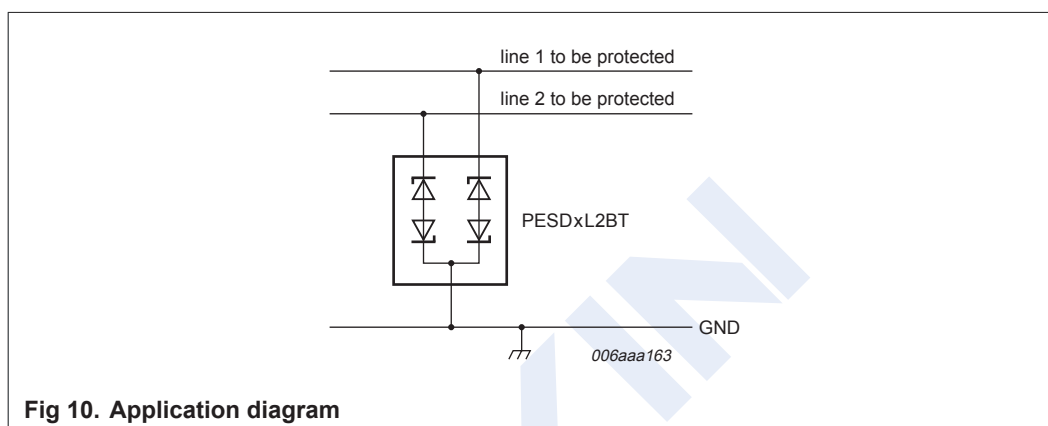
Fig 9. ESD clamping test setup and waveforms

ESD Protection Diodes

PESDxL2BT series

■ Application information

The PESDxL2BT series is designed for the protection of two bidirectional signal lines from the damage caused by ESD and surge pulses. The PESDxL2BT series may be used on lines where the signal polarities are above and below ground. The PESDxL2BT series provides a surge capability of up to 350 W per line for an 8/20 μ s waveform.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESDxL2BT as close to the input terminal or connector as possible.
2. The path length between the PESDxL2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.