PESD5V0F5UF

Femtofarad unidirectional fivefold ESD protection array

Rev. 1 — 17 July 2012 Product data sheet

1. Product profile

1.1 General description

Femtofarad capacitance unidirectional ElectroStatic Discharge (ESD) protection diode array designed to protect up to five signal lines from the damage caused by ESD and other transients. The device is encapsulated in a leadless ultra small DFN1410-6 (SOT886) Surface-Mounted Device (SMD) plastic package.

The combination of extremely low capacitance, high ESD maximum rating and ultra small package makes the device ideal for high-speed data line protection and antenna protection applications.

1.2 Features and benefits

- ESD protection of up to 5 lines
- Low diode capacitance C_d = 0.55 pF
- Ultra low leakage current I_{RM} < 1 nA
- ESD protection up to 8 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PPM} = 2 A
- AEC-Q101 qualified

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- Portable electronics
- SIM card protection
- High-speed data lines

1.4 Quick reference data

Table 1. Quick reference data

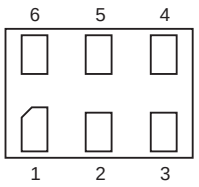
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	-	0.55	0.7	pF

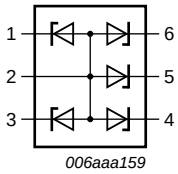
2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode		
2	common anode		
3	cathode		
4	cathode		
5	cathode		
6	cathode		



Transparent top view



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3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0F5UF	DFN1410-6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

4. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0F5UF	UT

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 μs	[1][2]	-	2	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−55	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.

[2] Measured from pin 1, 3, 4, 5 or 6 to pin 2.

Table 6. ESD maximum ratings

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	-	8	kV
		IEC 61000-4-2 (air discharge)	[1][2]	-	8	kV
		machine model	[2]	-	400	V
		MIL-STD-883 (human body model)		-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1, 3, 4, 5 or 6 to pin 2.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 8 kV (contact)
MIL-STD-883; class 3B (human body model)	> 8 kV

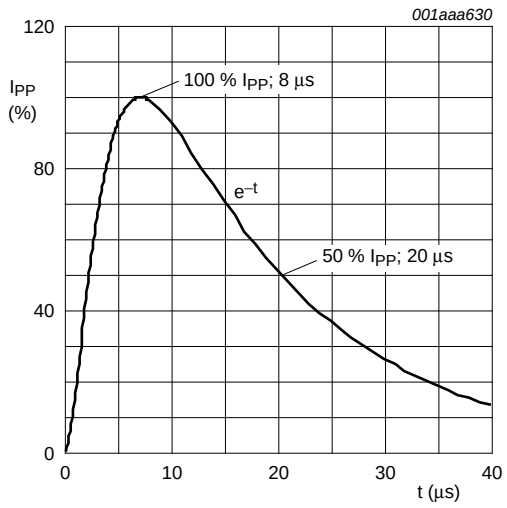


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

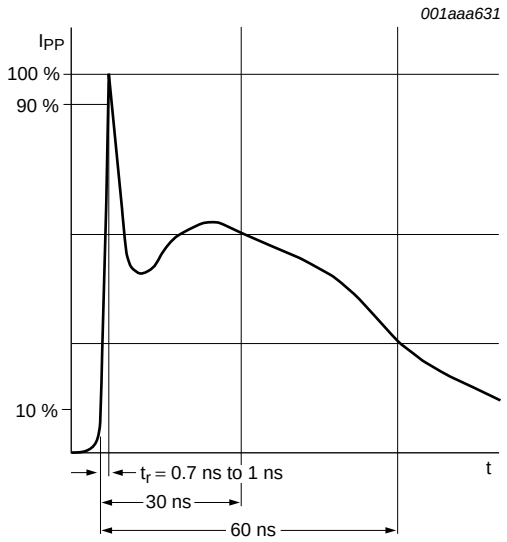


Fig 2. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 8. Characteristics

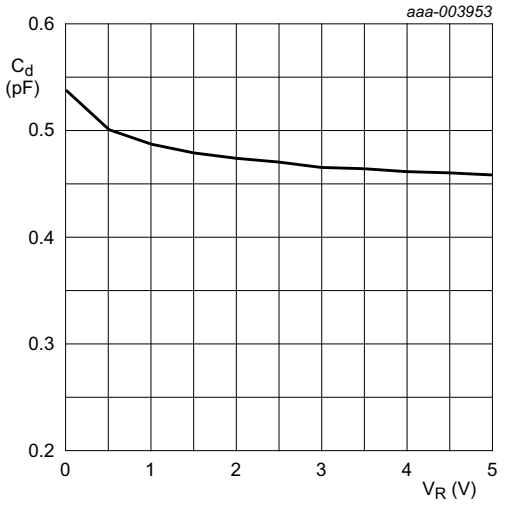
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage			-	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V		-	< 1	10	nA
V_{BR}	breakdown voltage	I_R = 10 mA		7.5	8.8	10	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	0.55	0.7	pF
V_{CL}	clamping voltage	I_{PP} = 1 A	[1][2]	-	-	13	V
		I_{PPM} = 2 A	[1][2]	-	-	15	V
r_{dyn}	dynamic resistance	I_R = 10 A	[3]	-	1.1	-	Ω

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.

[2] Measured from pin 1, 3, 4, 5 or 6 to pin 2.

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANS/IESD STM5-1-2008.



T_{amb} = 25 °C

Fig 3. Diode capacitance as a function of reverse voltage; typical values

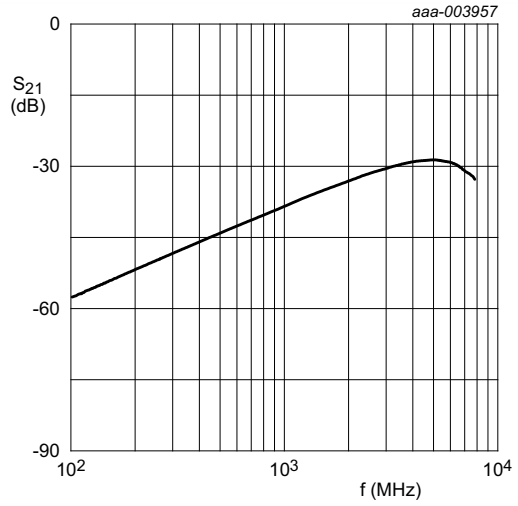


Fig 4. Crosstalk; typical values

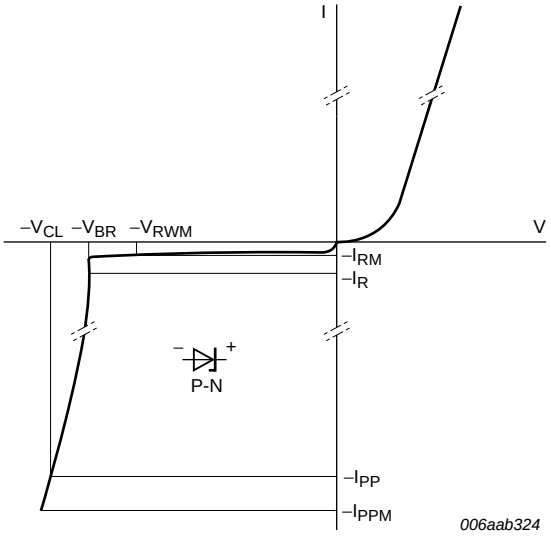


Fig 5. V-I characteristics for a unidirectional ESD protection diode

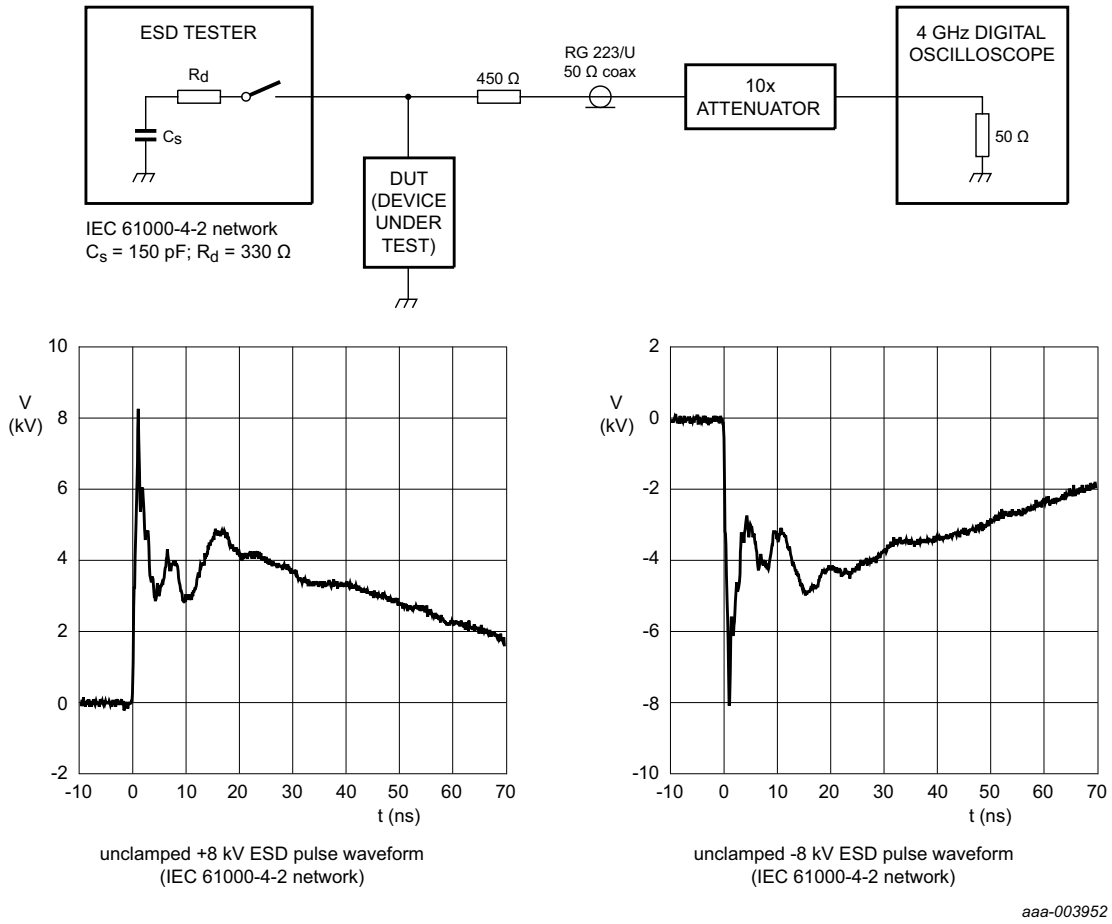


Fig 6. ESD clamping test setup

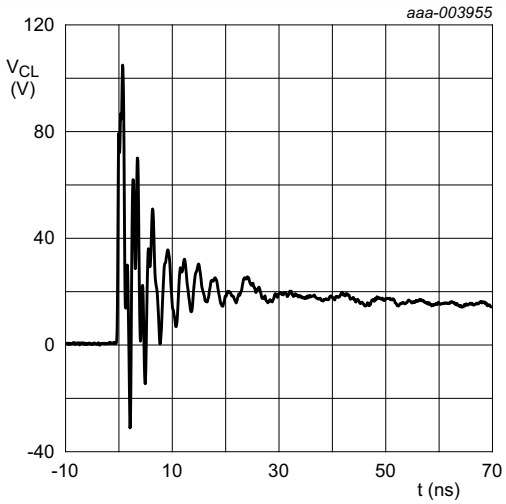


Fig 7. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

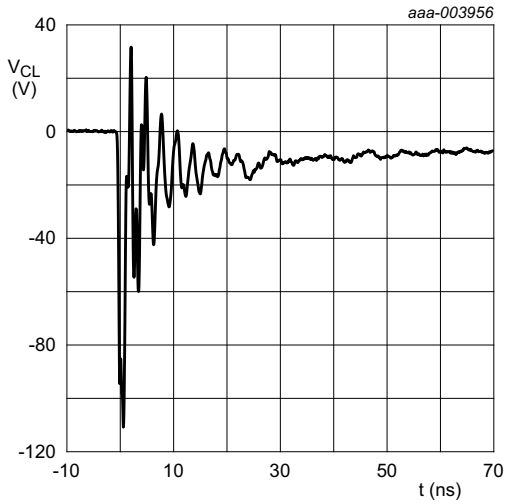


Fig 8. Clamped –8 kV pulse waveform (IEC 61000-4-2 network)

7. Application information

The device is designed for the protection of up to five unidirectional data or signal lines from surge pulses and ESD damage.

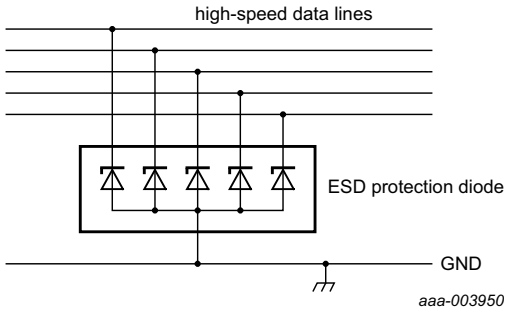


Fig 9. Typical application for unidirectional application of five lines

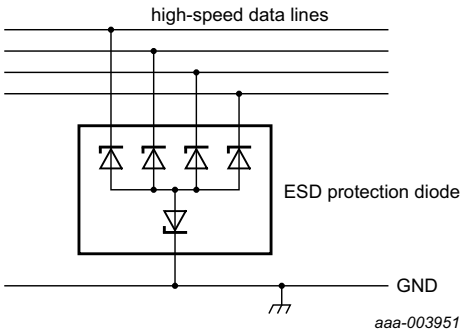


Fig 10. Typical application for bidirectional application of four lines

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

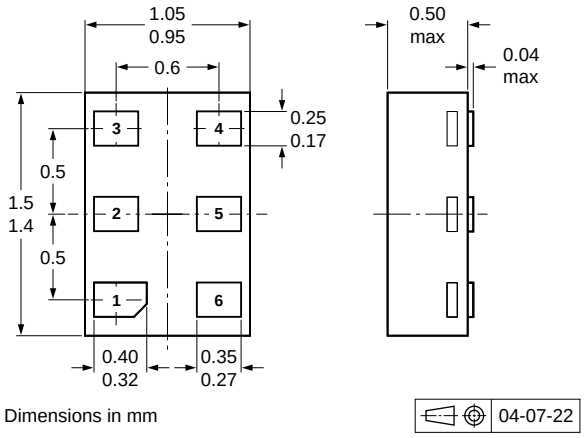


Fig 11. Package outline DFN1410-6 (SOT886)

10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description		Packing quantity
				5000
PESD5V0F5UF	DFN1410-6 (SOT886)	4 mm pitch, 8 mm tape and reel; T1	[2]	-115
		4 mm pitch, 8 mm tape and reel; T4	[3]	-132

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping.

[3] T4: 90° rotated reverse taping.

11. Soldering

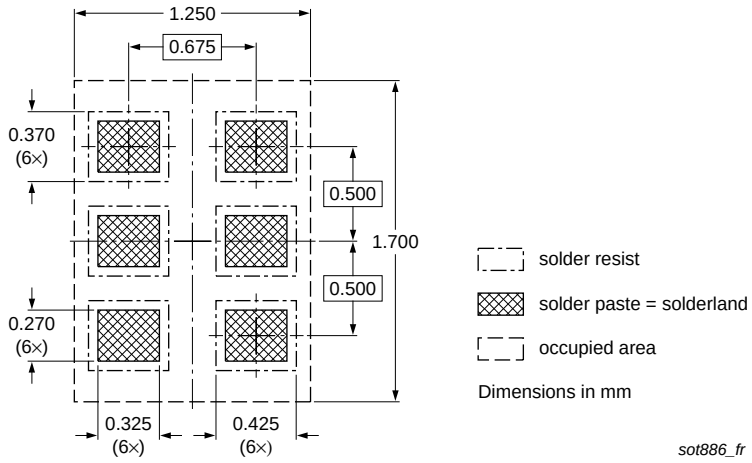


Fig 12. Reflow soldering footprint DFN1410-6 (SOT886)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0F5UF v.1	20120717	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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