# 1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the high speed TrEOS Protection family. This device is housed in a small leadless DFN1006L-2 (SOD882L) Surface-Mounted Device (SMD) laminate package, optimized for high speed communication. The device is designed to protect one automotive in-vehicle network bus line from the damage caused by ESD and other transients.

## 2. Features and benefits

- DFN1006L-2 package, optimized for protection of high speed data lines
- Extremely low insertion loss: -3 dB at 14.6 GHz
- Single line bidirectional ESD protection
- Ultra low capacitance: C<sub>d</sub> < 0.25 pF</li>
- ESD protection 15 kV (IEC 61000-4-2)
- Deep snap-back combined with dynamic resistance of 0.35 Ω
- Qualified according to AEC-Q101 and recommended for use in automotive applications

# 3. Applications

ESD protection for in-vehicle network lines in automotive environments

- Ultra high-speed data lines such as USB 3.2 or HDMI 2.0
- Low-Voltage Differential Signaling (LVDS) automotive
- Automotive Multi-Gigabit Ethernet
- Automotive A/V monitors, displays and cameras

# 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{RWM}$	reverse standoff voltage	T <sub>amb</sub> = 25 °C		-	-	5	V
I <sub>PPM</sub>	rated peak pulse current	$t_p = 8/20 \ \mu s$	[1]	-	-	6.5	Α
C <sub>d</sub>	diode capacitance	f = 1 MHz; V <sub>R</sub> = 0 V; T <sub>amb</sub> = 25 °C	[2]	-	-	0.25	pF

- [1] According to IEC 61000-4-5.
- [2] Measured from pin 1 to pin 2.



# 5. Pinning information

## **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)		
2	K2	cathode (diode 2)	Transparent top view  DFN1006L-2 (SOD882L-1)	K1 K2 sym045

# 6. Ordering information

## **Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PESD5V0H1BLL-Q		Leadless ultra small plastic package, 2 terminals, 0.65mm pitch; 1 mm x 0.6 mm x 0.45 mm body	SOD882L-1

# 7. Marking

## Table 4. Marking codes

Type number	Marking code
PESD5V0H1BLL-Q	888

# 8. Limiting values

### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I <sub>PPM</sub>	rated peak pulse current	t <sub>p</sub> = 8/20 μs	[1]	-	6.5	А
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
ESD maximu	m ratings					,
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	15	kV

- [1] According to IEC 61000-4-5.
- [2] Measured from pin 1 to pin 2.
- [3] Device stressed with ten non-repetitive ESD pulses.

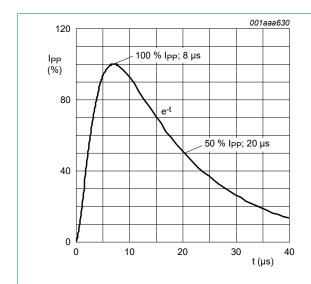


Fig. 1.  $8/20~\mu s$  pulse waveform according to IEC 61000-4-5

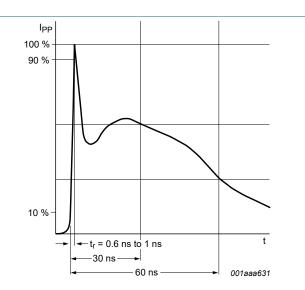


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

# 9. Characteristics

**Table 6. Characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{RWM}$	reverse standoff voltage	T <sub>amb</sub> = 25 °C		-	-	5	V
$V_{BR}$	breakdown voltage		[1]	6	10	-	V
I <sub>RM</sub>	reverse leakage current	V <sub>R</sub> = 5 V; T <sub>amb</sub> = 25 °C	[1]	-	1	50	nA
C <sub>d</sub>	diode capacitance	f = 1 MHz; V <sub>R</sub> = 0 V; T <sub>amb</sub> = 25 °C	[1]	-	-	0.25	pF
V <sub>CL</sub>	clamping voltage	$I_{PPM} = 6.5 \text{ A}; t_p = 8/20  \mu\text{s}; T_{amb} = 25 ^{\circ}\text{C}$	[1] [2]	-	5	-	V
		$I_{PP}$ = 8 A; $t_p$ = 100 ns; $T_{amb}$ = 25 °C	[3]	-	5	-	V
		$I_{PP}$ = 16 A; $t_p$ = 100 ns; $T_{amb}$ = 25 °C	[3]	-	7.5	-	V
R <sub>dyn</sub>	dynamic resistance	I <sub>R</sub> = 10 A; t <sub>p</sub> = 100 ns; T <sub>amb</sub> = 25 °C	[1] [3]	-	0.35	-	Ω

- [1] Measured from pin 1 to pin 2.
- [2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

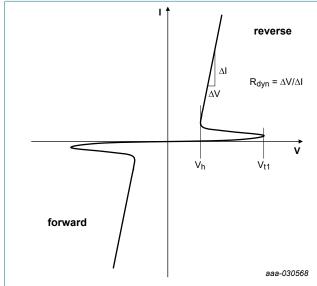


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

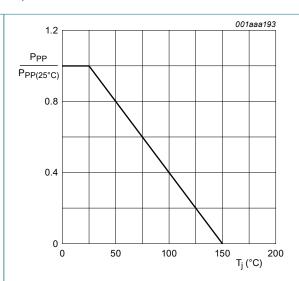


Fig. 4. Relative variation of peak pulse power as a function of junction temperature; typical values

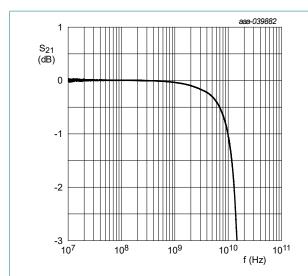
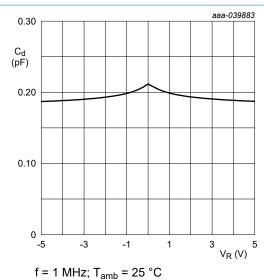
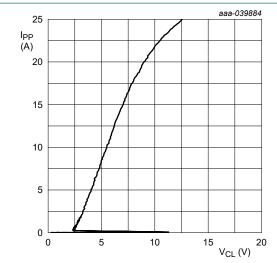


Fig. 5. Insertion loss; typical values



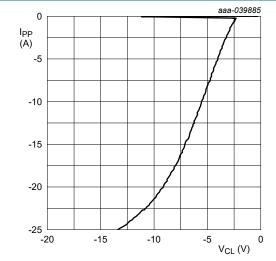
1 – 1 Wil IZ, 1 amb – 25 C

Fig. 6. Diode capacitance as a function of reverse voltage; typical values



Transmission Line Pulse (TLP);  $t_p = 100 \text{ ns}$ ;  $t_r = 1 \text{ ns}$ 

Fig. 7. Dynamic resistance with positive clamping; typical values



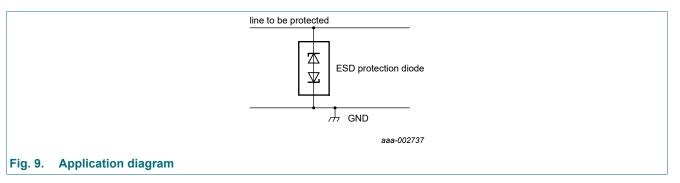
Transmission Line Pulse (TLP);  $t_p = 100 \text{ ns}$ ;  $t_r = 1 \text{ ns}$ 

Fig. 8. Dynamic resistance with negative clamping; typical values

# 10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



#### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 11. Test information

#### **Quality information**

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

# 12. Package outline

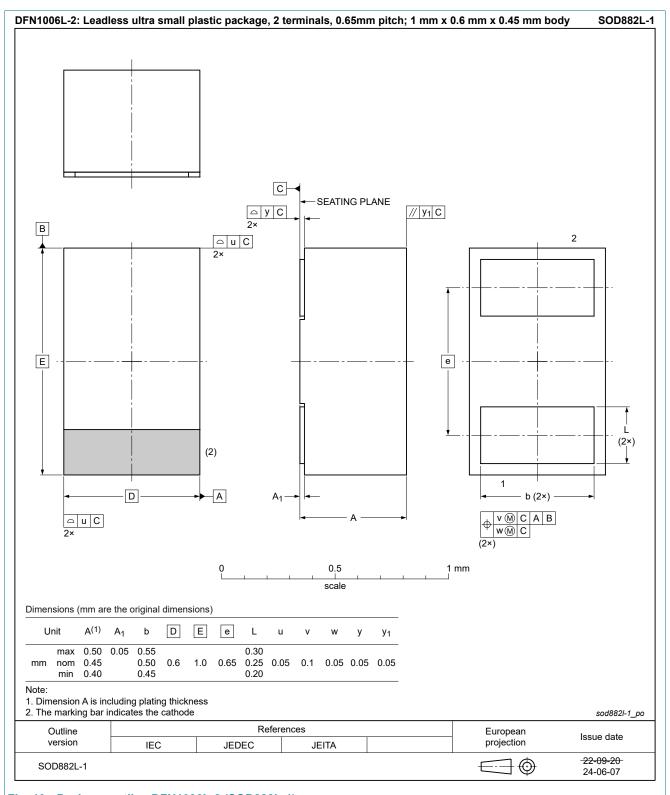
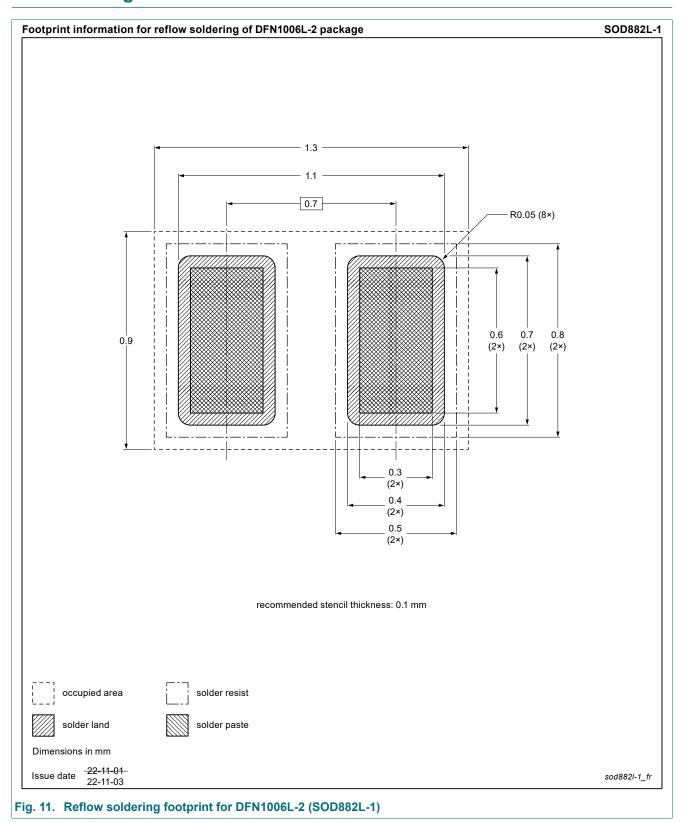


Fig. 10. Package outline DFN1006L-2 (SOD882L-1)

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# 13. Soldering



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# 14. Revision history

# Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0H1BLL-Q v.1	20240802	Product data sheet	-	-

# 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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