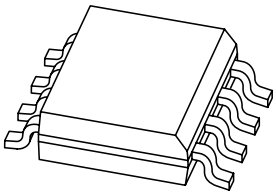
DATA SHEET



PESD5V0L7BS

Low capacitance 7-fold bi-directional ESD protection diode array in SO8 package

Product specification

2004 Mar 15

Philips
Semiconductors

Low capacitance 7-fold bi-directional ESD protection diode array in SO8 package

PESD5V0L7BS

FEATURES

- Bi-directional ESD protection of up to 7 lines
- Low diode capacitance
- Max. peak pulse power: P_{pp} = 35 W at t_p = 8/20 µs
- Low clamping voltage: $V_{(CL)R}$ = 17 V at I_{pp} = 2.5 A
- Ultra low leakage current: I_{RM} = 3 nA at V_{RWM} = 5 V
- ESD protection: >10 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5; (surge): I_{pp} = 2.5 A at t_p = 8/20 µs.

APPLICATIONS

- Computers and peripherals
- Communication systems
- Audio and video equipment
- High speed data lines
- Parallel ports.

DESCRIPTION

Low capacitance 7-fold bi-directional ESD protection diode array in a small SO8 plastic package, designed to protect up to seven transmission or data lines from ElectroStatic Discharge (ESD) damage.

MARKING

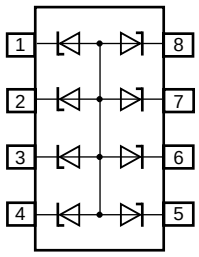
TYPE NUMBER	MARKING CODE
PESD5V0L7BS	5V0L7BS

QUICK REFERENCE DATA

SYMBOL	PARAMETER	VALUE	UNIT
V_{RWM}	reverse stand-off voltage	5	V
C_d	diode capacitance; V_R = 0 V; f = 1 MHz	8	pF
	number of protected lines	7	

PINNING

PIN	DESCRIPTION
1, 2, 3, 4, 5, 6, 7, 8	cathodes



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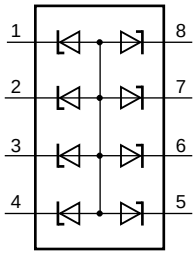


sym005

Fig.1 Simplified outline (SO8) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PESD5V0L7BS	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
P_{pp}	peak pulse power	8/20 μs pulse; note 1	–	35	W
I_{pp}	peak pulse current	8/20 μs pulse; note 1	–	2.5	A
T_{amb}	operating ambient temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–65	+150	°C

Notes

1. Non-repetitive current pulse 8/20 μs exponential decay waveform; see Fig.2.

ESD maximum ratings

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
ESD	electrostatic discharge capability	IEC 61000-4-2 (contact discharge); note 1	10	kV
		HBM MIL-Std 883	10	kV

Notes

1. Device stressed with ten non-repetitive ESD pulses; see Fig.3.

ESD standards compliance

IEC 61000-4-2, level 4 (ESD); see Fig.3	> 8 kV (contact)
HBM MIL-Std 883, class 3	> 4 kV

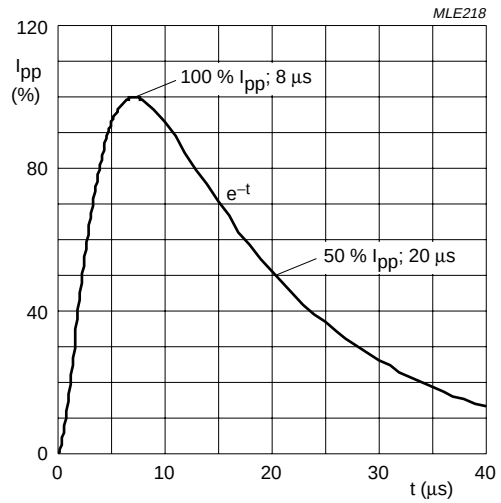


Fig.2 8/20 µs pulse waveform according to IEC 61000-4-5.

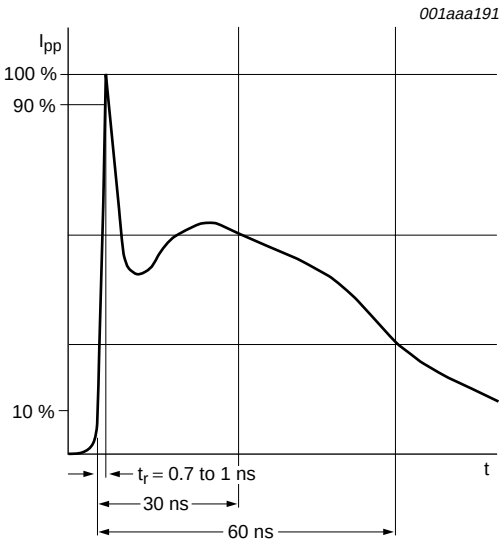


Fig.3 ElectroStatic Discharge (ESD) pulse waveform according to IEC 61000-4-2.

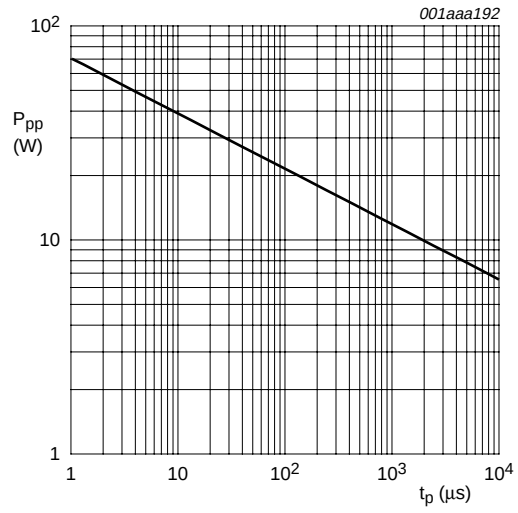
ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per diode						
V_{RWM}	reverse stand-off voltage		–	–	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V	–	3	25	nA
$V_{(CL)R}$	clamping voltage	note 1				
		I_{pp} = 1 A	–	–	11	V
		I_{pp} = 2.5 A	–	–	17	V
V_{BR}	breakdown voltage	I_R = 1 mA	7.2	7.6	7.9	V
R_{diff}	differential resistance	I_R = 1 mA	–	–	100	Ω
C_d	diode capacitance	V_R = 0 V; f = 1 MHz	–	8	10	pF

Note

1. Non-repetitive current pulse 8/20 µs exponentially decaying waveform; see Fig.2.



T_{amb} = 25 °C.
t_p = 8/20 µs exponential decay waveform; see Fig.2.

Fig.4 Peak pulse power as a function of pulse time; typical values.

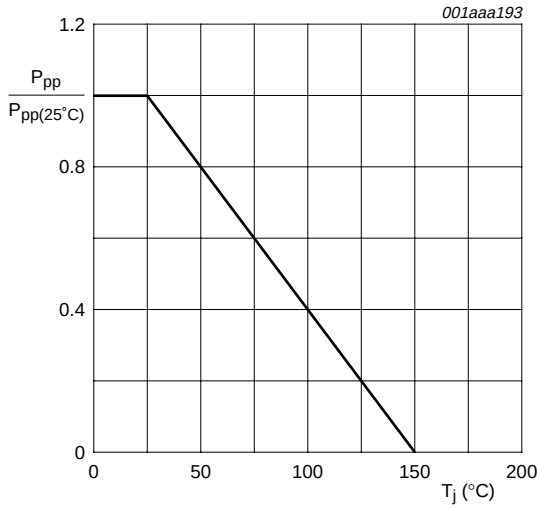
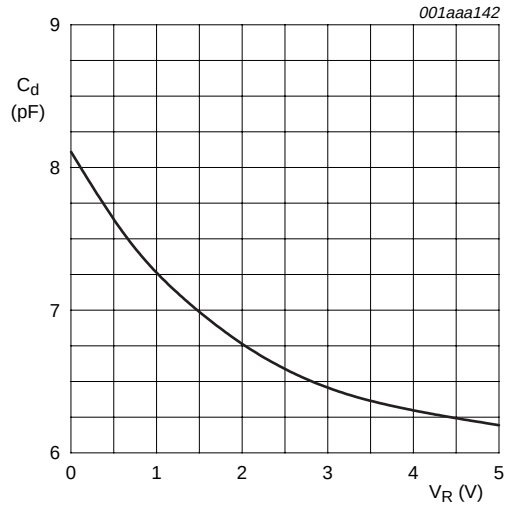


Fig.5 Relative variation of peak pulse power as a function of junction temperature; typical values.



T_{amb} = 25 °C; f = 1 MHz.

Fig.6 Diode capacitance as a function of reverse voltage; typical values.

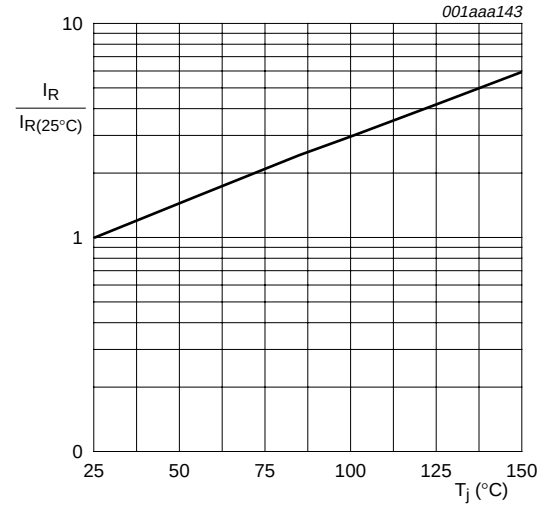
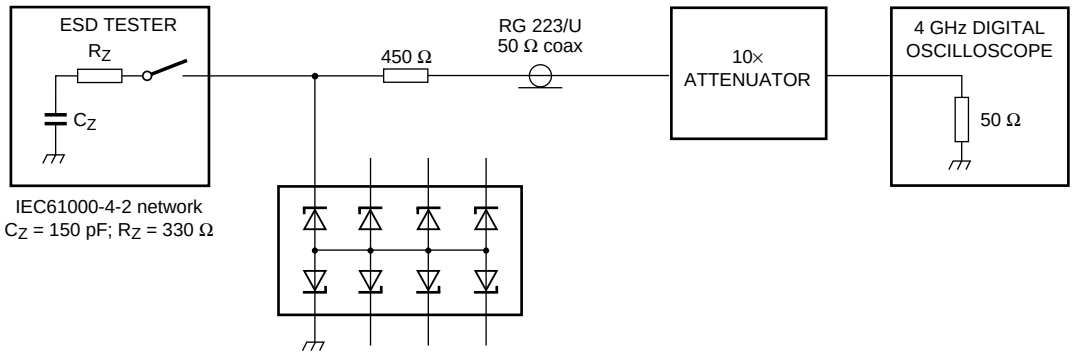
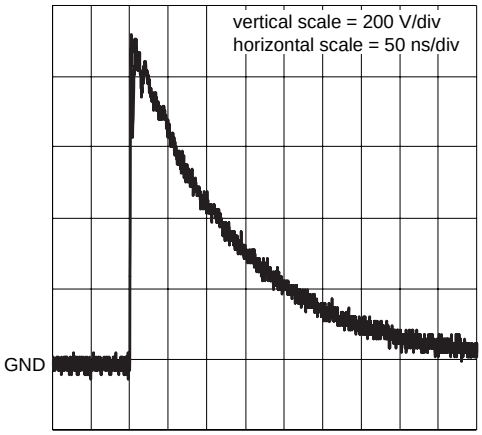


Fig.7 Relative variation of reverse leakage current as a function of junction temperature; typical values.

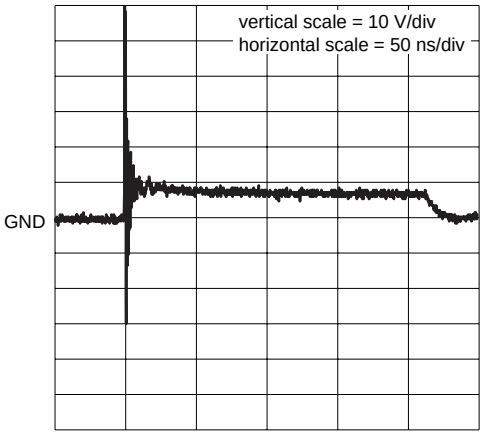


IEC61000-4-2 network
C_Z = 150 pF; R_Z = 330 Ω

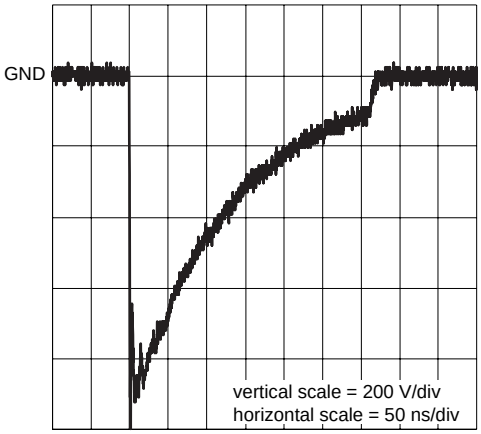
DUT: PESD5V0L7BS



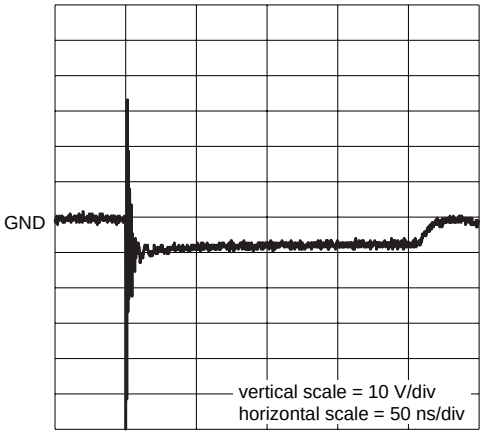
unclamped +1 kV ESD voltage waveform
(IEC61000-4-2 network)



clamped +1 kV ESD voltage waveform
(IEC61000-4-2 network)



unclamped –1 kV ESD voltage waveform
(IEC61000-4-2 network)



clamped –1 kV ESD voltage waveform
(IEC61000-4-2 network)

001aaa144

Fig.8 ESD clamping test set-up and waveforms.

APPLICATION INFORMATION

The PESD5V0L7BS can protect up to seven lines against damage caused by bi-directional ElectroStatic Discharge (ESD) and surge pulses whose polarities. The PESD5V0L7BS can be used to protect lines whose signal polarities are above and below ground. The PESD5V0L7BS provides a surge capability of 35 W (P_{pp}) per line for a 8/20 μs waveform.

Typical application

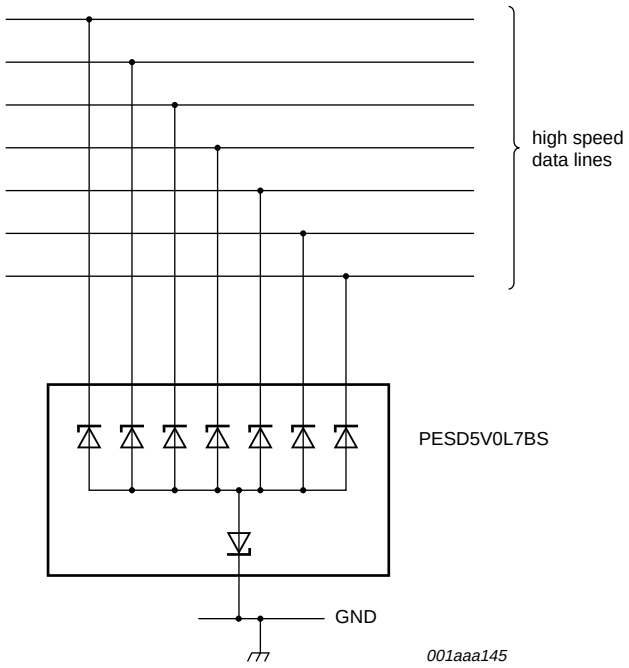


Fig.9 Typical application: bi-directional ESD protection of seven data lines.

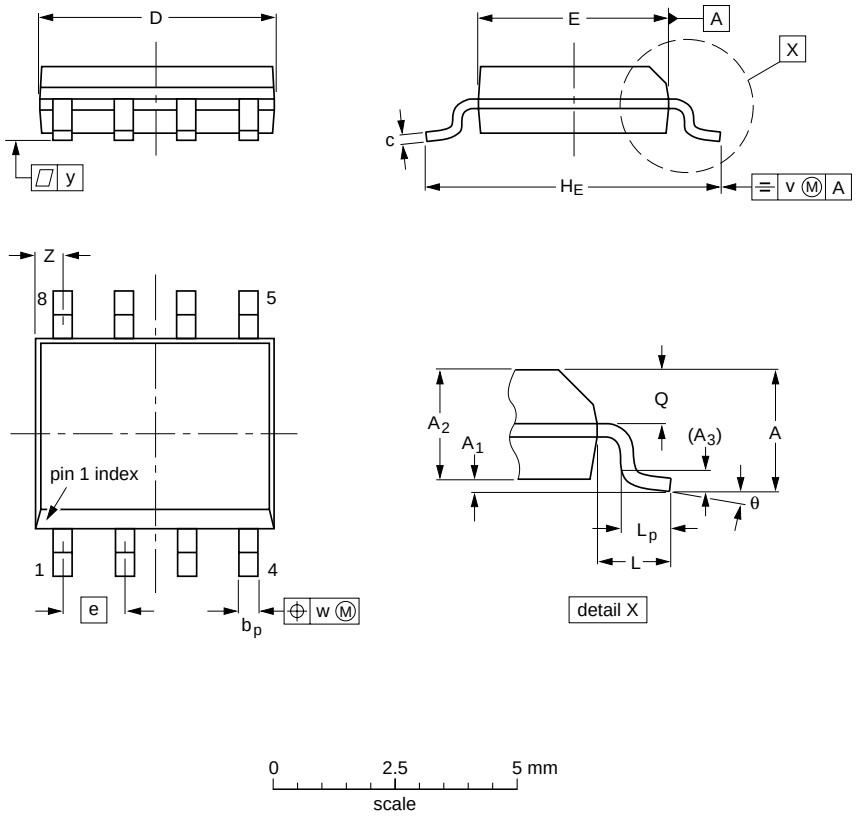
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, EFT and surge transients. The following guidelines are recommended:

- Place the PESD5V0L7BS as close as possible to the input terminal or connector
- Minimize the path length between the PESD5V0L7BS and the protected line
- Keep parallel signal paths to a minimum
- Avoid running protected conductors in parallel with unprotected conductors
- Minimize all printed-circuit board conductive loops including power and group loops
- Minimize the length of transient return paths to ground
- Avoid using shared return paths to a common ground point
- Ground planes should be used whenever possible.
- Use vias for multi-layer printed-circuit boards.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

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SCA76

Printed in The Netherlands R76/01/pp10 Date of release: 2004 Mar 15 Document order number: 9397 750 12249

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