

Ultra low capacitance bidirectional double ESD protection

Rev. 1 — 13 March 2012

Product data sheet

Product profile

1.1 General description

Ultra low capacitance bidirectional double ElectroStatic Discharge (ESD) protection array designed to protect up to two signal lines from the damage caused by ESD and other transients. The device is housed in a leadless ultra small SOT883B (DFN1006B-3) Surface-Mounted Device (SMD) plastic package.

1.2 Features and benefits

- ESD protection of up to two lines
- Ultra low diode capacitance C_d = 2.9 pF ESD protection up to 10 kV
- Ultra low leakage current I_{RM} = 5 nA
- AEC-Q101 qualified

 - IEC 61000-4-2; level 4 (ESD)

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- SIM card protection
- FireWire
- High-speed data lines

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage		-	-	5	V
C _d	diode capacitance	$f = 1 MHz; V_R = 0 V$	-	2.9	3.5	pF



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode		
2	cathode	1 3	1
3	common cathode	23	2 1 3
		Transparent top view	006aab331

3. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PESD5V0U2BMB	DFN1006B-3	leadless ultra small plastic package; 3 solder lands; body 1.0 \times 0.6 \times 0.37 mm	SOT883B			

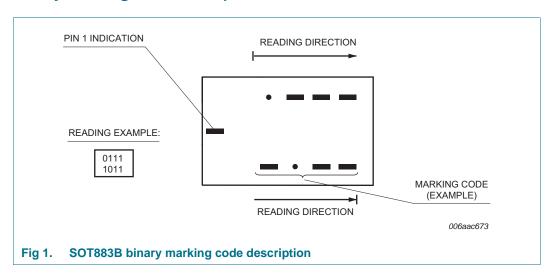
4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PESD5V0U2BMB	0001 1010

[1] For SOT883B binary marking code description, see Figure 1.

4.1 Binary marking code description



5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
I _{PPM}	rated peak pulse current	$t_p = 8/20 \ \mu s$	[1][2]	1.5	Α
Per device					
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		–55	+150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] Device stressed with ten non-repetitive current pulses (8/20 μ s exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).

Table 6. ESD maximum ratings

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode	9				
- LOD	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	<u>[1][2]</u> _	10	kV
		machine model	[2] -	400	V
		MIL-STD-883 (human body model)	-	8	kV

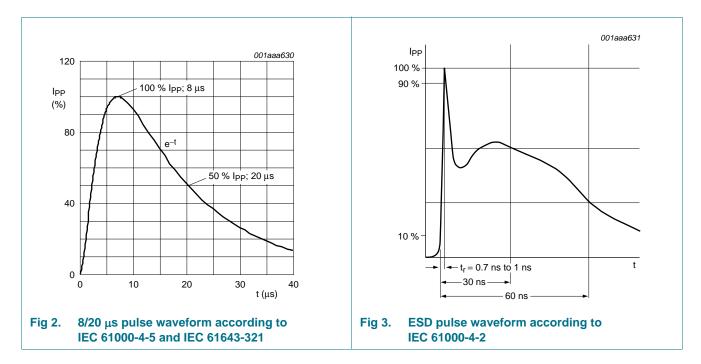
^[1] Device stressed with ten non-repetitive ESD pulses.

Table 7. ESD standards compliance

Conditions
> 8 kV (contact)
> 8 kV

^[2] Measured from pin 1 or 2 to 3.

^[2] Measured from pin 1 or 2 to 3.



6. Characteristics

Table 8. Characteristics

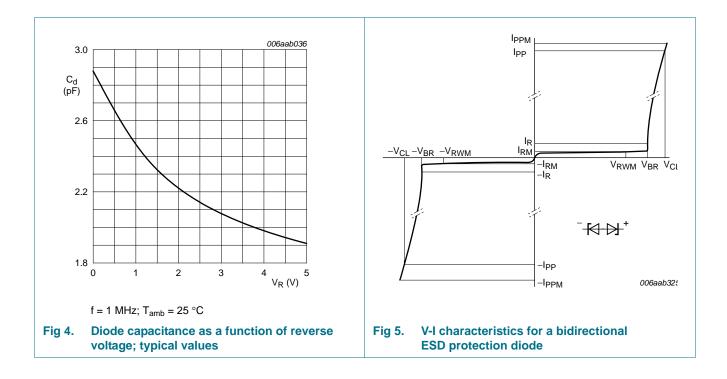
 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per diod	е						
V_{RWM}	reverse standoff voltage			-	-	5	V
I _{RM}	reverse leakage current	$V_{RWM} = 5 V$		-	5	100	nA
V_{BR}	breakdown voltage	$I_R = 5 \text{ mA}$		5.5	6.5	9.5	V
C_{d}	diode capacitance	$f = 1 MHz; V_R = 0 V$		-	2.9	3.5	pF
		f = 1 MHz; V _R = 5 V		-	1.9	-	pF
V _{CL}	clamping voltage		[1][2]				
		I _{PP} = 1 A		-	-	10	V
		I _{PPM} = 1.5 A		-	-	12	V
r _{dyn}	dynamic resistance	I _R = 10 A	[3]	-	0.6	-	Ω

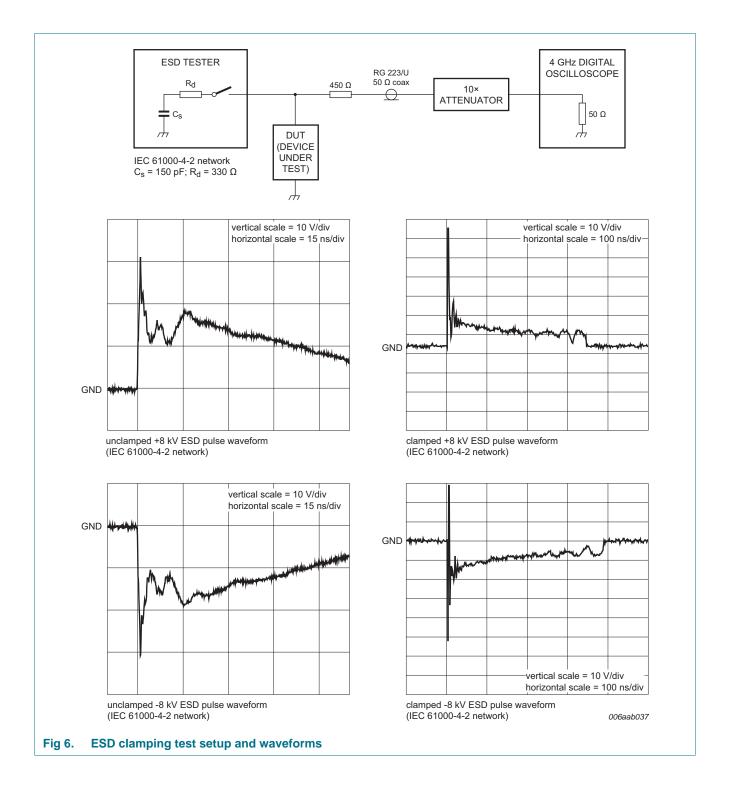
^[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.

^[2] Measured from pin 1 or 2 to 3.

^[3] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANS/IESD STM5-1-2008.

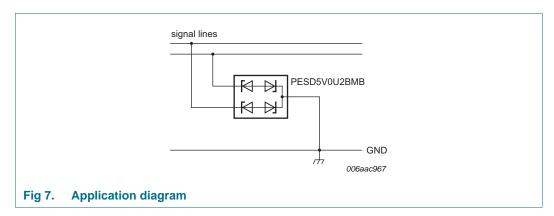


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7. Application information

The device is designed for the protection of up to two bidirectional data or signal lines from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

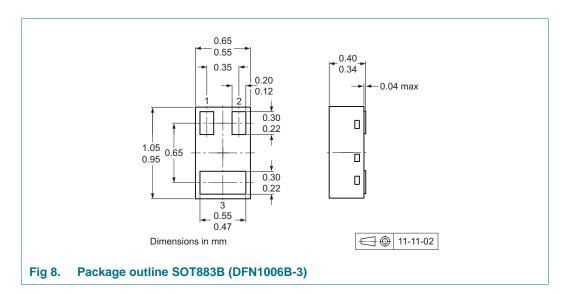
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

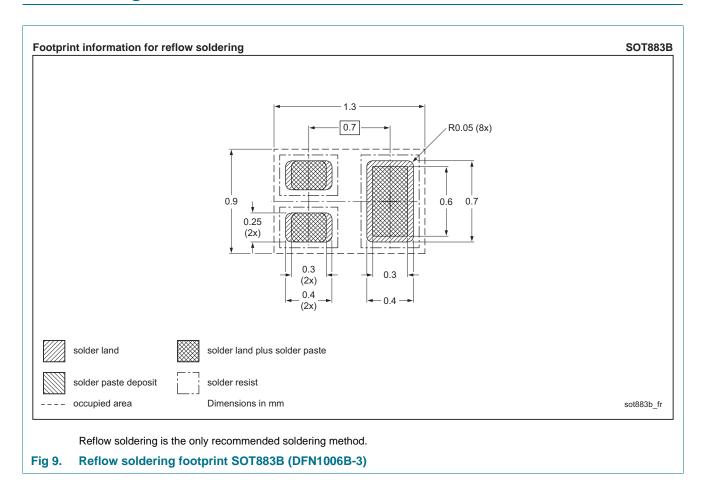
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity
			10000
PESD5V0U2BMB	SOT883B	2 mm pitch, 8 mm tape and reel	-315

[1] For further information and the availability of packing methods, see Section 14.

11. Soldering





12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U2BMB v.1	20120313	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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