PESD5V0U4BF; PESD5V0U4BW

Ultra low capacitance bidirectional quadruple ESD protection arrays

Rev. 01 — 15 August 2008 Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance bidirectional quadruple ElectroStatic Discharge (ESD) protection arrays in ultra small Surface-Mounted Device (SMD) plastic packages designed to protect up to four signal lines from the damage caused by ESD and other transients.

Table 1. Product overview

Type number	Package		Package configuration
	NXP	JEDEC	
PESD5V0U4BF	SOT886	MO-252	leadless ultra small
PESD5V0U4BW	SOT665	-	ultra small and flat lead

1.2 Features

- Bidirectional ESD protection of up to four lines
- Ultra low diode capacitance: C_d = 2.9 pF
- Ultra low leakage current: I_{RM} = 5 nA
- ESD protection up to 10 kV
- IEC 61000-4-2; level 4 (ESD)
- AEC-Q101 qualified

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection
- FireWire
- High-speed data lines

1.4 Quick reference data

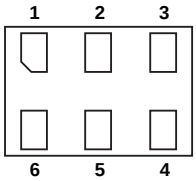
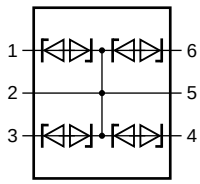
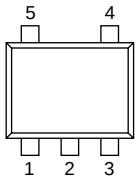
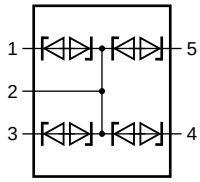
Table 2. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	-	2.9	3.5	pF

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
PESD5V0U4BF			
1	cathode (diode 1)	 bottom view	 006aab333
2	common cathode		
3	cathode (diode 2)		
4	cathode (diode 3)		
5	common cathode		
6	cathode (diode 4)		
PESD5V0U4BW			
1	cathode (diode 1)		 006aab334
2	common cathode		
3	cathode (diode 2)		
4	cathode (diode 3)		
5	cathode (diode 4)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U4BF	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
PESD5V0U4BW	-	plastic surface-mounted package; 5 leads	SOT665

4. Marking

Table 5. Marking codes

Type number	Marking code
PESD5V0U4BF	B1
PESD5V0U4BW	A6

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		–55	+150	°C
T_{stg}	storage temperature		–65	+150	°C

Table 7. ESD maximum ratings

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
Per diode						
V_{ESD}	electrostatic discharge voltage		[1]			
	PESD5V0U4BF	IEC 61000-4-2 (contact discharge)	[2]	-	10	kV
	PESD5V0U4BW	IEC 61000-4-2 (contact discharge)	[3]	-	10	kV
	PESD5V0U4BF	MIL-STD-883 (human body model)	[2]	-	8	kV
	PESD5V0U4BW	MIL-STD-883 (human body model)	[3]	-	8	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1, 3, 4 or 6 to pin 2 or 5.

[3] Measured from pin 1, 3, 4 or 5 to pin 2.

Table 8. ESD standards compliance

Standard	Conditions
Per diode	
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

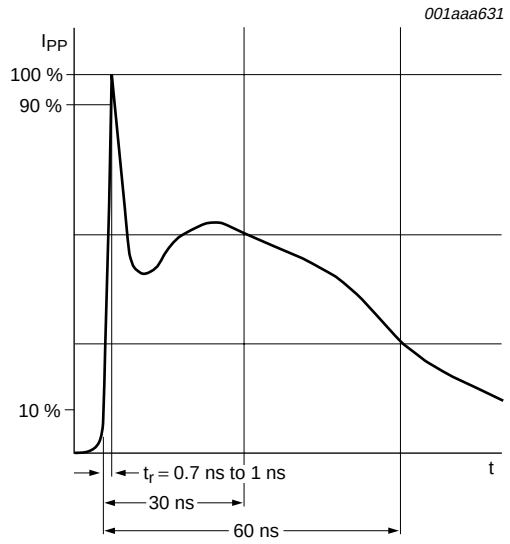


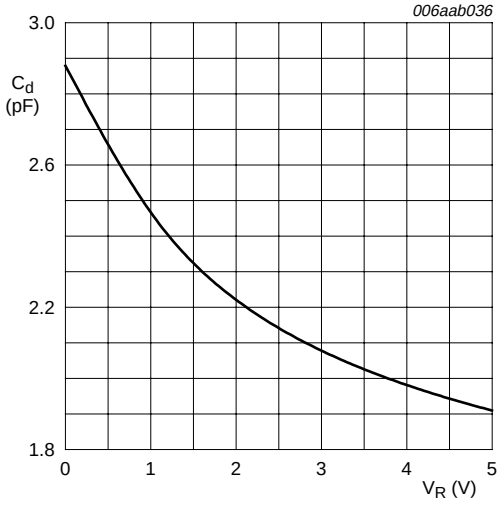
Fig 1. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 9. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage		-	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V	-	5	100	nA
V_{BR}	breakdown voltage	I_R = 5 mA	5.5	6.5	9.5	V
C_d	diode capacitance	f = 1 MHz				
		V_R = 0 V	-	2.9	3.5	pF
		V_R = 5 V	-	1.9	-	pF
r_{dif}	differential resistance	I_R = 1 mA	-	-	100	Ω



f = 1 MHz; T_{amb} = 25 °C

Fig 2. Diode capacitance as a function of reverse voltage; typical values

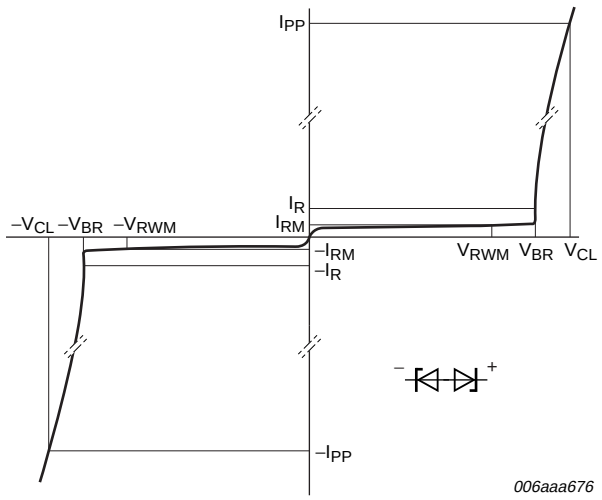


Fig 3. V-I characteristics for a bidirectional ESD protection diode

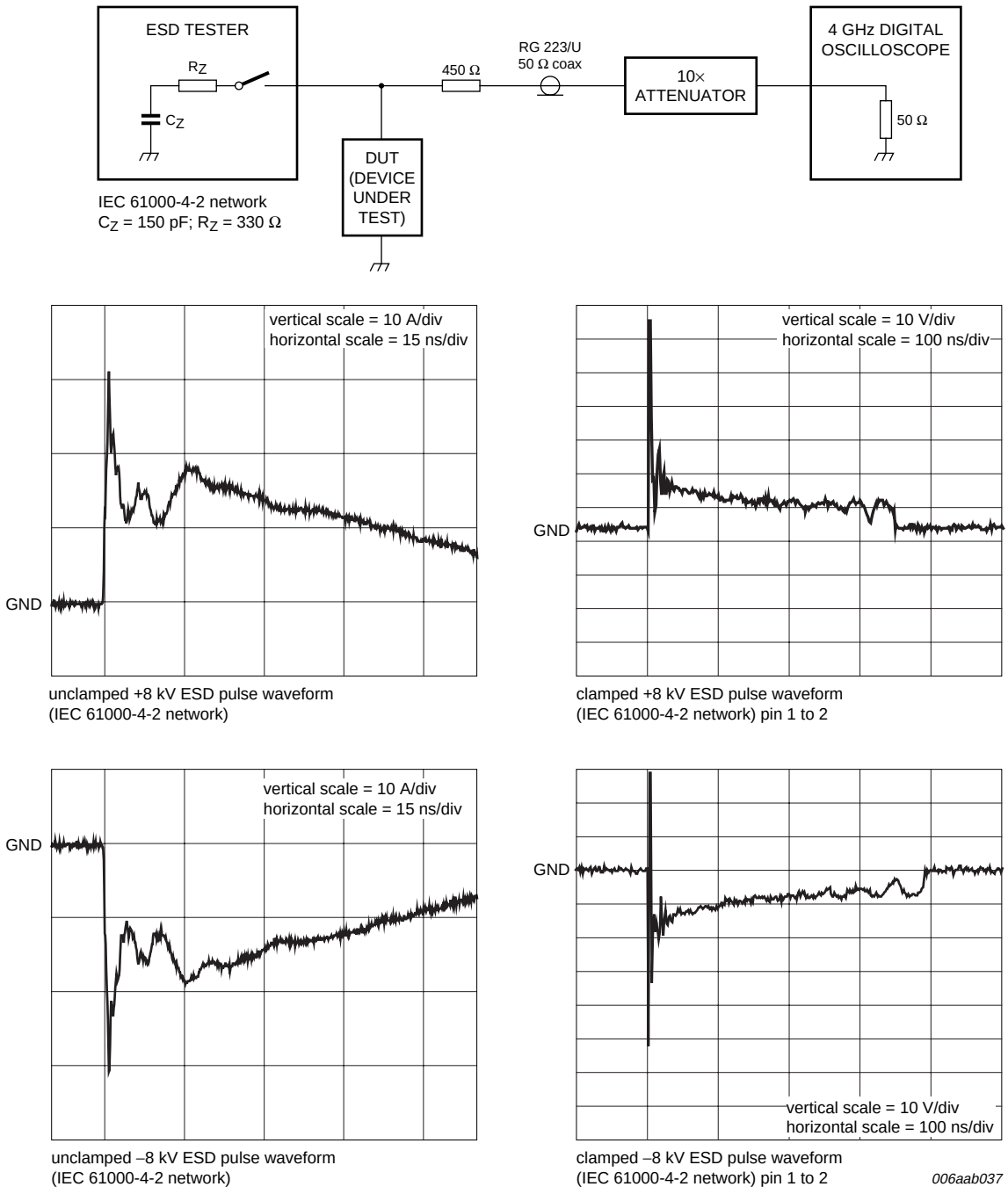


Fig 4. ESD clamping test setup and waveforms

7. Application information

The PESD5V0U4BF and the PESD5V0U4BW are designed for the protection of up to four bidirectional data or signal lines from the damage caused by ESD and surge pulses. The devices may be used on lines where the signal polarities are both, positive and negative with respect to ground.

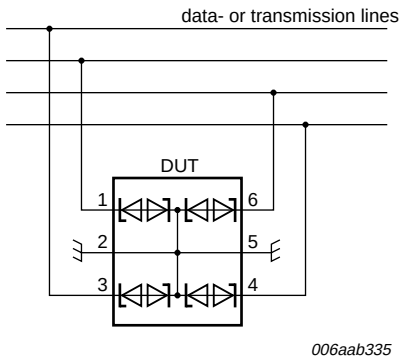


Fig 5. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

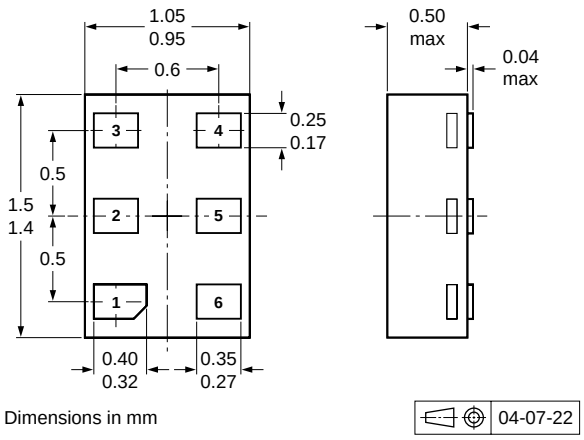


Fig 6. Package outline PESD5V0U4BF (SOT886)

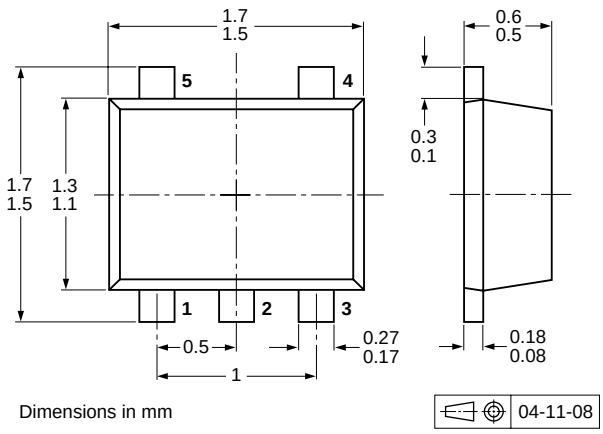


Fig 7. Package outline PESD5V0U4BW (SOT665)

10. Packing information

Table 10. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

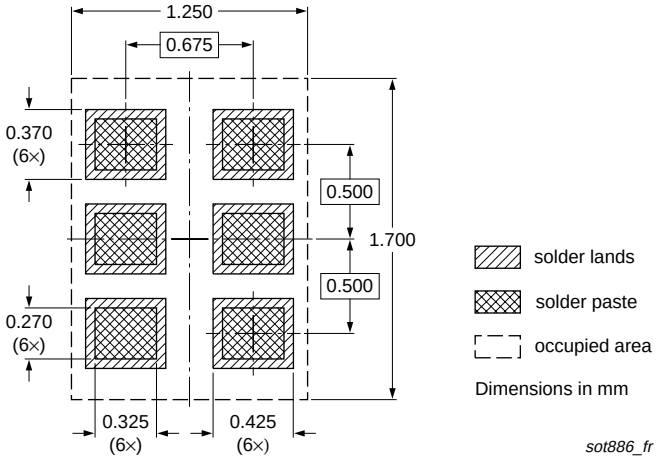
Type number	Package	Description		Packing quantity		
				4000	5000	8000
PESD5V0U4BF	SOT886	4 mm pitch, 8 mm tape and reel; T1	[2]	-	-115	-
		4 mm pitch, 8 mm tape and reel; T4	[3]	-	-132	-
PESD5V0U4BW	SOT665	2 mm pitch, 8 mm tape and reel		-	-	-315
		4 mm pitch, 8 mm tape and reel		-115	-	-

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

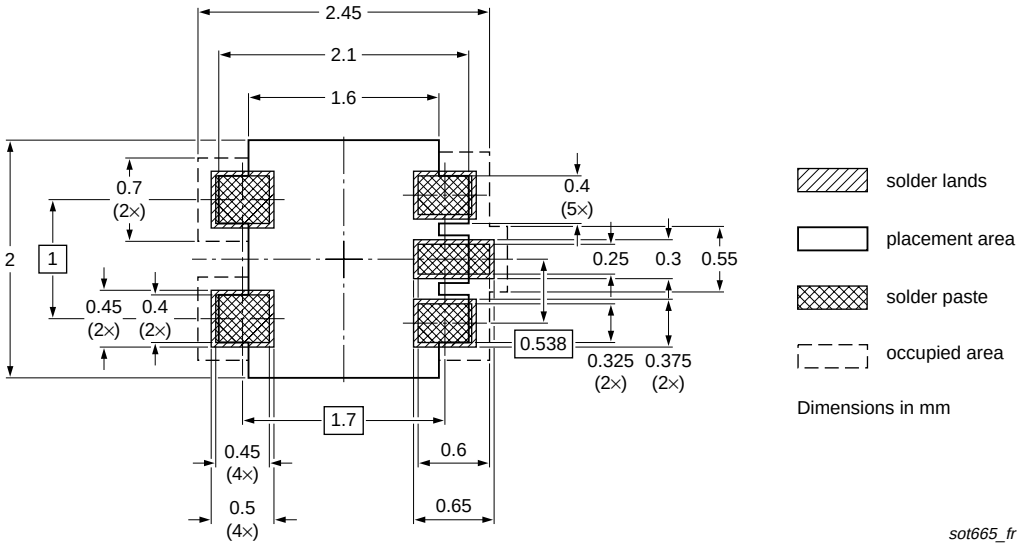
[3] T4: 90° rotated reverse taping

11. Soldering



Reflow soldering is the only recommended soldering method.

Fig 8. Reflow soldering footprint PESD5V0U4BF (SOT886)



Reflow soldering is the only recommended soldering method.

Fig 9. Reflow soldering footprint PESD5V0U4BW (SOT665)

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U4BF_PESD5V0U4BW_1	20080815	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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