PESD5V0X2UAM

Ultra low capacitance unidirectional double ESD protection diode

10 April 2014 **Product data sheet**

1. General description

Ultra low capacitance unidirectional double ElectroStatic Discharge (ESD) protection diode in a DFN1006-3 (SOT883) leadless ultra small Surface-Mounted Device (SMD) plastic package designed to protect up to two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Ultra low diode capacitance: C_d = 0.80 pF
- ESD protection up to 15 kV; IEC61000-4-2
- I_{PPM} = 2.5 A; IEC 61643-321 (surge)
- AEC-Q101 qualified

3. Applications

- High-speed data lines
- Portable electronics
- Communication systems
- Computers and peripherals

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	[1]	-	0.8	0.95	pF
V_{RWM}	reverse standoff voltage			-	-	5	V

[1] Measured from pin 1 or 2 to 3.

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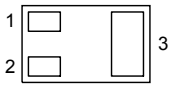
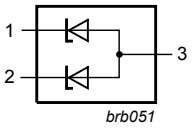
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DFN1006-3 (SOT883)**	
2	K2	cathode (diode 2)		
3	A	common anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0X2UAM	DFN1006-3	DFN1006-3: leadless ultra small plastic package; 3 solder lands	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0X2UAM	ZJ

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per diode						
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1][2]	-	2.5	A
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			-55	150	°C
T_{amb}	ambient temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[3][2]	-	15	kV
		IEC 61000-4-2 (air discharge)	[3][2]	-	15	kV
		machine model	[2]	-	400	V
		MIL-STD-883 (human body model)		-	10	kV

[1] According to IEC 61000-4-5 and IEC 61643-321.
[2] Measured from pin 1 or 2 to 3.
[3] Device stressed with ten non-repetitive ESD pulses.

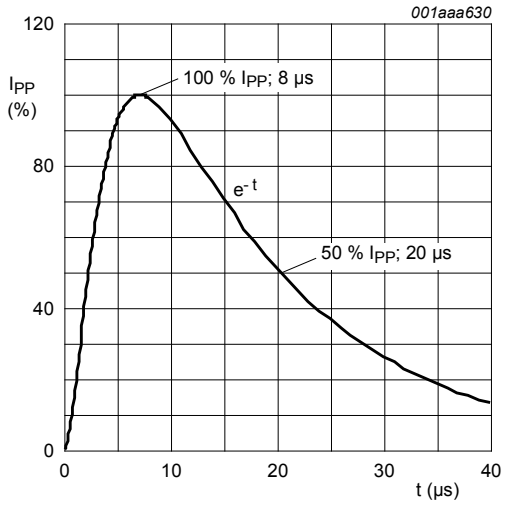

Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

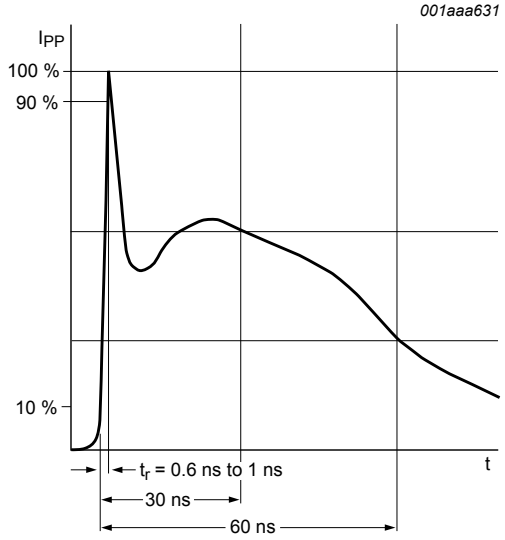

Fig. 2. ESD pulse waveform according to IEC 61000-4-2

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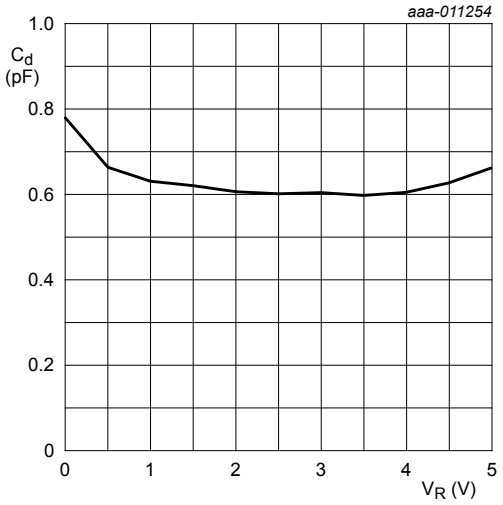
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse standoff voltage			-	-	5	V
I_{RM}	reverse leakage current	V_R = 5 V	[1]	-	1	10	nA
V_{CL}	clamping voltage	I_{PP} = 1 A; t_p = 8/20 µs	[2][1]	-	-	13	V
		I_{PP} = 2.5 A; t_p = 8/20 µs	[2][1]	-	-	14	V
V_{BR}	breakdown voltage	I_R = 10 mA	[1]	7.5	8.8	10	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	[1]	-	0.8	0.95	pF
R_{dyn}	dynamic resistance	I_R = 10 A	[3][1]	-	0.65	-	Ω

[1] Measured from pin 1 or 2 to 3.
[2] According to IEC 61000-4-5 and IEC 61643-321.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.



f = 1 MHz; T_{amb} = 25 °C

Fig. 3. Diode capacitance as a function of reverse voltage; typical values

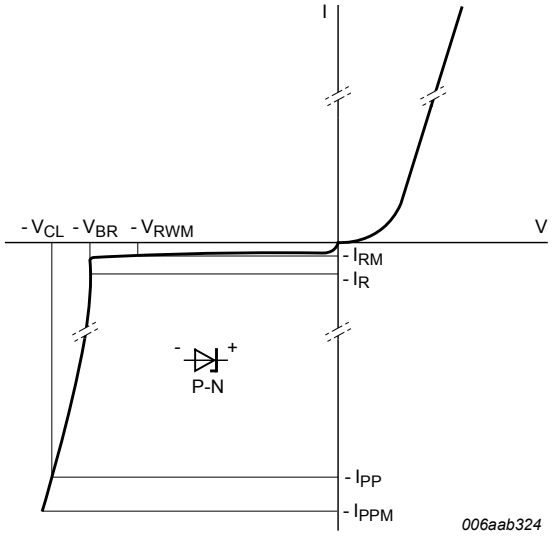


Fig. 4. V-I characteristics for a unidirectional ESD protection diode

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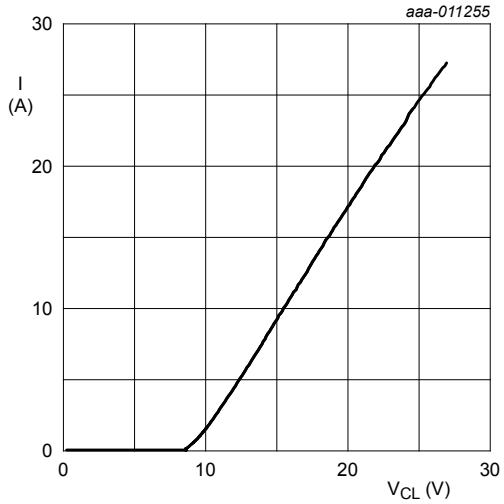

t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 5. Dynamic resistance

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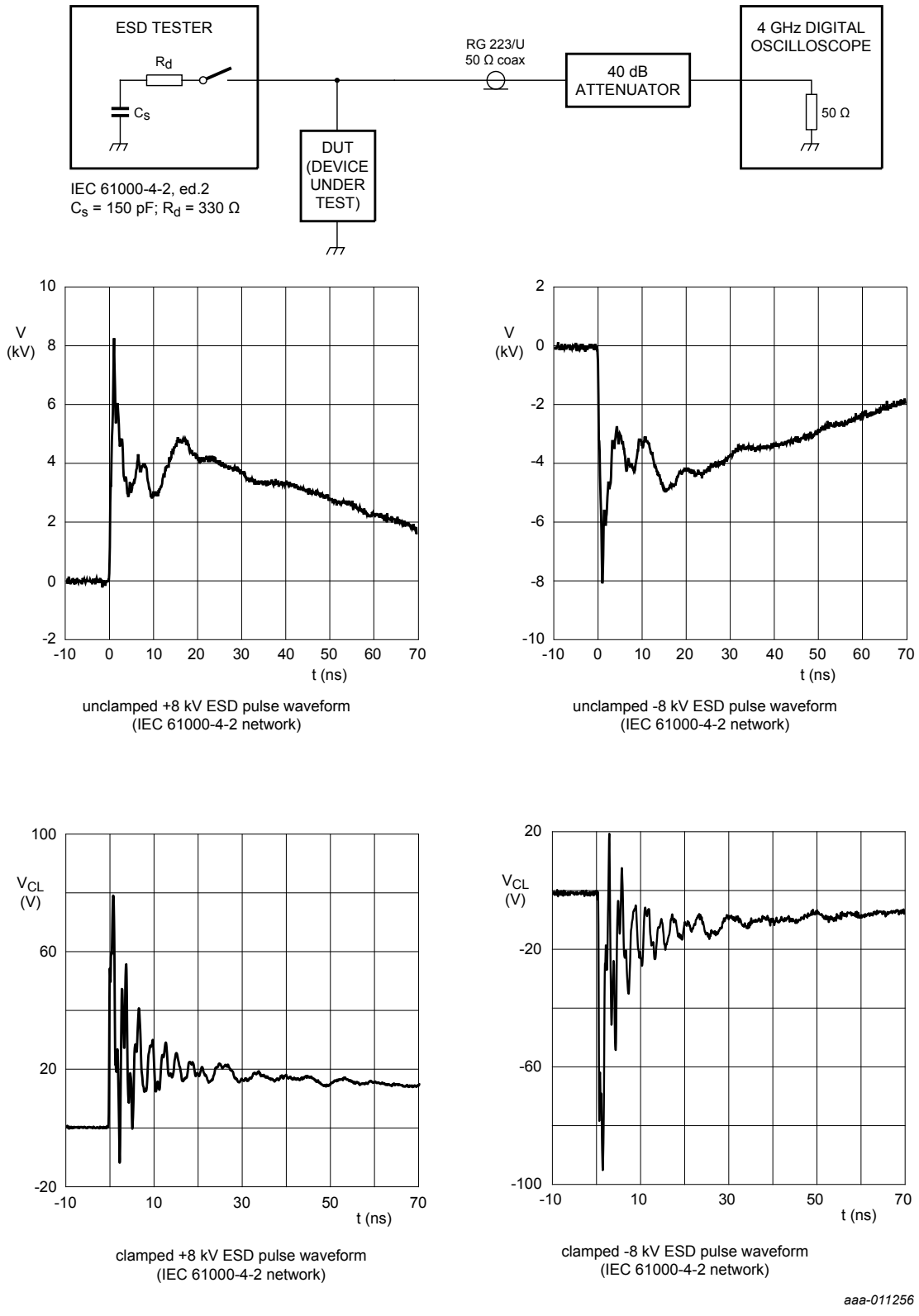

Fig. 6. ESD clamping test setup and waveforms

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10. Test information

10.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

11. Application information

The device is designed for the protection of up to two unidirectional data lines from surge pulses and ESD damage.

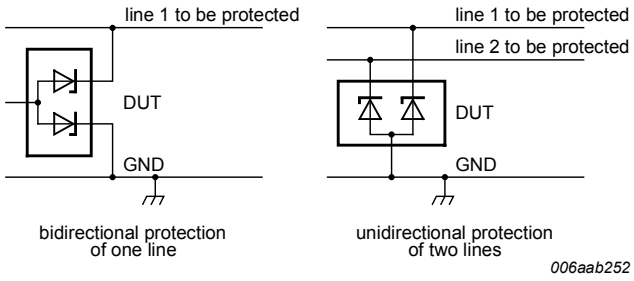

Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

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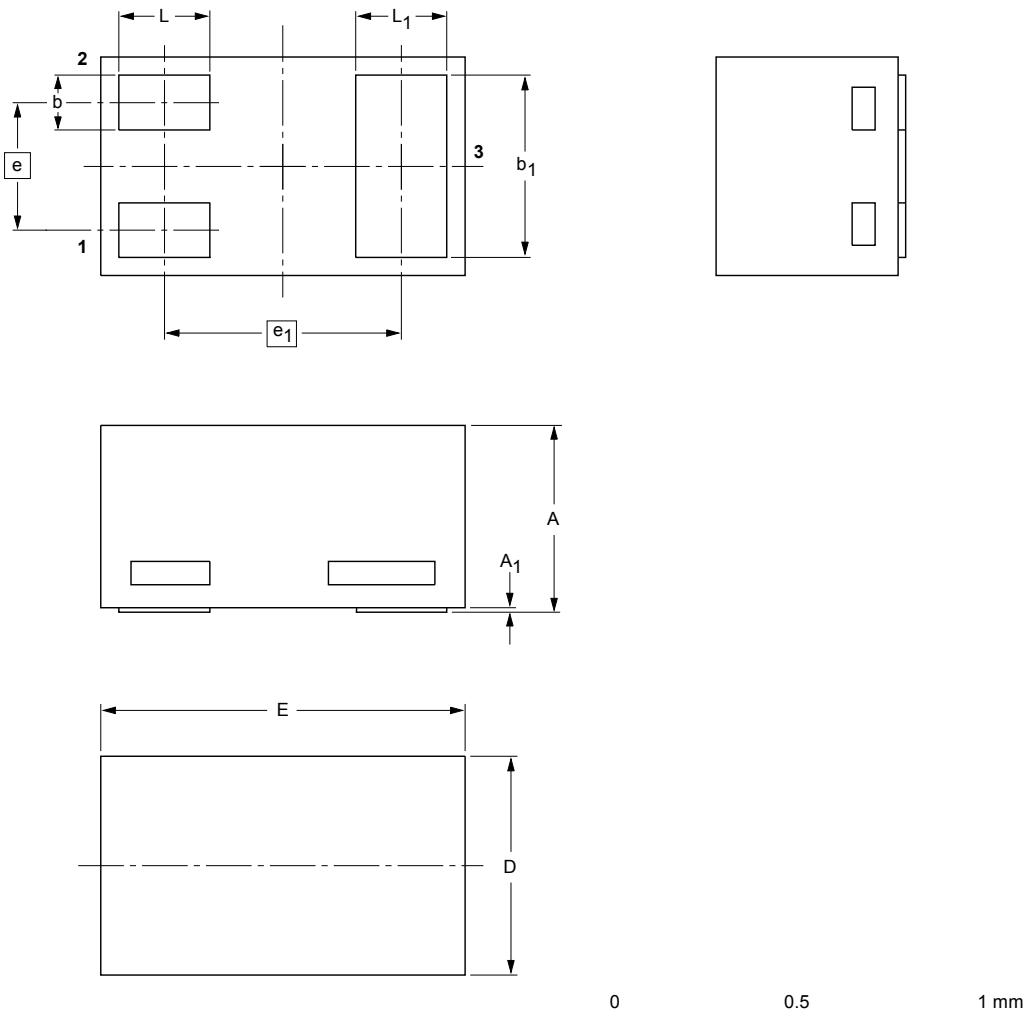
12. Package outline

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm **SOT883**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1)	A_1 max.	b	b_1	D	E	e	e_1	L	L_1
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			~~03-02-05~~ 03-04-03

Fig. 8. Package outline DFN1006-3 (SOT883)

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13. Soldering

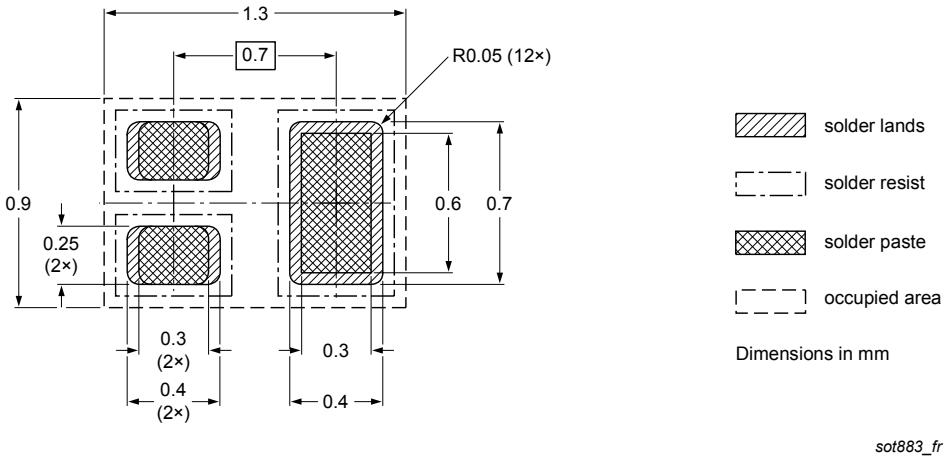

Fig. 9. Reflow soldering footprint for DFN1006-3 (SOT883)

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14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0X2UAM v.1	20140410	Product data sheet	-	-

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15. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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