



PESD5V5C1BBSF-Q

Extremely low capacitance bidirectional ESD protection diode

16 July 2025

Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- $V_{RWM} = 5.5$ V device
- IEC 61000-4-5 (surge): $I_{PPM} = 8.1$ A
- Extremely low diode capacitance $C_d = 0.26$ pF typical
- Extremely low clamping voltage to protect sensitive I/Os
- Very low peak clamping for sensitive IC with low-inductance traces between protection and protected system
- Extremely low-inductance protection path to ground
- ESD protection up to ± 15 kV according to IEC 61000-4-2
- Very low trigger voltage $V_{t1} = 7.9$ V to protect against low-voltage surge pulses
- Ultra-small SMD package
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Automotive Low-Voltage Differential Signaling (LVDS)
- Automotive Multigigabit Ethernet
- SERDES lines
- Automotive A/V monitors, displays and cameras
- USB4 and Thunderbolt 4 data lines

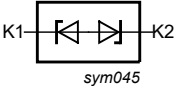
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-5.5	-	5.5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	-	0.26	0.31	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view DSN0603-2 (SOD962-2)	 <i>sym045</i>
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V5C1BBSF-Q	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V5C1BBSF-Q	5D

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{RWM}	reverse standoff voltage			-5.5	5.5	V
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1]	-8.1	8.1	A
T _{amb}	ambient temperature			-40	125	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-15	15	kV
		IEC 61000-4-2; air discharge	[2]	-15	15	kV

- [1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
- [2] Device stressed with ten non-repetitive ESD pulses.

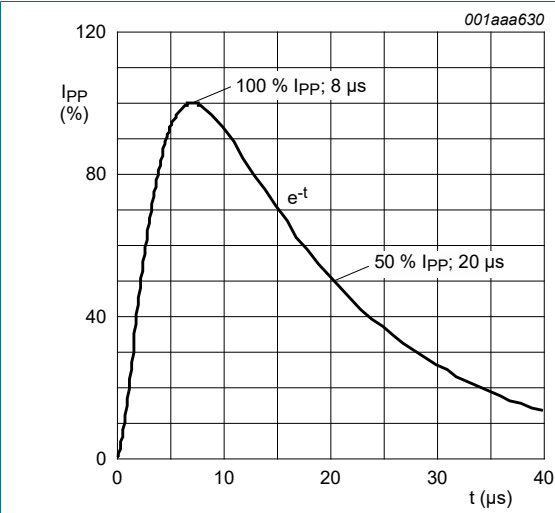


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

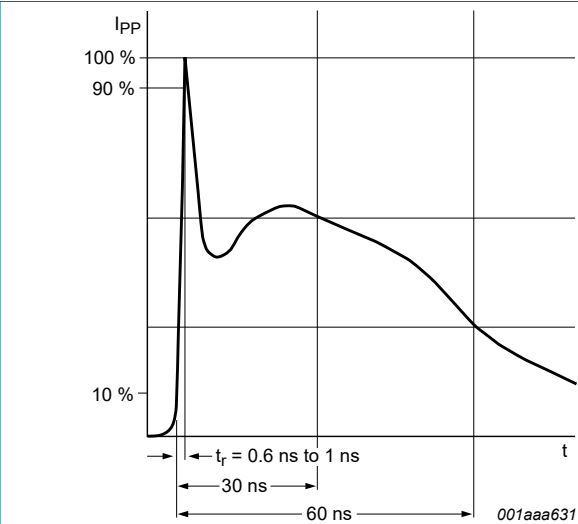


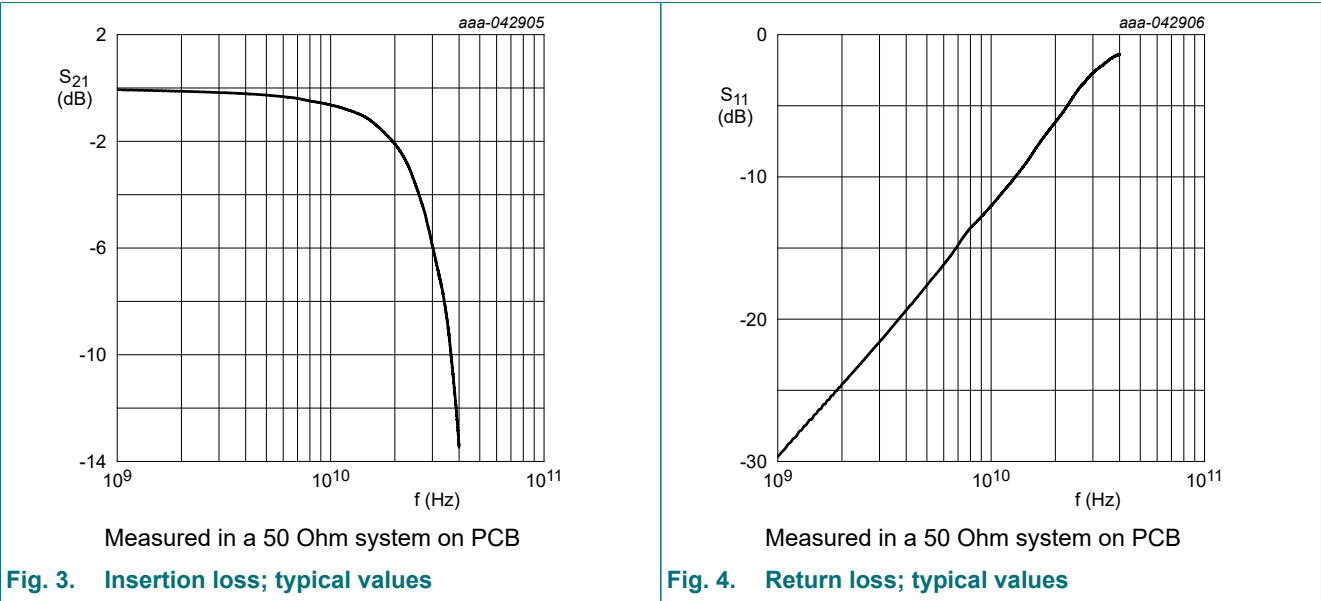
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C		5.6	7	10	V
V _{t1}	trigger voltage	t _p = 100 ns; T _{amb} = 25 °C	[1]	-	7.9	-	V
I _{RM}	reverse leakage current	V _{RWM} = 5.5 V; T _{amb} = 25 °C		-	1	50	nA
		V _{RWM} = -5.5 V; T _{amb} = 25 °C		-	-1	-50	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	0.26	0.31	pF
V _{CL}	clamping voltage	I _{PP} = 8 A; t _p = 100 ns; T _{amb} = 25 °C	[1]	-	4.3	-	V
		I _{PP} = 16 A; t _p = 100 ns; T _{amb} = 25 °C	[1]	-	6	-	V
		I _{PP} = 8 A; t _p = 8/20 µs; T _{amb} = 25 °C	[2]	-	4.6	-	V
R _{dyn}	dynamic resistance	I _R = 12 A; t _p = 100 ns; T _{amb} = 25 °C	[1]	-	0.2	-	Ω
		I _R = -12 A; t _p = 100 ns; T _{amb} = 25 °C	[1]	-	0.2	-	Ω
α _{IL}	insertion loss	f = 10 GHz; T _{amb} = 25 °C		-	-0.64	-	dB
α _{RL}	input return loss			-	-12	-	dB
f _{-3dB}	-3 dB cut-off frequency	T _{amb} = 25 °C; normalized to attenuation at 1 MHz		-	23.6	-	GHz

- [1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.
- [2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.



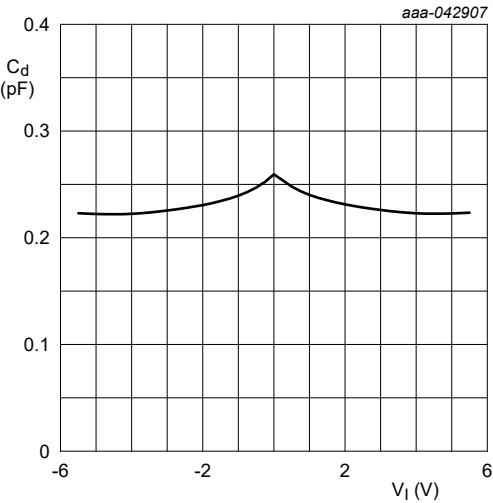
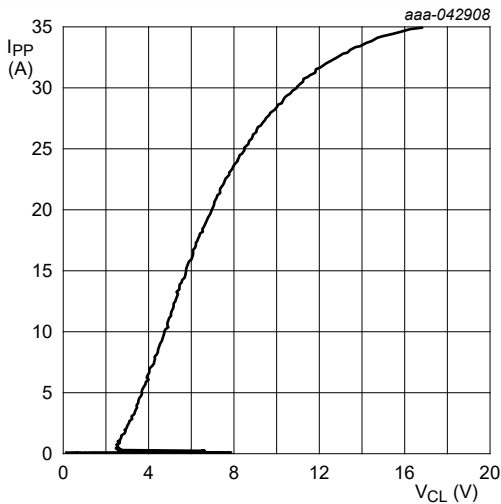
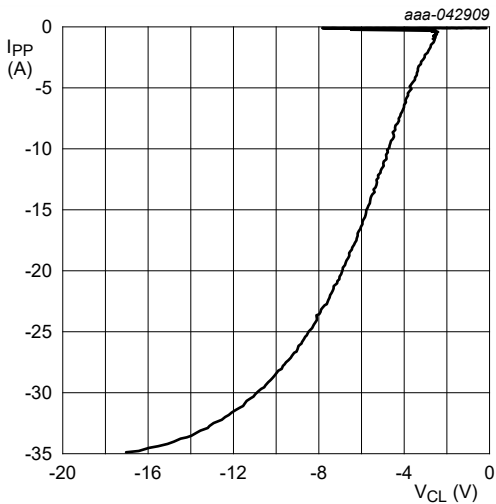


Fig. 5. Capacitance as a function of reverse standoff voltage; typical values



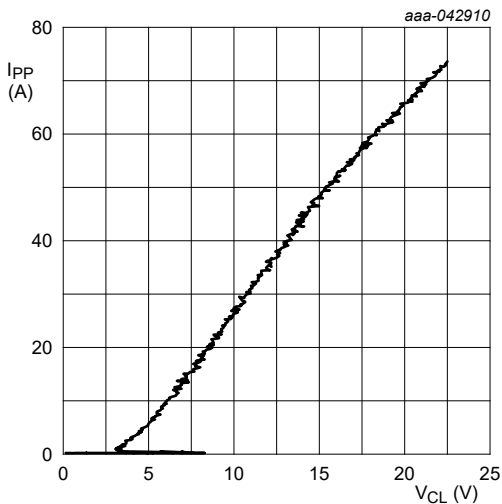
Transmission Line Pulse (TLP);
 $t_p = 100$ ns; $t_r = 1$ ns

Fig. 6. Dynamic resistance with positive clamping; typical values



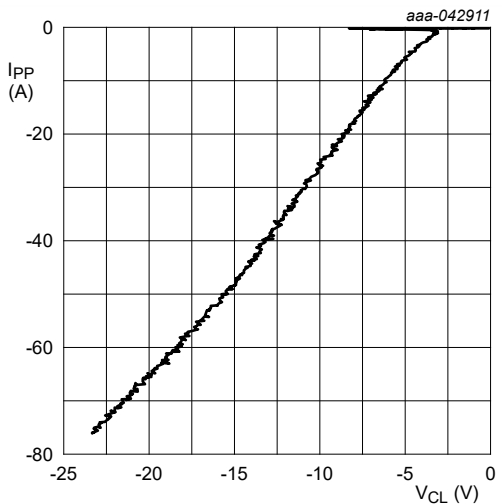
Transmission Line Pulse (TLP);
 $t_p = 100$ ns; $t_r = 1$ ns

Fig. 7. Dynamic resistance with negative clamping; typical values



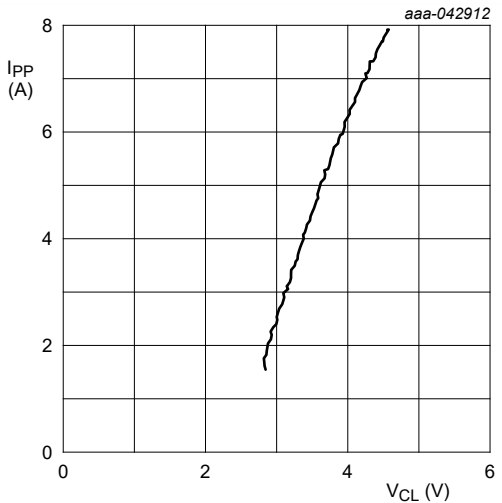
Very-Fast Transmission Line Pulse (VF-TLP);
 $t_p = 5\text{ ns}$; $t_r = 600\text{ ps}$

Fig. 8. Dynamic resistance with positive clamping; typical values



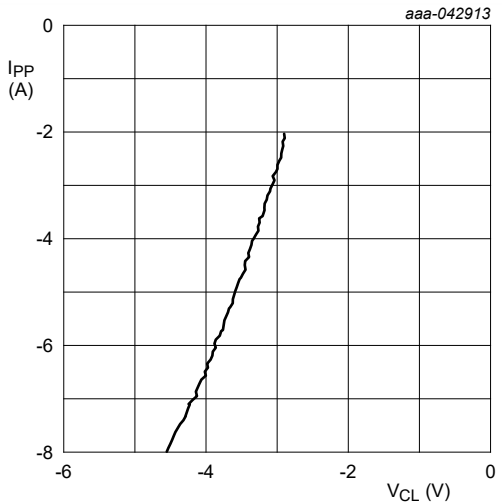
Very-Fast Transmission Line Pulse (VF-TLP);
 $t_p = 5\text{ ns}$; $t_r = 600\text{ ps}$

Fig. 9. Dynamic resistance with negative clamping; typical values



IEC 61000-4-5; $t_p = 8/20\text{ }\mu\text{s}$; positive pulse

Fig. 10. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20\text{ }\mu\text{s}$; negative pulse

Fig. 11. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

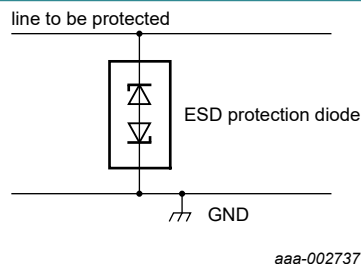


Fig. 12. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

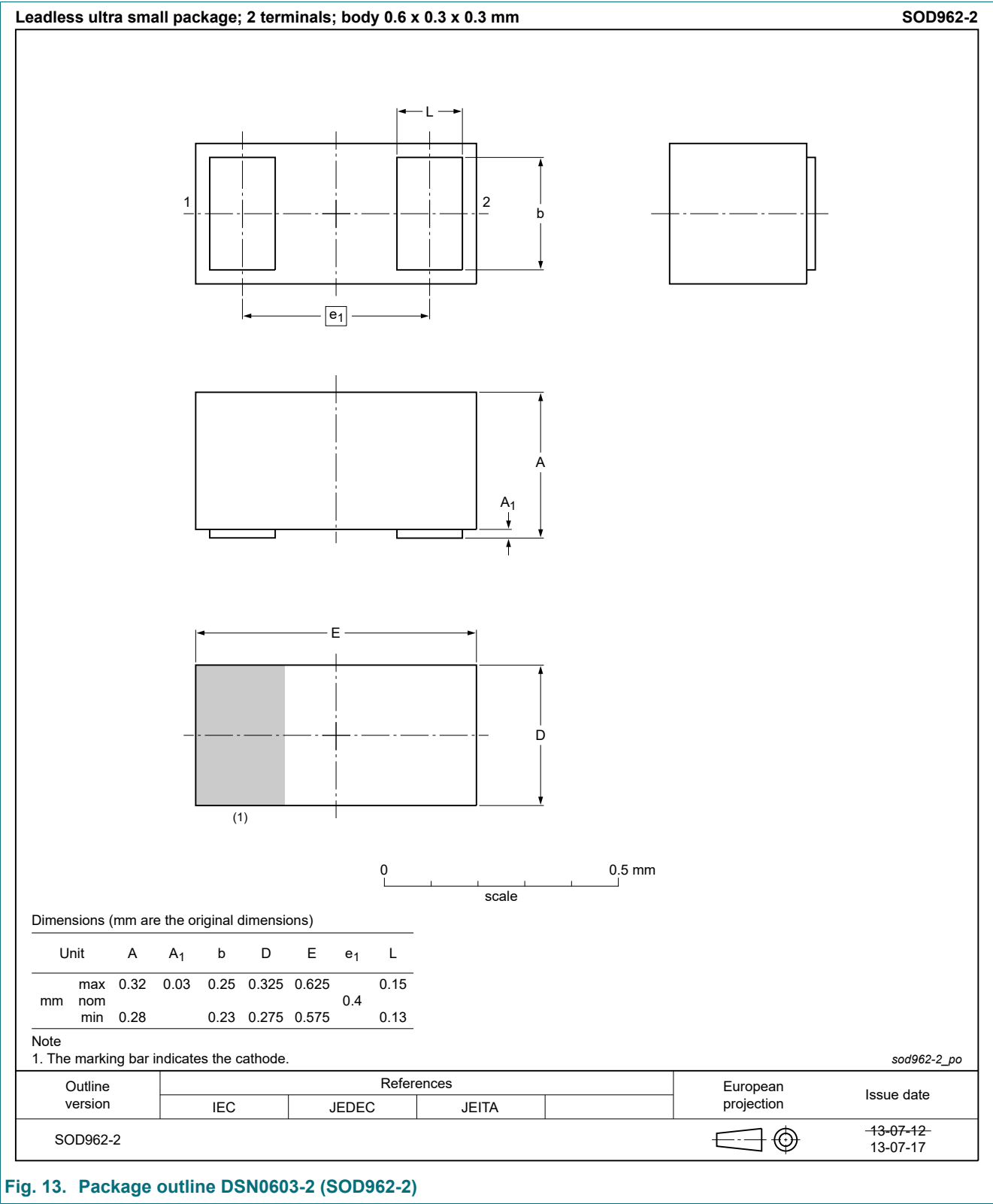
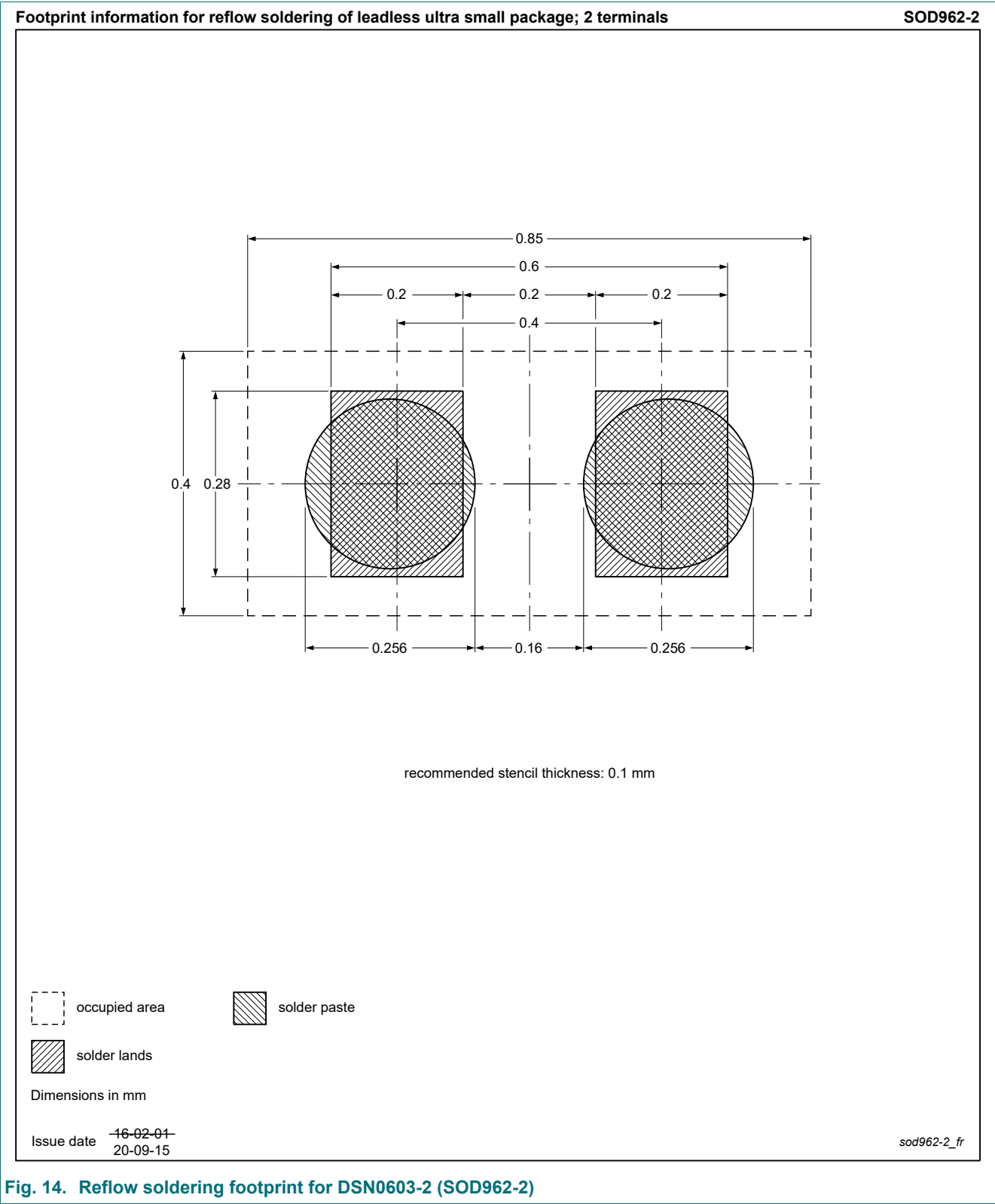


Fig. 13. Package outline DSN0603-2 (SOD962-2)

13. Soldering



14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V5C1BBSF-Q v.1	20250716	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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