

### Description

The PESDHC2FD7VUH ESD protector is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, lower operating voltage, lower clamping voltage and no device degradation when compared to MLVs. The PESDHC2FD7VUH protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. The PESDHC2FD7VUH is available in a DFN1006-2L package with working voltages of 7 volt. It gives designer the flexibility to protect one unidirectional line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium.



**DFN1006-2L(Bottom View)**

### Feature

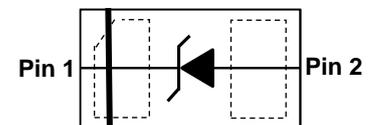
- 450W Peak pulse power per line ( $t_P = 8/20\mu S$ )
- DFN1006-2L package
- Replacement for MLV(0402)
- Unidirectional configurations
- Response time is typically < 1 nS
- Protect one I/O or power line
- Low clamping Voltage
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD)  $\pm 30kV$ (air),  $\pm 30kV$ (contact); IEC 61000-4-4 (EFT) 40A (5/50nS)



**Marking (Top View)**

### Applications

- Cell phone handsets and accessories
- Personal digital assistants (PDA's)
- Notebooks, desktops, and servers
- Portable instrumentation
- Cordless phones
- Digital cameras
- Peripherals
- MP3 players



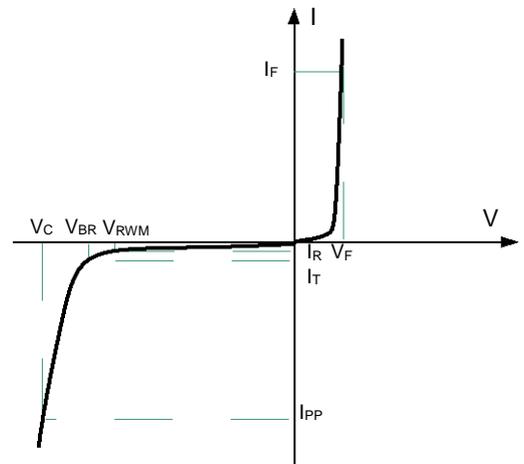
**Circuit Diagram**

### Mechanical Characteristics

- Mounting position: Any
- Qualified max reflow temperature: 260°C
- Device meets MSL 1 requirements
- DFN1006-2L without plating

Electronics Parameter

Symbol	Parameter
$V_{RWM}$	Peak Reverse Working Voltage
$I_R$	Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$P_{PP}$	Peak Pulse Power
$C_J$	Junction Capacitance
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$



Electrical characteristics per line @25°C ( unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	$V_{RWM}$				7	V
Breakdown Voltage	$V_{BR}$	$I_T = 1mA$	7.5		10	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 7V$			1	$\mu A$
Clamping Voltage <sup>(1)</sup>	$V_C$	TLP=16A, $t_P = 100ns$		10.5		V
Dynamic Resistance <sup>(1)</sup>	$R_{DYN}$			0.09		$\Omega$
Clamping Voltage <sup>(2)</sup>	$V_C$	$I_{PP} = 10A, t_P = 8/20\mu S$		10.5	12.5	V
		$I_{PP} = 32A, t_P = 8/20\mu S$		14.5	16.5	V
Junction Capacitance	$C_J$	$V_R = 0V, f = 1MHz$		180		pF

Notes: 1) TLP parameter:  $Z_0 = 50\Omega, t_p = 100ns, t_r = 2ns$ , averaging window from 60ns to 80ns.  $R_{DYN}$  is calculated from 4A to 16A.

2) Non-repetitive current pulse, according to IEC61000-4-5.

Absolute maximum rating @25°C

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_P = 8/20\mu s$ )	$P_{PP}$	450	W
Peak Pulse	$I_{PP}$	32	A
Lead Soldering Temperature	$T_J$	-55 to 150	°C
Operating Temperature	$T_{STG}$	-55 to 150	°C
ESD Protection-Contact Discharge	$V_{ESD}$	$\pm 30$	kV
ESD Protection-Air Discharge	$V_{ESD}$	$\pm 30$	kV

Typical Characteristics

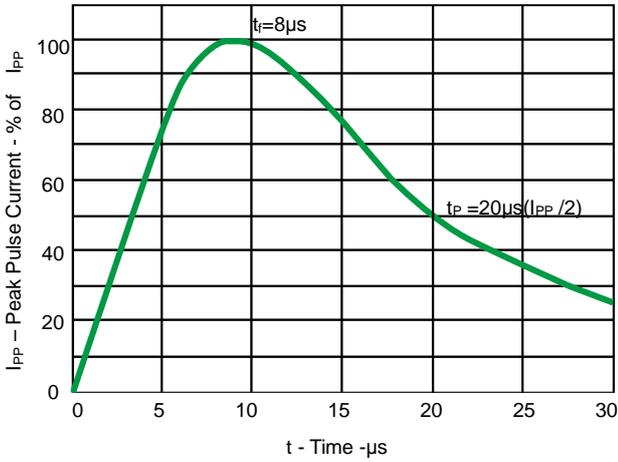


Fig 1. Pulse Waveform

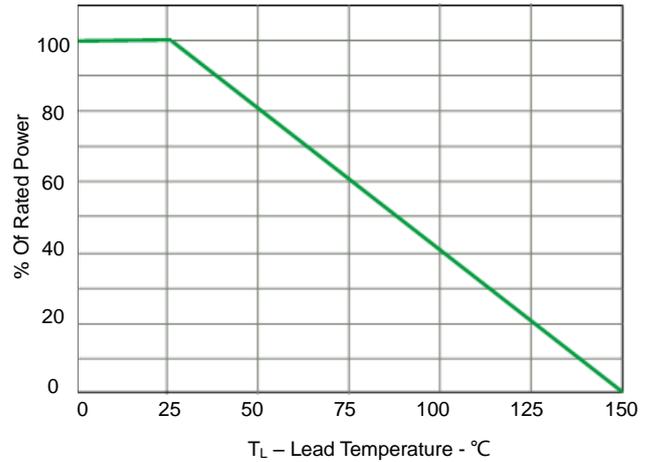


Fig 2. Power Derating Curve

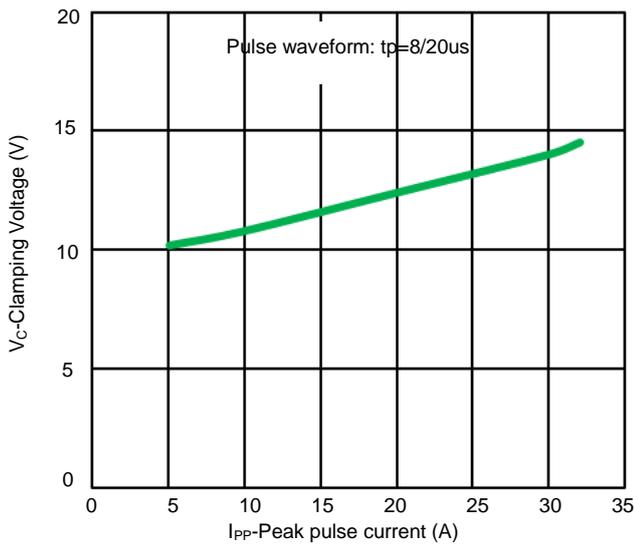


Fig 3. Clamping voltage vs. Peak pulse current

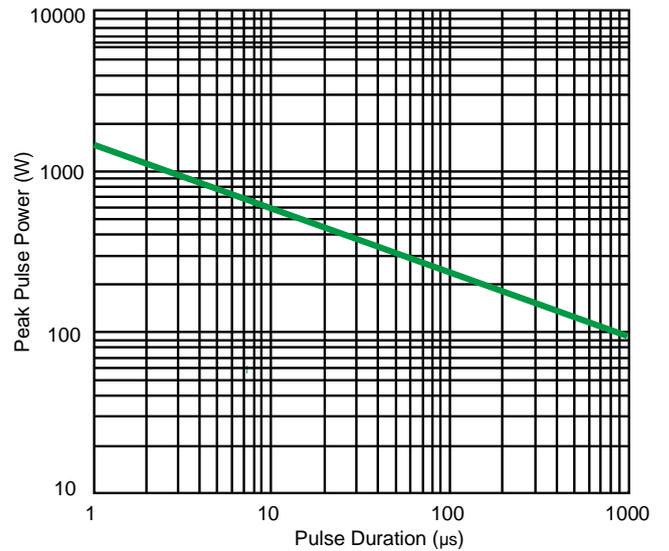


Fig 4. Non-Repetitive Peak Pulse Power vs. Pulse time

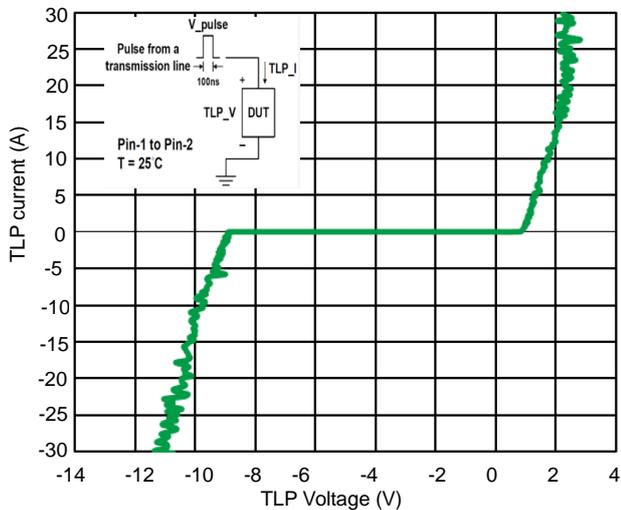


Fig 5. TLP Measurement

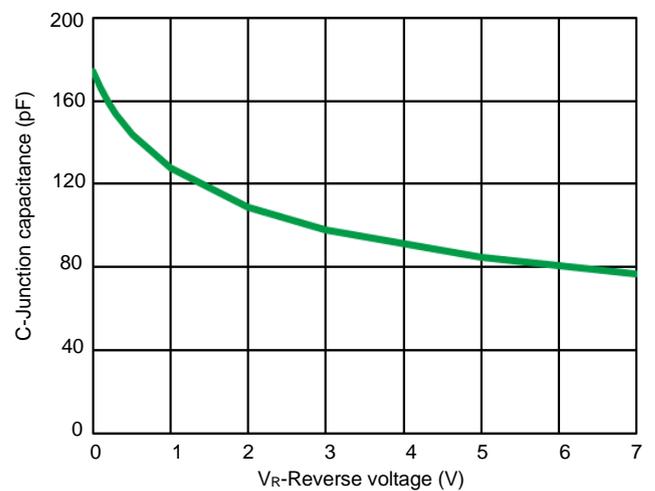


Fig 6. Capacitance vs. Reverse voltage

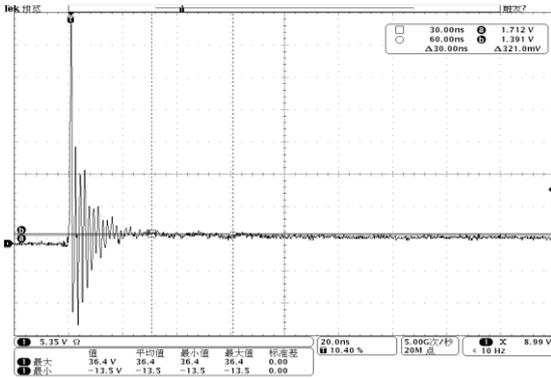


Fig 7. ESD clamping voltage (IEC61000-4-2 +8kV contact)

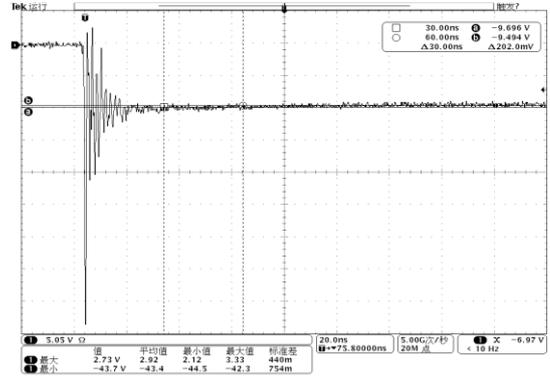
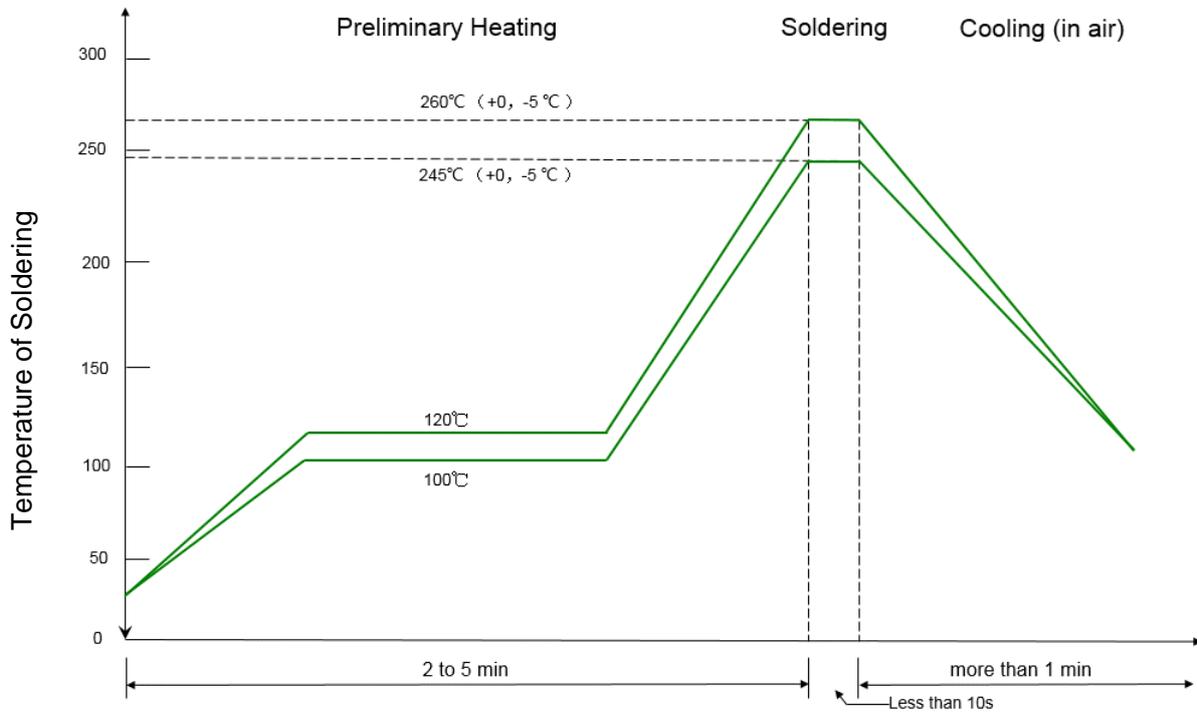


Fig 8. ESD clamping voltage (IEC61000-4-2-8kV contact)

Solder Reflow Recommendation



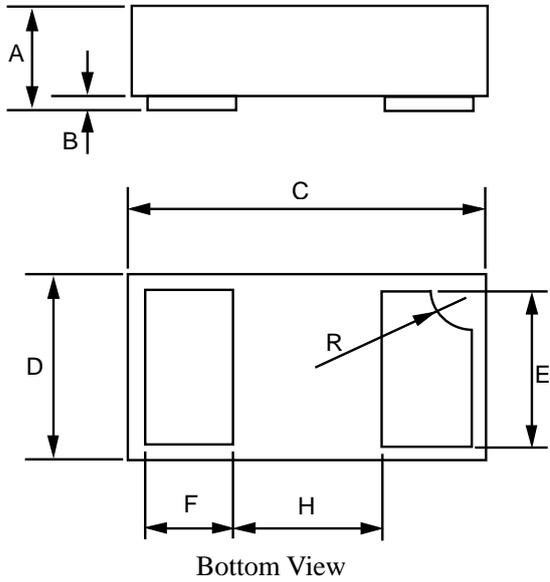
Remark: Pb free for 260°C; Pb for 245°C

PCB Design

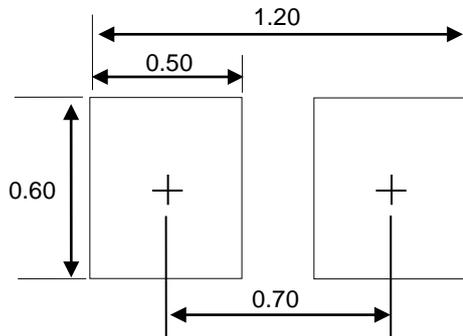
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (DFN1006-2L)



Dim	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.013	0.020	0.34	0.50
B	0.000	0.002	0.00	0.05
C	0.037	0.043	0.95	1.080
D	0.022	0.027	0.55	0.68
E	0.016	0.024	0.40	0.60
F	0.008	0.012	0.20	0.30
H	0.015Typ.		0.40Typ.	
R	0.001	0.005	0.05	0.15



Unit: mm

Suggested PCB Layout

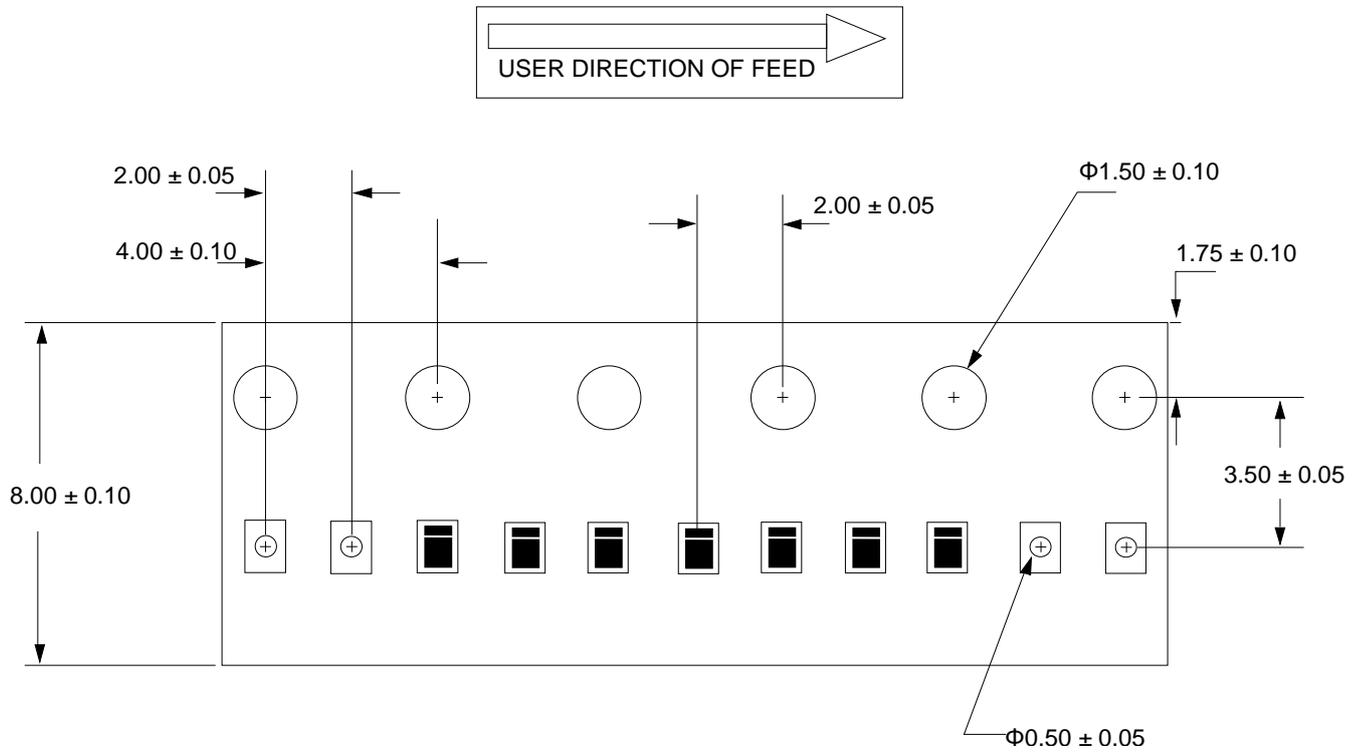
Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

Ordering information

Device	Package	Reel	MPQ
PESDHC2FD7VUH	DFN1006-2L (Pb-Free)	7"	10000 / Tape & Reel

Load with information



Unit: mm

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