PF0027

Preliminary

MOS FET Power Amplifier Module for E-TACS Handy Phone

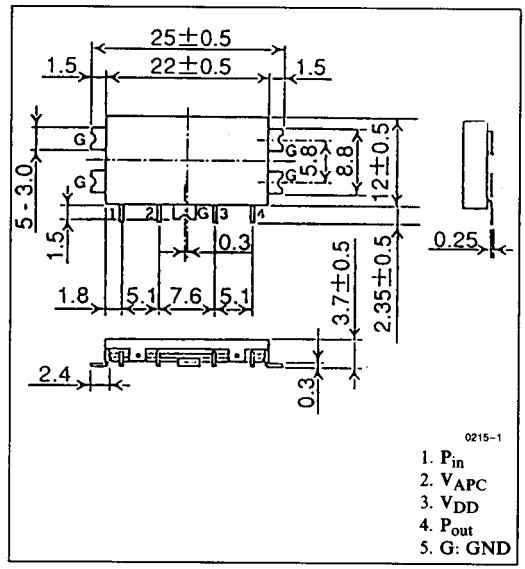
■ FEATURES

- Surface Mounted Small Package with Shielded Cover 1cc, 3g
- High Efficiency ..... 47% Typ at Actual Output Condition 1.2W
- Low Voltage Operation 6V
- Low Power Control Current ..... 300 μA

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	12	V
Supply Current	I_{DD}	2	A
APC Voltage	V_{APC}	±8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	T_C(op)	−30 ~ +100	°C
Storage Temperature	T_{stg}	−30 ~ +100	°C

■ OUTLINE DRAWING (Unit: mm)



■ ELECTRICAL CHARACTERISTICS (T_C = 25°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Drain Cutoff Current	I_{DS}	—	100	μA	V_{DD} = 12V, V_{APC} = 0V, Rg = R_L = 50Ω
Total Efficiency	ηT	43	—	%	f = 872 to 905 MHz, P_{in} = 2 mW, V_{DD} = 6V, Rg = R_L = 50Ω, P_{out} = 1.2W (at APC Controlled)
2nd Harmonic Distortion	2nd H.D.	—	−30	dB	
3rd Harmonic Distortion	3rd H.D.	—	−30	dB	
Input VSWR	VSWR(in)	—	3	—	
Output Power	P_{out}(1)	1.6	—	W	V_{DD} = 6V, f = 872 to 905 MHz, P_{in} = 2 mW, V_{APC} = 4V, Rg = R_L = 50Ω
Isolation	P_{out}(2)	—	−35	dBm	V_{DD} = 6V, f = 872 to 905 MHz, P_{in} = 2 mW, V_{APC} = 0.5V, Rg = R_L = 50Ω
Load VSWR Tolerance	—	No Degradation		—	V_{DD} ≤ 8V, f = 872 to 905 MHz, P_{in} = 2 mW, Rg = 50Ω, V_{APC} ≤ 4V, t = 20 sec, Load VSWR ≤ 20 All Phase Angles
Stability	—	No Parasitic Oscillation		—	f = 872 to 905 MHz, P_{in} = 2 mW, V_{DD} = 5.2 ~ 7.5V, P_{out} ≤ 1.6W, Zg = 50Ω, Load VSWR = 3 All Phases Angles

2

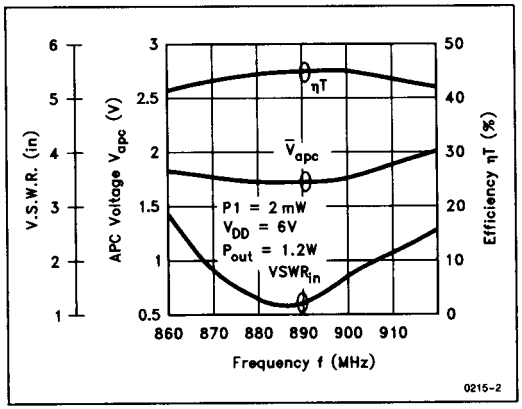


Figure 1

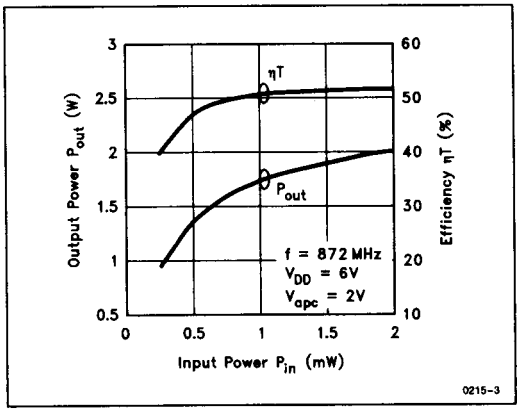


Figure 2

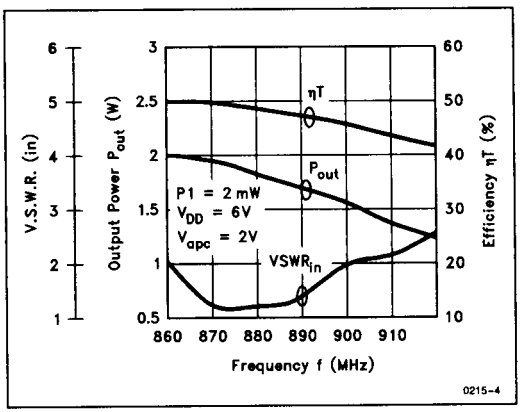


Figure 3

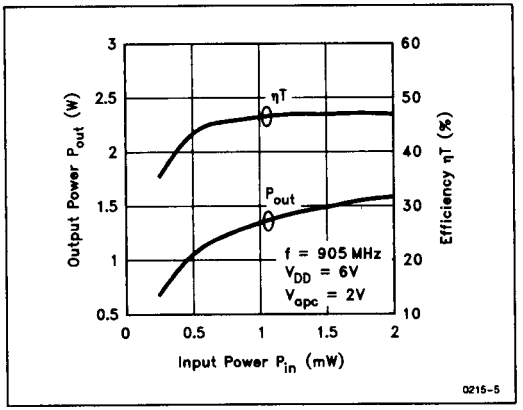


Figure 4

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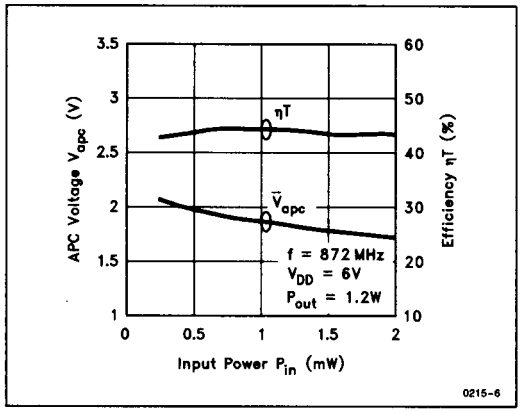


Figure 5

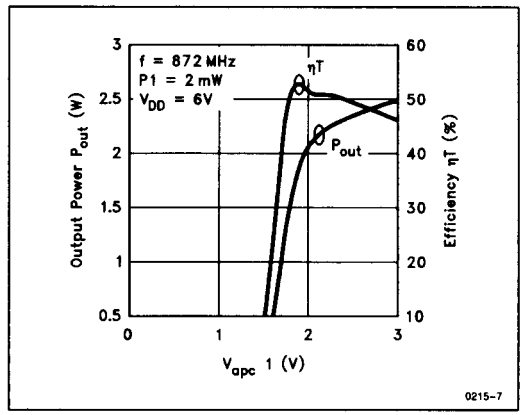


Figure 6

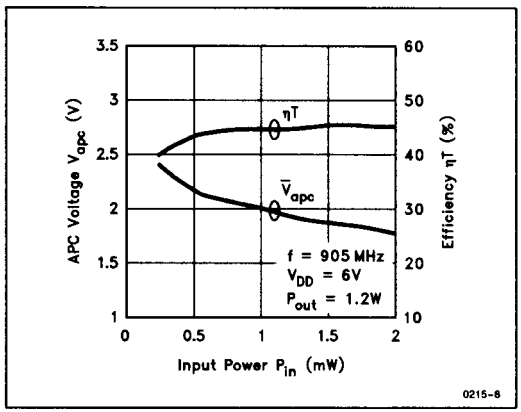


Figure 7

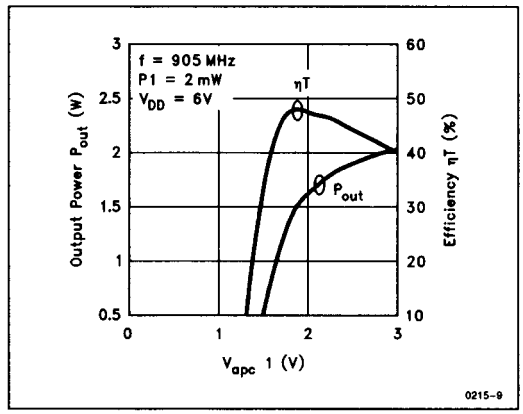


Figure 8

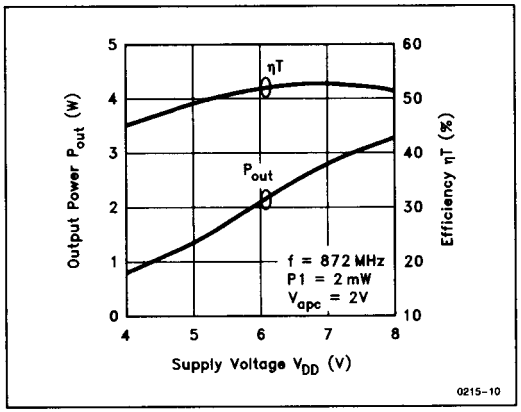


Figure 9

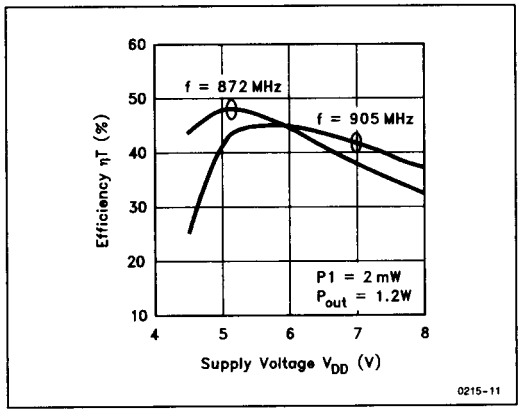


Figure 10

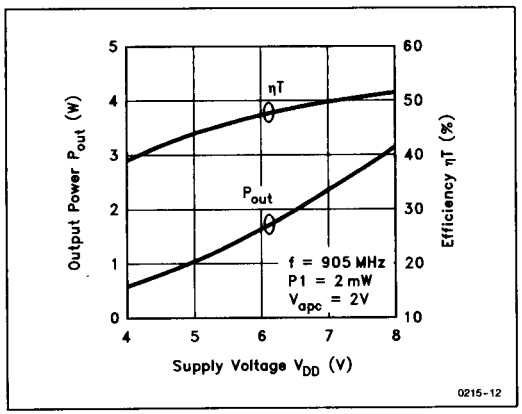


Figure 11

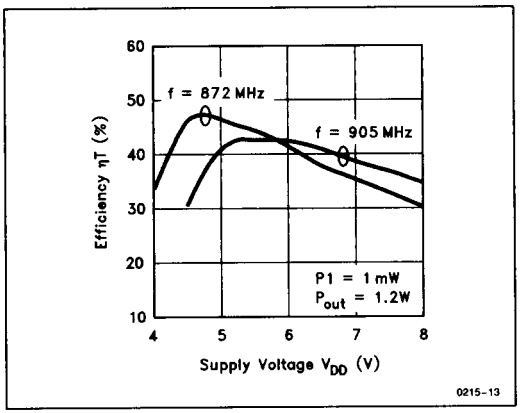


Figure 12

■ TEST SYSTEM DIAGRAM

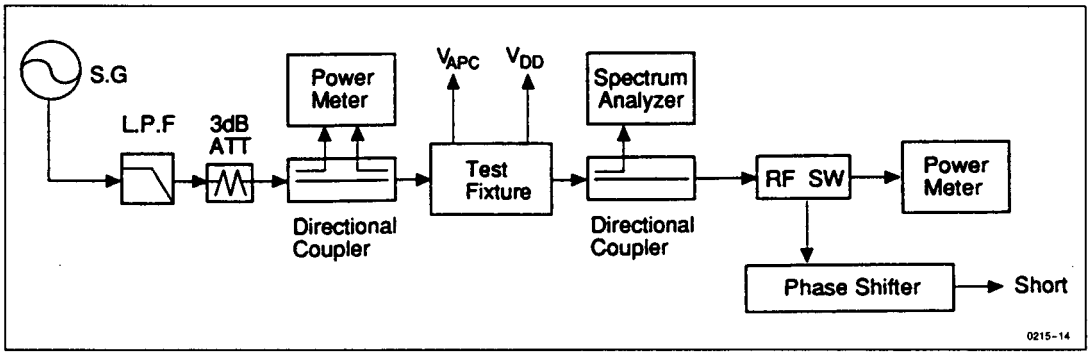
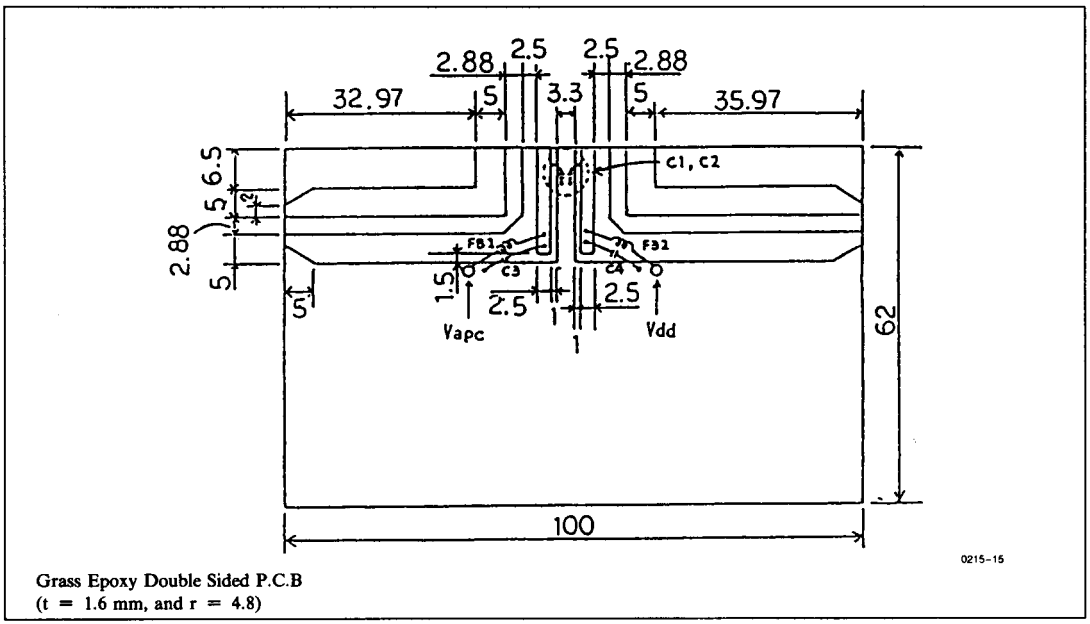


Figure 13

■ TEST FIXTURE PATTERN

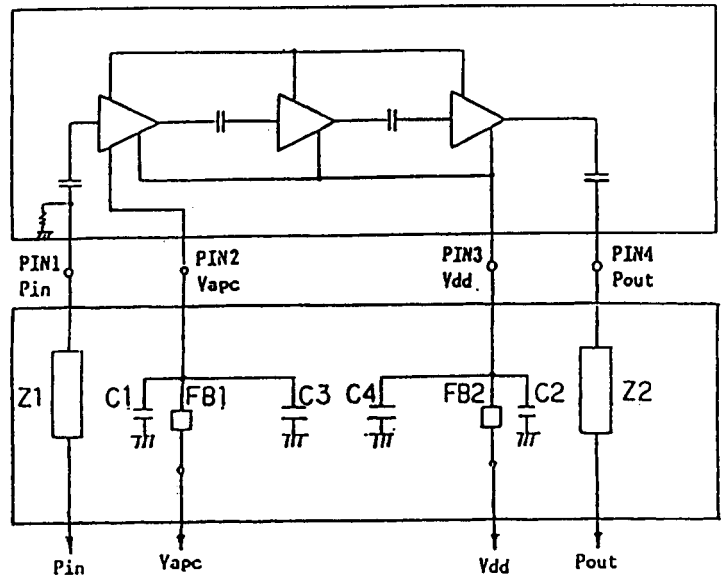
Unit: mm



Grass Epoxy Double Sided P.C.B
(t = 1.6 mm, and r = 4.8)

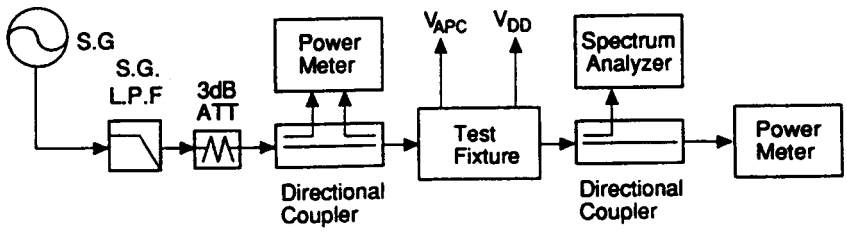
Figure 14

■ INTERNAL DIAGRAM AND EXTERNAL CIRCUIT



C1 = C2 = 0.01 μF Ceramic Chip
C3 = C4 = 4.7 μF Tantalum
FB = Ferrite Bead BLO1RN1-A62-001 (Murata) or Equivalent
Z1 = Z2 = 50Ω Microstrip Line

Figure 15



Output power P_{out} is defined at the root point of the module output pin P_{out}.
The coefficient of output power loss **in the PCB output line Z2** is: $1/(S_{21})^2 = 1/(0.9805)^2 = 1.04$

Figure 16

■ NOTE FOR USE

1. Don't apply the reflow soldering process.
2. Don't apply the dipping solder process to the lead pins.
3. To avoid the stress against the lead pins, lead pins should be soldered after the soldering of ground flange.
4. Soldering temperature and time should be less than 230°C, 10 sec per each pin.
5. To protect devices from electro-static damage, soldering iron, measuring equipment and human body etc. should be grounded.
6. To avoid the degradation of efficiency and output power, lead pins should not be float from PCB, and connected just on the RF signal line. (Refer to Figure 17.)
7. Recommendation to decrease the thermal resistance is shown below.
   a. Arrangement of through holes under as many as possible under **PF0027**.
   b. Addition of external heat sink on the metal case of **PF0027**.
8. Don't wash **PF0027** except led pins and ground flanges.
9. It should be recommended to apply a non-chlorine solder for modules. For example, KR19 by Nihpn Almit Co., LTD.
10. When the external parts (Isorator, Duplexer, etc.) of the module are changed, the electrical characteristics should be evaluated enough.
11. When V_{APC} is increased more than 3V, output power is saturated, however, drain current is increased still more. So V_{APC} should be limitted less than 3V.

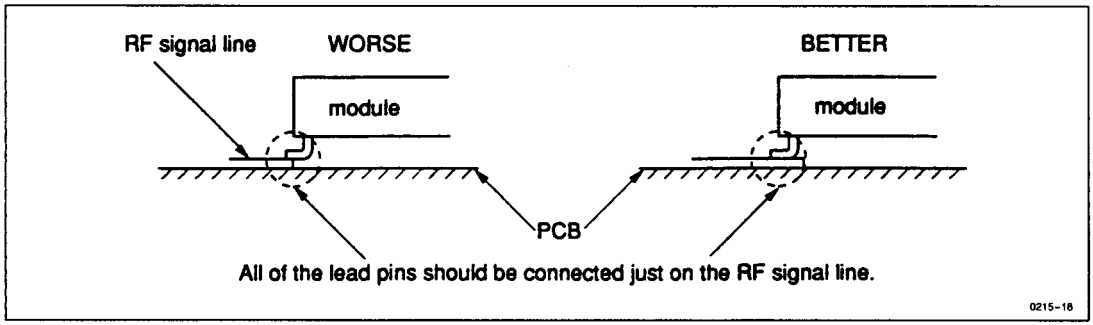


Figure 17