Green PWM Current-Mode Controller with Excellent Efficiency Improvement

Preliminary Specification Rev. P4, (Confidential for AtechOEM only)

FEATURES

- CCM/Valley Switching Operation
- High Driving Capability +200mA/-600mA
- Adjustable OVP (Over Voltage Protection)
- Accurate OLP (Over Load Protection)
- VCC OVP (Internal OVP)
- AC Brown in/out Protection
- DEM/CS Open/Short Protection
- Internal Slope Compensation
- Current Mode Control
- Tiny SOT-26 Package
- Extremely Low Startup Current(<1uA)
- Internal Soft Start
- Internal and External OTP

APPLICATIONS

- AC/DC Adaptor
- AC/DC Power Supply

GENERAL DESCRIPTION

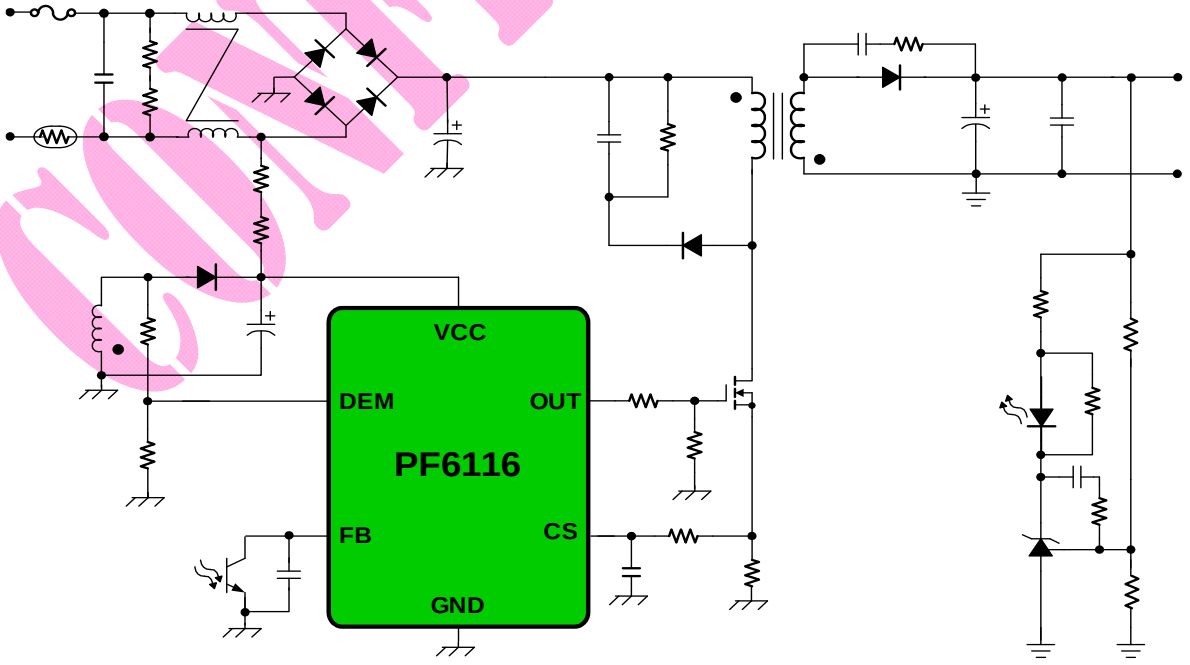
The PF6116 provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, and switch to valley switching at light load.

Using Power Forest patented technology, several function are integrated: OVP, OLP, SCP and AC brown in/out functions. A compact and robust power supply can be implemented using very few external components.

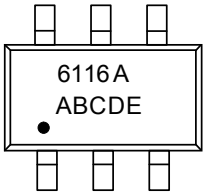
With ultra low startup current and switching frequency control, PF6116 also offers good power saving performance. The operation further gets into burst mode for light load efficiency.

PF6116 is packaged by using tiny SOT-26 package.

TYPICAL APPLICATION

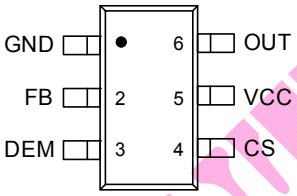


MARKING INFORMATION



6116A:	IC Part Number
Datecode:	ABCDE
A:	Year Code (A~Z mean 2010~2035)
B:	Week Code (A~Z and a~y mean WW01~WW51, z mean WW52+WW53
CDE:	Package Lot Code

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN NAME	PIN NO.	DESCRIPTION
GND	1	Ground
FB	2	Voltage feedback pin. By connecting a photo-coupler, the voltage feedback loop is built to close the control loop and regulate the output voltage of isolated AC/DC power supplies
DEM	3	Demagnetization detection signal. This pin can also provide adjustable output voltage OVP and AC brown in/out protection.
CS	4	The CS pin plays the role as providing the current feedback signal for current mode control. The OCP (over current protection) and OTP (over temperature protection) are also detected from this pin.
VCC	5	Voltage Supplying and VCC over voltage protection.
OUT	6	MOSFET Gate Driver

ORDERING INFORMATION

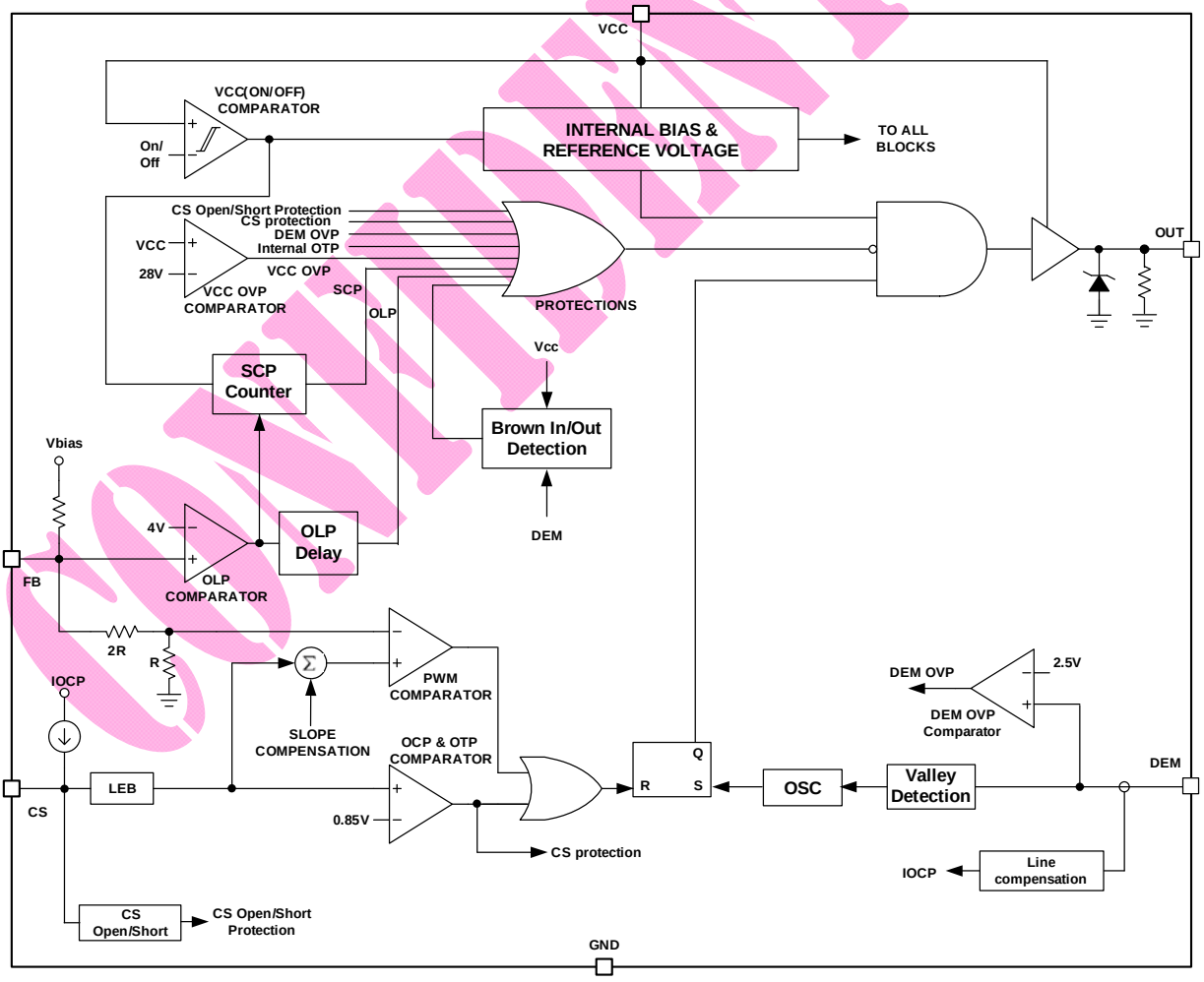
Part number	Package	Switch Frequency	Temp. Range	Protection Mode			
				VCC OVP	DEM OVP	OLP	SCP
PF6116AG	SOT-26	65KHz	-40°C to 85°C	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery
PF6116CG	SOT-26	65KHz	-40°C to 85°C	Latch	Latch	Auto-Recovery	Auto-Recovery
PF6116LG	SOT-26	65KHz	-40°C to 85°C	Latch	Latch	Latch	Latch

Note:

1. Part number "G" is package code for SOT-26, due to limited package space, won't mark "G" on IC body.
2. All Power Forest ICs are GREEN products and meet the following criterions:

- RoHS Compliance
- Pb-free and Halogen-free

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

- VCC ..... -0.3~30V
- OUT ..... -0.3~VCC+0.3V
- FB, CS, DEM ..... -0.3~5.5V
- Junction Temperature ..... 150°C
- Lead Temperature (Soldering, 10sec) ..... 260°C
- Operating Ambient Temperature ..... -40°C to 85°C
- Storage Temperature Range ..... -65°C to 150°C
- Package Thermal Resistance, θ_{JA} (SOT-26) ..... 250°C/W
- Power Dissipation @ T_A = +25°C (SOT-26) 400mW

Caution:

Stresses beyond those ratings listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Rating" condition for extended periods may affect device reliability.

Note:

(1) Tested per JEDEC51-3 standard at T_A = 25°C

(2) Calculated in accordance with junction temperature T_J = 125°C

RECOMMENDED OPERATING CONDITIONS

- Supply Voltage VCC ..... 11V to 26V
- Start up Resistor ..... 0.86~4.4 MΩ
- VCC Capacitor ..... 2.2~4.7 μF

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise stated, VCC=15V)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage					
VCC (ON)		15	16	17	V
VCC (OFF)		8.5	9	9.5	V
Vcc holdup Level		9.5	10	10.5	V
Startup Current	VCC<VCC (ON)-0.5V			1	μA
Operating Current	V_{FB}=3V Cout=1nF		1.25		mA
	V_{FB}=Burst Level		330		μA
	Protect mode current	350	450	550	μA
VCC OVP Threshold		27	28	29	V
VCC De-Latch Level	VCC=VCC De-Latch Level+0.1V		2.35		V
VCC De-Latch Current	VCC=VCC De-Latch Level+0.1V		4.5		μA
VCC OVP De-bounce Time	Guaranteed by Design		4		Times
Oscillator & Switching Frequency					
Switching Frequency		62	65	68	KHz
Temperature Stability	Guaranteed by Design			5	%
Voltage Stability				2	%
Green Mode Frequency		20	23	26	KHz
Frequency Spreading Range			±5.0		KHz
Spreading Frequency			245		Hz
Voltage Feedback					
Open Loop Voltage		4.5			V
OLP Level		3.8	4.0	4.2	V
High-Threshold			1.95		V
Low-Threshold			1.65		V
Zero Duty Level	OUT disable		300		mV
Zero Duty Hys.	OUT recovery		200		mV
OLP De-bounce Time	VFB>4V	70	80	90	mS
FB Pin Short Current		100	120	140	uA
Current Sensing					
Vcs (off)	1. Over current protection level 2. Over temperature protection level	0.83	0.85	0.87	V
Leading Edge Blanking Time (LEB)	Guaranteed by Design		150		nS
Propagation Delay Time	Guaranteed by Design		100		nS
OCP Compensation Current	IDEM source current=100uA		200		μA

Slope Compensation	Guaranteed by Design		300		mV
Soft Start Time			8		mS
Gate Drive Output					
Output Low Level	VCC=15V,Iout=20mA			1	V
Output High Level	VCC=15V,Io=20mA	11.5		15	V
Rising Time	10% to 90% of Vout, CL=1nF		250		nS
Falling Time	90% to 10% of Vout, CL=1nF		30		nS
Out Clamping	VCC=20V		13.5		V
Maximum Duty Cycle		70	75	80	%
Demagnetization (DEM) Detection					
DEM OVP sampling instant	Guaranteed by Design		3		uS
DEM OVP threshold level		2.45	2.5	2.55	V
DEM OVP De-bounce Time	Guaranteed by Design		4		Times
Demagnetization Detection level	Guaranteed by Design		350		mV
Demagnetization delay	Guaranteed by Design		270		nS
DEM_BNI		47	50	53	uA
DEM_BNO		43	45.5	48	uA
BNO De-bounce Time		70	80	90	mS
Thermal Shut Down					
OTP Threshold			145		℃
Hysteresis			30		℃

APPLICATION NOTE

Start-up Circuit

The start-up circuit of the PF6116 is shown in Fig.1. A startup resistor is connected to one node of the AC mains (L,N). The start-up current is supplied through R1 and R2 to charge the C1 capacitor. The component values of R1,R2 and C1 will affect the startup time and power loss of R1 and R2. The extremely low start-up current technology of PF6116 (< 900nA max.) is made to implement higher value of start-up resistor to obtain low power consumption in R1 and R2. The ultra low operation current at burst mode is specially designed (0.33mA Typ.), so the user could adopt smaller VCC capacitor to achieve quick startup time. The recommended components parameter of R1,R2 and C1 are 430KΩ+430KΩ with 4.7uF VCC capacitor, respectively. The power loss of R1 and R2 are 37mW at 264Vac and start up time is 1.8 second at 90Vac. The D1 IN4148 can improve surge capability to 6.6KV.

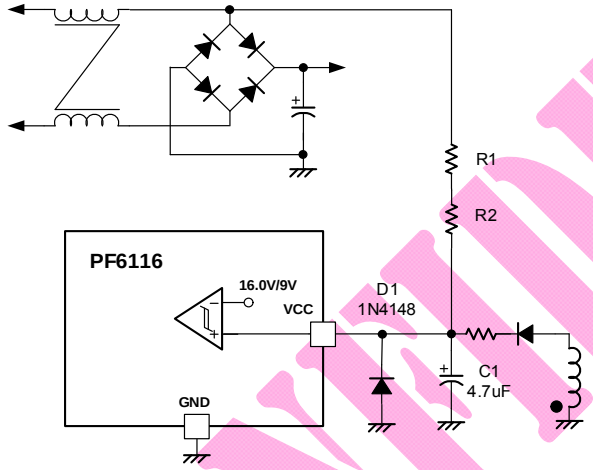


Fig. 1 Startup Circuit

Operation Mode

The PF6116 provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, once if the converter enters into DCM, the PF6116 automatically finds the local minimum Vds point and switching at this local valley.

Normally, the conduction loss is dominated at heavy load condition, and the switching loss turns to be larger than conduction loss in light load, especially at 1/4 ~ 1/2 of full load. By this kind of mixed mode operation to have CCM in heavy load and valley switching in light load can optimize the overall average efficiency during the entire operation range.

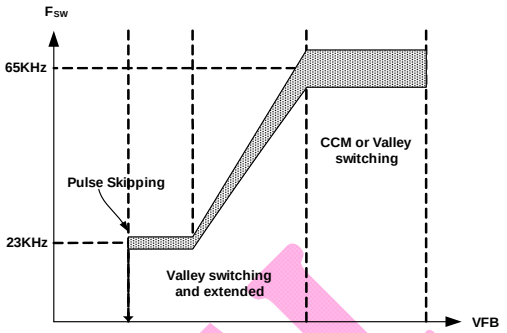


Fig. 2 FB vs. Fsw Curve

As shown in Fig. 3, at deep light-load or no-load condition, the switching loss is the dominant factor. To improve the light-load efficiency, burst mode operation will stop the switching cycle of the OUT pin when FB pin voltage is below “Zero Duty OFF” Level and restart the switching cycle of the OUT pin when FB pin voltage is above “Zero Duty ON Level”.

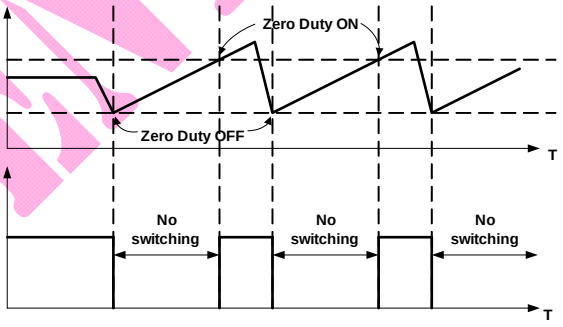


Fig. 3 Burst Mode Operation

Over Voltage Protection on VCC Pin

After startup sequence, the auxiliary winding of transformer (as shown in Fig. 4) will take over the supply voltage of VCC. The auxiliary winding couples with the main transformer in different turn ratio. Thus, the auxiliary voltage is in proportional to output voltage. When output feedback loop is open, the PF6116 FB pin voltage will go high. It will increase the PWM duty’s on time and primary peak current, which will let the transformer to transfer more power to secondary side. Therefore the output voltage and the VCC pin voltage of auxiliary winding will rise toward the maximum level as soon as possible. While the VCC pin voltage exceeds VCC OVP threshold (28V typ.), the internal OVP comparator will be triggered, and the PF6116 will stop OUT pin from switching immediately to avoid power circuit from damage.

When the OUT pin stops switching, the power of

VCC will not be supplied by the auxiliary winding. The VCC pin will sink a protection current to discharge the energy that is stored in the VCC capacitor (as shown in Fig. 5). The VCC OVP will not be reset until VCC (off) is tripped.

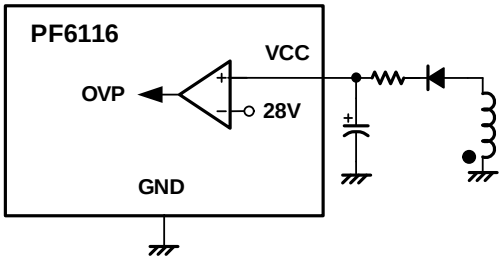


Fig. 4 VCC OVP

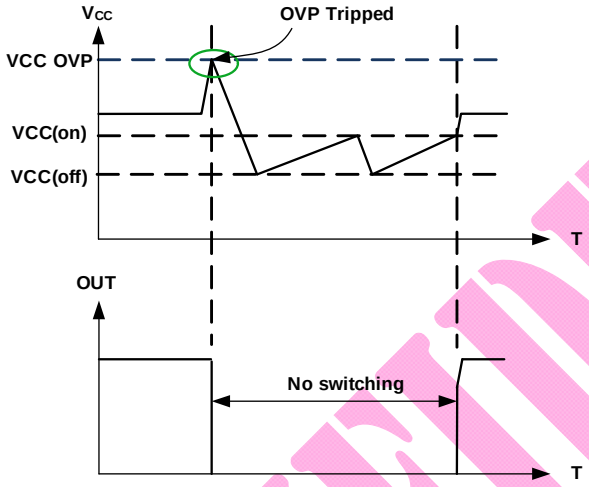


Fig. 5 VCC OVP Operation

Open Loop Protection

The purpose of the feedback loop is to maintain a constant output voltage operating from no-load to full-load with the full input voltage range. Once the feedback loop opens, the PF6116 will increase the on time of power MOSFET. In such condition, FB pin voltage will run toward the open loop level (4.5V min). Once the FB pin voltage exceeds the comparator's threshold level (4.0V Typ.) for a time longer than the open loop protection delay time (OLP De-bounce Time), the OUT pin of the PF6116 will stop switching immediately. And the VCC pin will sink a protection current to discharge the energy that is stored in the VCC capacitor until VCC (OFF) is tripped. After that, the open loop protection will be reset and the startup current will charge the VCC capacitor and restart again. (Refer to Fig. 6 & 7).

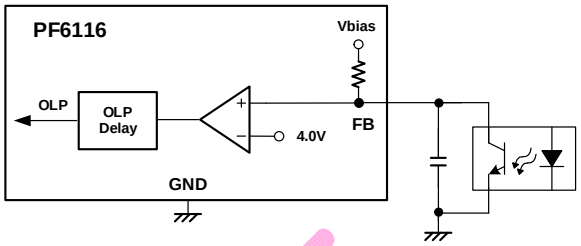


Fig. 6 Feedback Circuit on FB

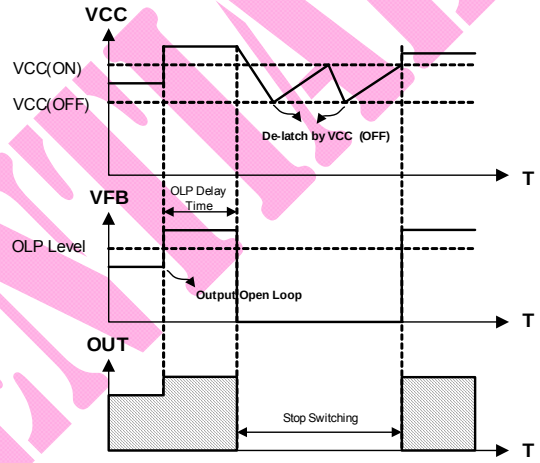


Fig. 7 OLP Operation of FB

Brown in/out & DEM OVP Protection

To prevent high current stress at too low AC voltage condition, the PF6116 implements an AC brown in/out protection through the DEM pin. The current sourcing out from the DEM pin when the OUT pin is enabled is monitored to have the AC input voltage level information. When the current keeps above the DEM_BNI threshold (50uA, typ.) for more than BNI De-bounce time 3 cycles, the AC brown in condition is issued and the OUT is enabled. Once if the current keeps under the DEM_BNO threshold (45.5uA, typ.) for more than BNO De-bounce time, the AC brown out condition is issued and the OUT is disabled.

The equation is used to calculate the brown in/out level:

$$V_{AC\_BNI} = 50u \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}}$$

$$V_{AC\_BNO} = 45.5u \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}}$$

An over voltage protection for Vo is fulfilled by

sampling the voltage on the DEM waveform after OUT is turn-off. After a short delay after OUT off, the sampled voltage is compared to the internal over voltage reference is determined whether if an OVP event is occurred. The internal over voltage reference is biased at 2.5V, uses can define the resistor divider ratio by the equation below based on the desired OVP level:

$$V_{O\_OVP} = 2.5 \times \frac{R_{DEM\_U} + R_{DEM\_D}}{R_{DEM\_D}} \times \frac{N_{SEC}}{N_{AUX}}$$

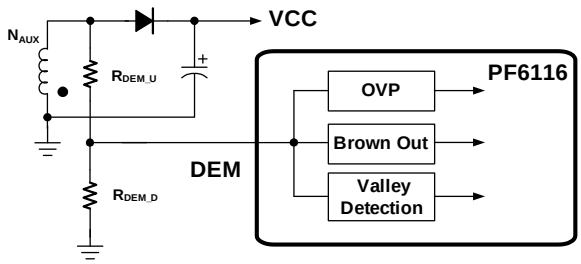


Fig. 8 DEM divider

Output Short Protection

Once the secondary output is shorted, the energy supplied from the aux. winding to the VCC capacitor is limited, leading to VCC drops to VCC (off) threshold. Things become worse especially in low output voltage applications, where the time internal of VCC collapse usually lower than the FB OLP timer. The PF6116 has output short circuited protection to limit the input power loss and lower the temperature of power components during this fault condition.

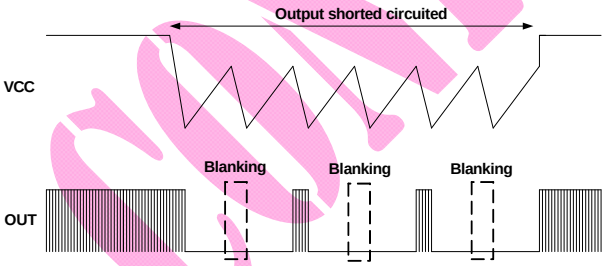


Fig. 9 Output Shorted Circuit Protection

VCC Hold Up Mode

At very light load conditions, the PF6116 may enter burst mode operation. The low frequency burst mode may lower VCC level while the operation current of PF6116 is only slightly lower than that at heavy load conditions.

To prevent the voltage on VCC is not enough to support normal operation at such extreme low load conditions, a scheme is added to supplement the energy to VCC. Every time the VCC level is lower than the VCC (off)+1v and the FB voltage is below the OLP trigger level, the OUT is enabled to have a small high period.

Cycle by Cycle Over-Current Protection

In a Flyback topology converter, the main MOSFET switch of the Flyback converter turns on and off rapidly. The energy is stored in the inductor when the MOSFET turns on. The inductor current flowing through the sensing resistor (RS) is shown in Fig. 10. The current limit is determined by the equation below:

$$I_{PEAK} = \frac{V_{CS}}{R_{RS}}$$

In order to prevent the CS pin from false triggering, an internal leading edge blanking time (200 nS Typ.) is added and an external low pass RC filter is also recommended to filter the turn-on spike of CS node.

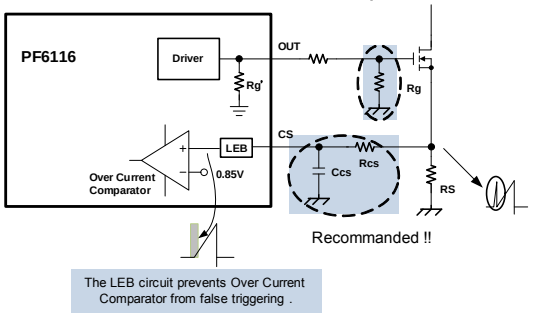
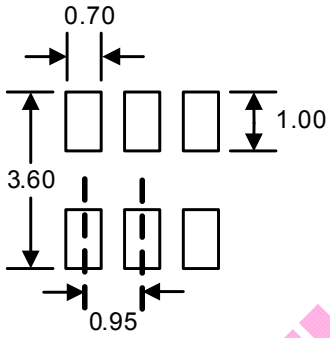


Fig. 10 Current Sensing

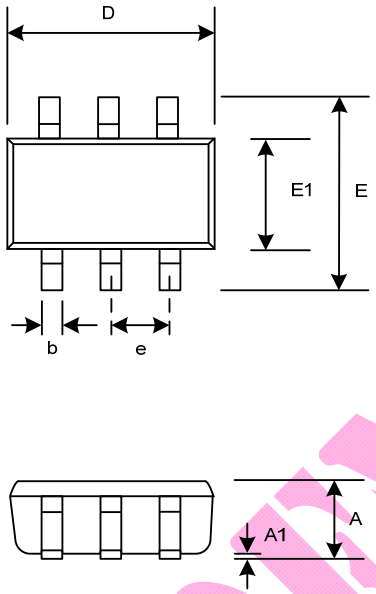
RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE INFORMATION

SOT-26



Symbols	Dimensions			
	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.889	1.450	0.031	0.057
A1	0.000	0.152	0.000	0.006
b	0.250	0.560	0.010	0.022
c	0.080	0.254	0.003	0.010
D	2.692	3.120	0.106	0.123
E	2.591	3.000	0.102	0.118
E1	1.397	1.803	0.055	0.071
e	0.838	1.041	0.033	0.041
L	0.300	0.610	0.012	0.024

DISCLAIMER

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