

PFP15T140 / PFB15T140

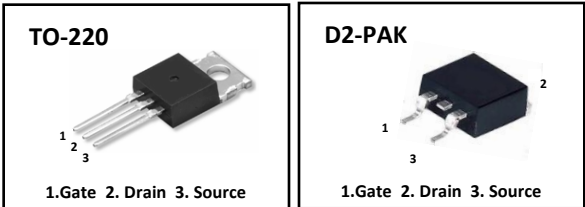
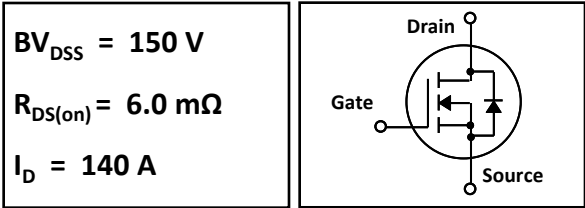
150V N-Channel MOSFET

FEATURES

- 100% EAS Test
- Super high density cell design
- Extremely Low Intrinsic Capacitances
- Remarkable Switching Characteristics
- Extended Safe Operating Area
- Lower $R_{DS(ON)}$: 6.0 mΩ (Typ.) @ $V_{GS}=10V$

APPLICATION

- DC Motor control for E-bike & Power tools
- Amplifier and car booster
- Load Switch
- DC-DC converters



Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	150	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ($T_C = 25^\circ\text{C}$)	140	A
	Continuous Drain Current ($T_C = 100^\circ\text{C}$)	100	A
I_{DM}	Pulsed Drain Current	560	A
E_{AS}	Single Pulsed Avalanche Energy	1296	mJ
P_D	Maximum Power Dissipation ($T_C = 25^\circ\text{C}$)	320	W
	Maximum Power Dissipation ($T_C = 100^\circ\text{C}$)	160	W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.47	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Package Marking and Ordering Information

Marking	Device	Package	Remark
NCEP15T14	PFP15T140	TO-220	RoHS
NCEP15T14D	PFB15T140	TO-263(D2-PAK)	RoHS

Electrical Characteristics $T_c=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Drain-Source On-Static Resistance	$V_{GS} = 10 \text{ V}, I_D = 70 \text{ A}, T_c = 25^\circ\text{C}$	--	6.0	7.2	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 70 \text{ A}$	70	-	-	V

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	150	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	-100	nA
V_{SD}	Diode Forward Voltage	$I_S = 140 \text{ A}, V_{GS} = 0 \text{ V}$	--	--	1.2	V

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS}=75 \text{ V}, V_{GS}=0 \text{ V}, f=1.0 \text{ MHz}$	--	5500	--	pF
C_{oss}	Output Capacitance		--	600	--	pF
C_{rss}	Reverse Transfer Capacitance		--	7	--	pF

Switching Characteristics

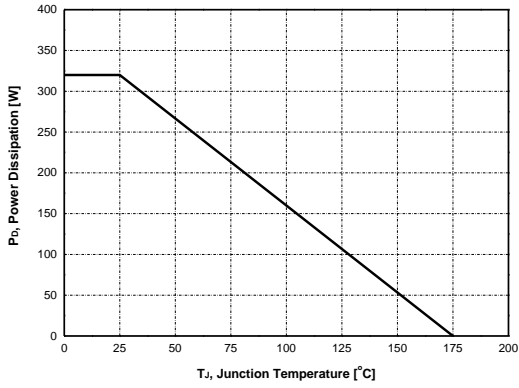
$t_{d(on)}$	Turn-On Time	$V_{DD} = 75 \text{ V}, I_D = 70 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	--	26	--	ns
t_r	Turn-On Rise Time		--	36	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	47	--	ns
t_f	Turn-Off Fall Time		--	15	--	ns
Q_g	Total Gate Charge	$V_{DS}=75 \text{ V}, I_D=70 \text{ A}, V_{GS}=10\text{V}$	--	74	--	nC
Q_{gs}	Gate-Source Charge		--	32	--	nC
Q_{gd}	Gate-Drain Charge		--	11	--	nC

Notes ;

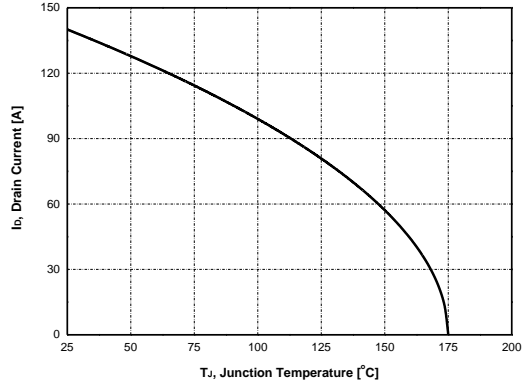
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=0.5\text{mH}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics

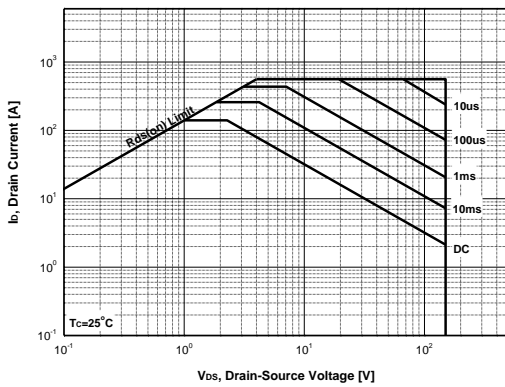
Power Dissipation



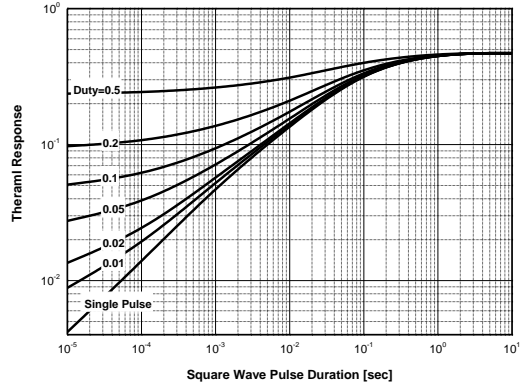
Drain Current



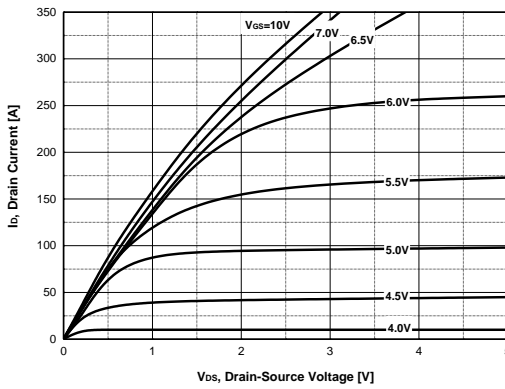
Safe Operation Area



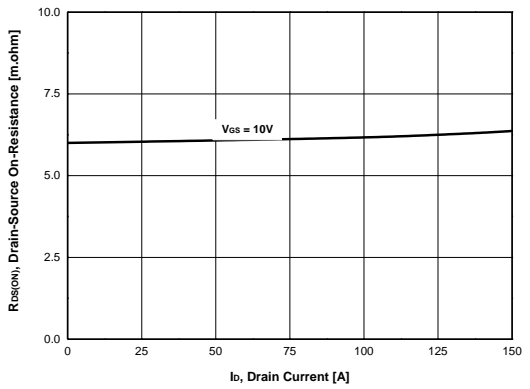
Thermal Transient Impedance



Output Characteristics

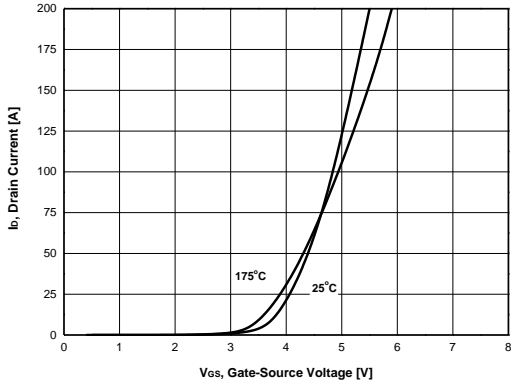


Drain-Source On Resistance

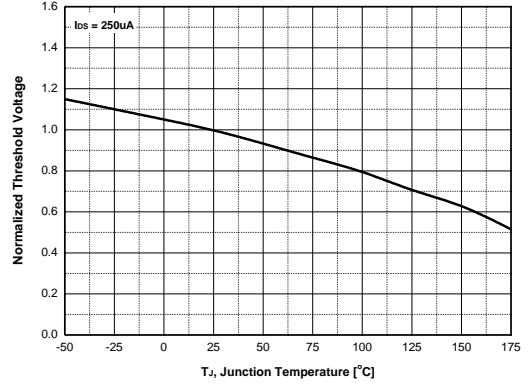


Typical Characteristics (continued)

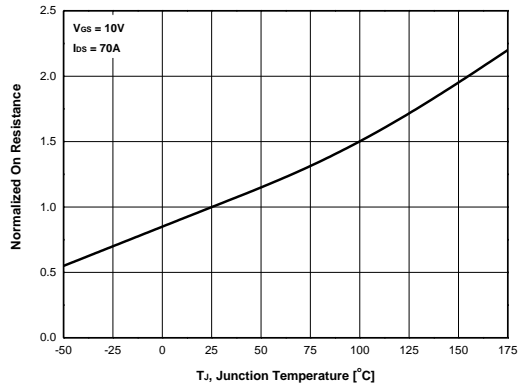
Transfer Characteristics



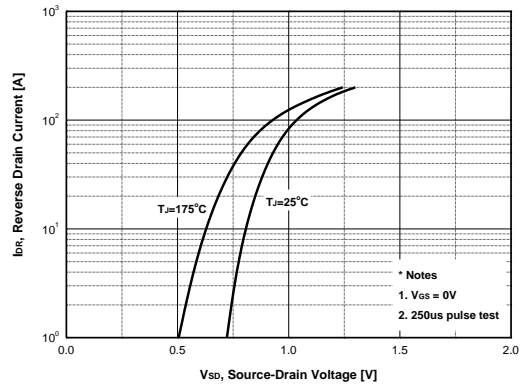
Gate Threshold Voltage



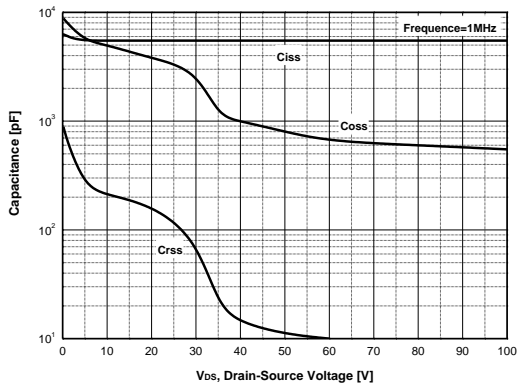
Drain-Source On Resistance



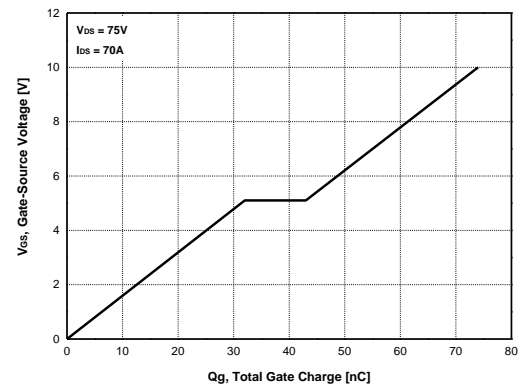
Source-Drain Diode Forward



Capacitance



Gate Charge



Characteristics Test Circuit & Waveform

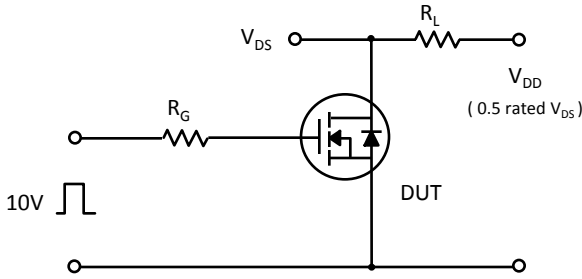


Fig 14. Resistive Switching Test Circuit & Waveforms

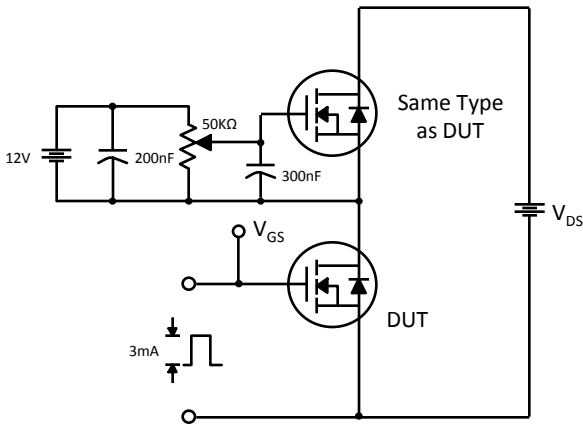
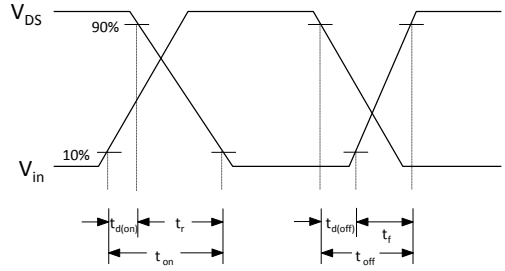


Fig 15. Gate Charge Test Circuit & Waveform

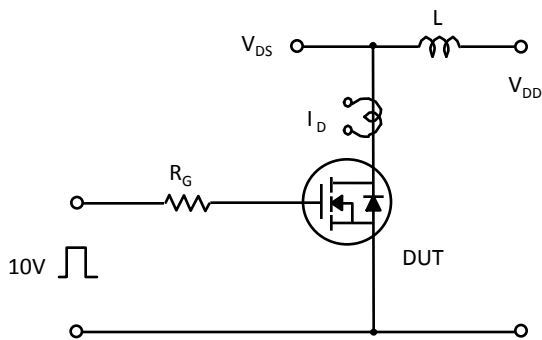
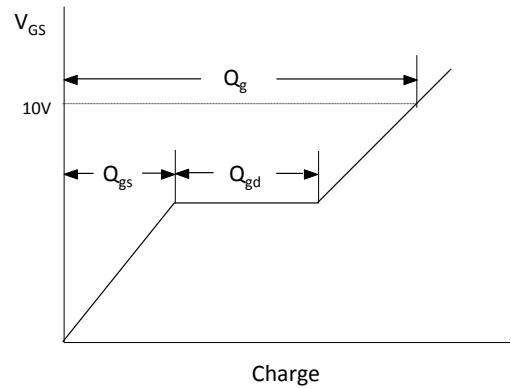
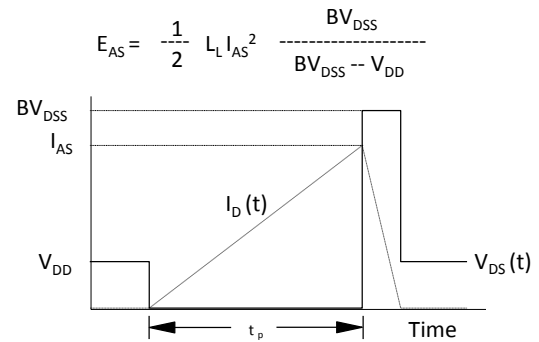


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms



Characteristics Test Circuit & Waveform (continued)

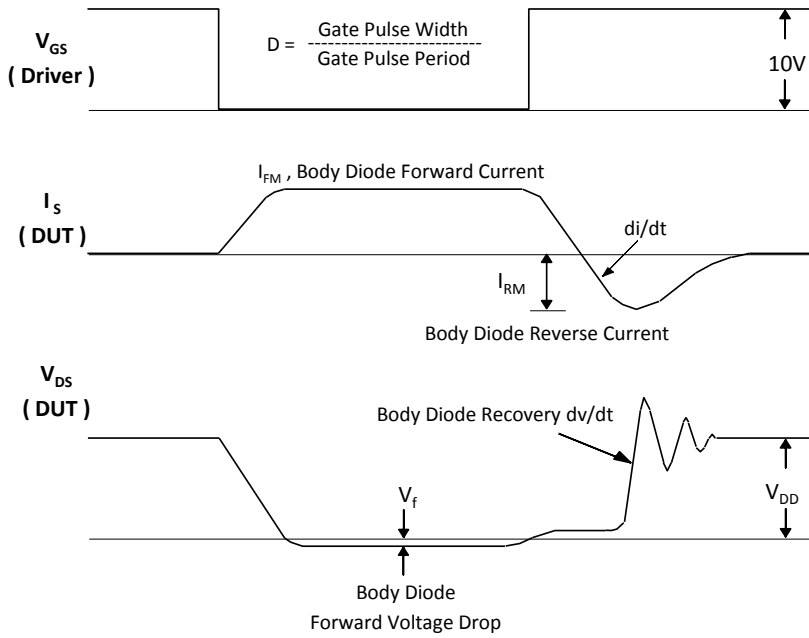
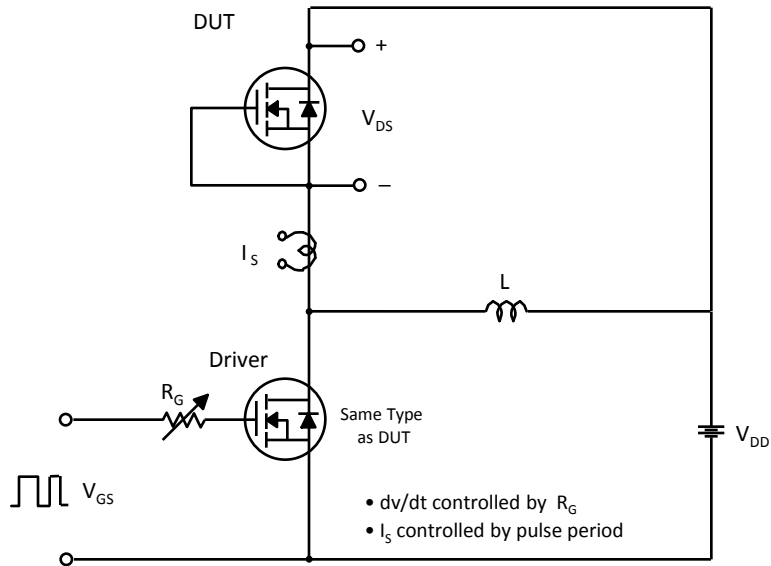


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms