PFU2N65/PFD2N65

650V N-Channel MOSFET

FEATURES

- Originative New Design
- 100% EAS Test
- Rugged Gate Oxide Technology
- Extremely Low Intrinsic Capacitances
- Remarkable Switching Characteristics
- Unequalled Gate Charge : 9.5 nC (Typ.)
- Extended Safe Operating Area
- Lower $R_{DS(ON)}$: 4.2 Ω (Typ.) @V_{GS}=10V

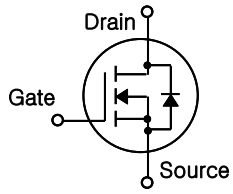
APPLICATION

- Low power battery chargers
- Switch mode power supply (SMPS)
- DC-AC converters.

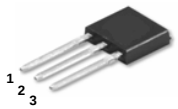
BV_{DSS} = 650 V

$R_{DS(on)\ typ}$ = 4.2 Ω

I_D = 1.8 A



I-PAK(TO-251)



1.Gate 2. Drain 3. Source

D-PAK(TO-252)

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Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		650	V
I_D	Drain Current – Continuous (T_C = 25℃)		1.8	A
	Drain Current – Continuous (T_C = 100℃)		1.1	A
I_{DM}	Drain Current – Pulsed	(Note 1)	6.0	A
V_{GS}	Gate-Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I_{AR}	Avalanche Current	(Note 1)	1.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	5.5	V/ns
P_D	Total Power Dissipation (T_A=25 °C) *		2.5	W
	Power Dissipation (T_C = 25℃)		44	W
	– Derate above 25℃		0.22	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	℃

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.87	℃/W
$R_{\theta JA}$	Junction-to-Ambient*	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics T_C=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.9 A	--	4.2	5.3	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	650	--	--	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to25℃	--	0.6	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 520 V, T_C = 125℃	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	320	420	pF
C_{oss}	Output Capacitance		--	35	46	pF
C_{rss}	Reverse Transfer Capacitance		--	4.5	6.0	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 325 V, I_D = 1.8 A, R_G = 25 Ω (Note 4,5)	--	8	30	ns
t_r	Turn-On Rise Time		--	23	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
t_f	Turn-Off Fall Time		--	28	70	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 1.8 A, V_{GS} = 10 V (Note 4,5)	--	9.5	13	nC
Q_{gs}	Gate-Source Charge		--	1.6	--	nC
Q_{gd}	Gate-Drain Charge		--	4.0	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	1.8	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	6	
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 1.8 A, V_{GS} = 0 V	--	--	1.5	V
trr	Reverse Recovery Time	I_S = 1.8 A, V_{GS} = 0 V di_F/dt = 100 A/μs (Note 4)	--	230	--	ns
Qrr	Reverse Recovery Charge		--	1.0	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=1.8A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. I_{SD}≤1.8A, di/dt≤300A/μs, V_{DD}≤BV_{DSS} , Starting T_J=25 °C
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

Typical Characteristics

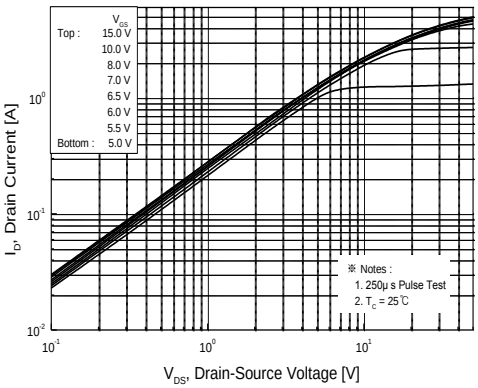


Figure 1. On Region Characteristics

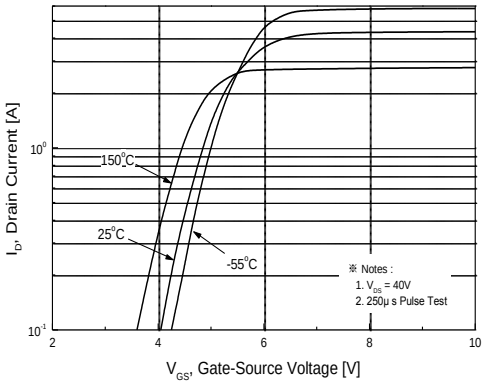


Figure 2. Transfer Characteristics

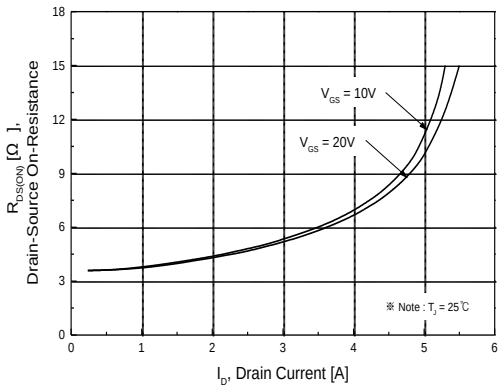


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

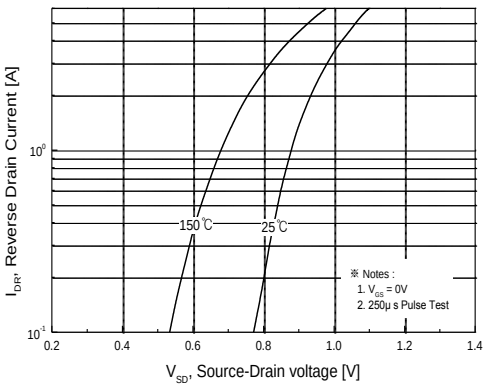


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

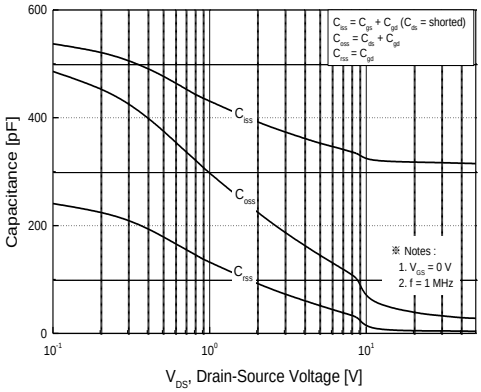


Figure 5. Capacitance Characteristics

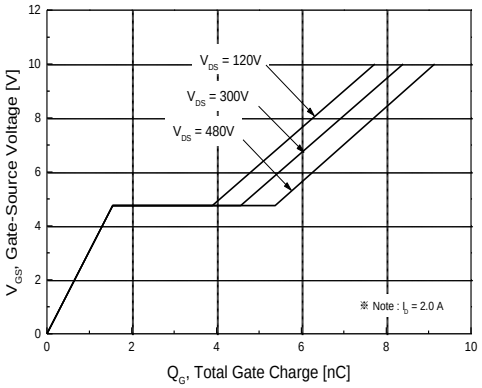


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

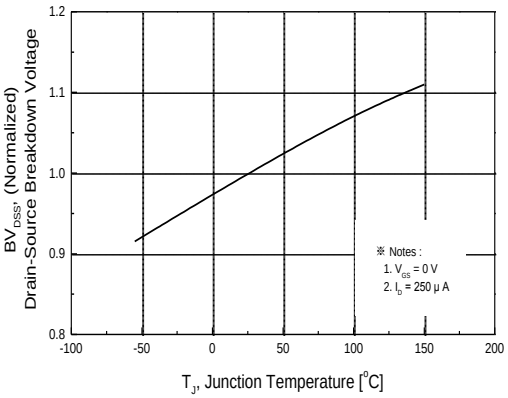


Figure 7. Breakdown Voltage Variation vs Temperature

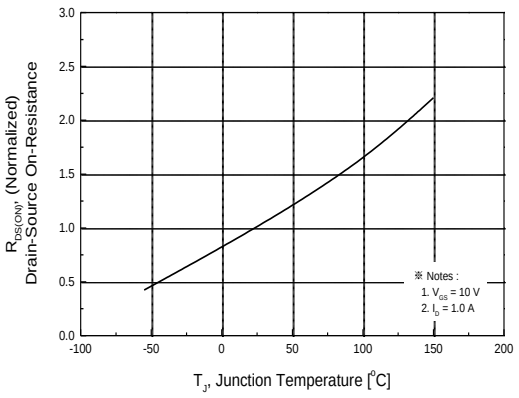


Figure 8. On-Resistance Variation vs Temperature

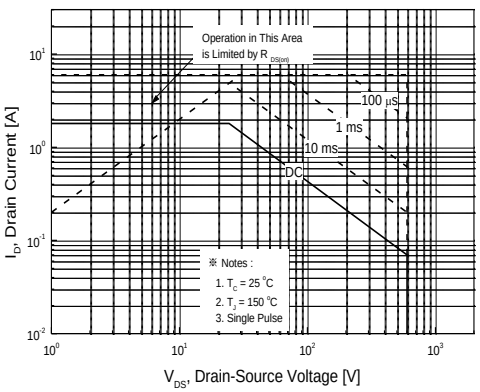


Figure 9. Maximum Safe Operating Area

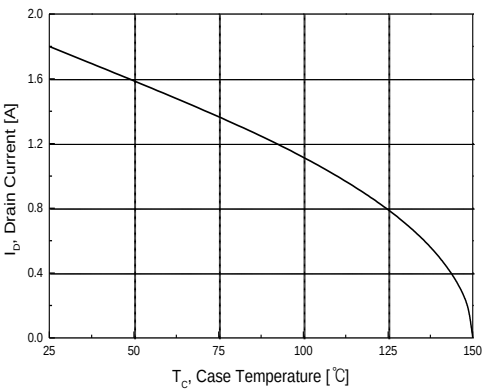


Figure 10. Maximum Drain Current vs Case Temperature

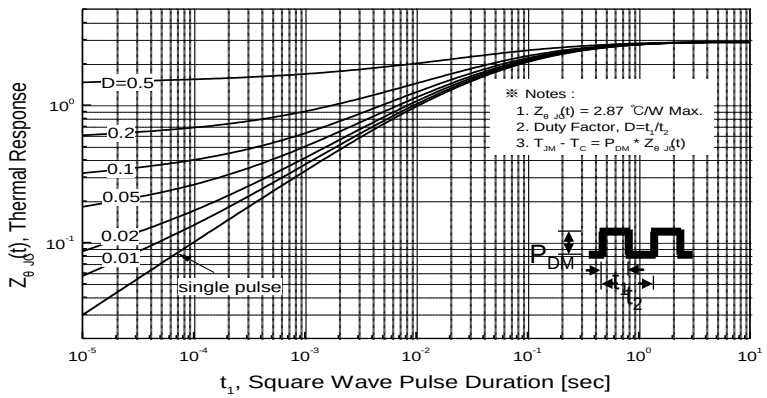


Figure 11. Transient Thermal Response Curve

Characteristics Test Circuit & Waveform

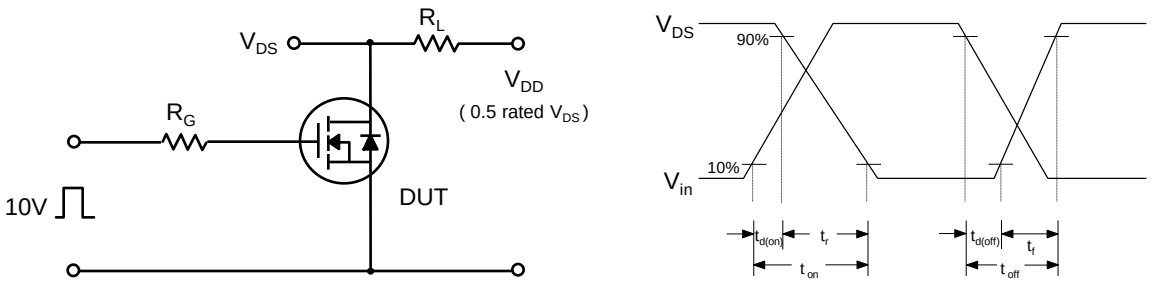


Fig 14. Resistive Switching Test Circuit & Waveforms

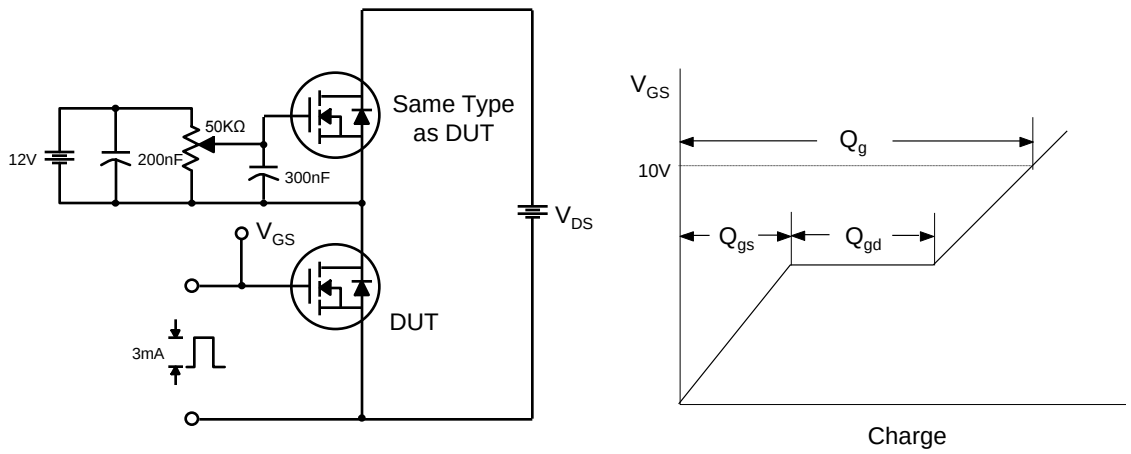


Fig 15. Gate Charge Test Circuit & Waveform

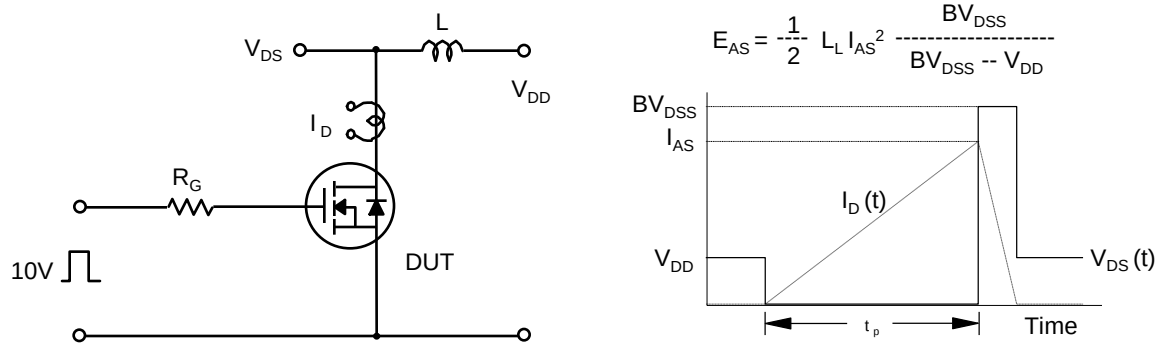
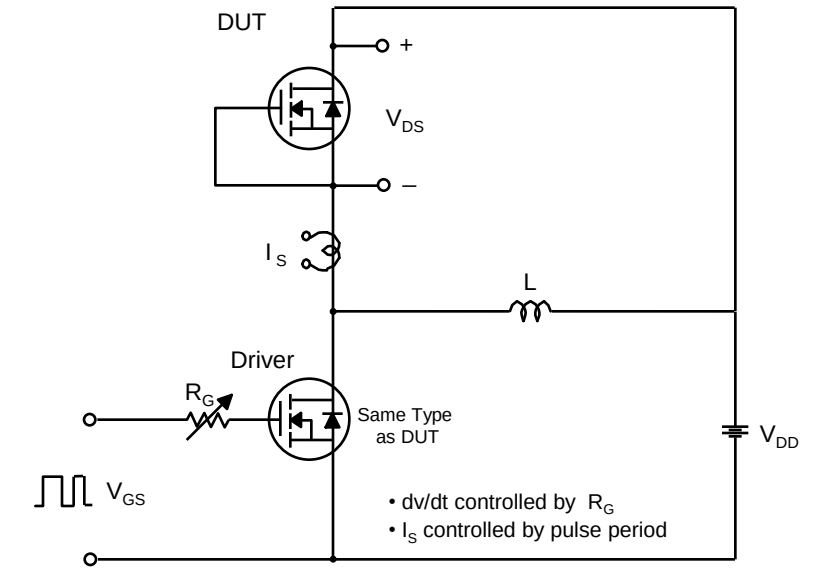


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)



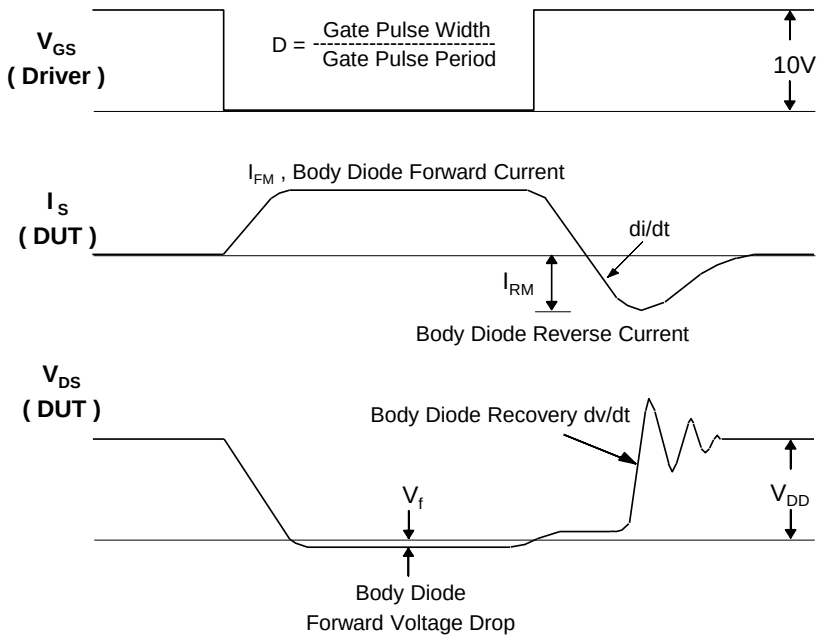
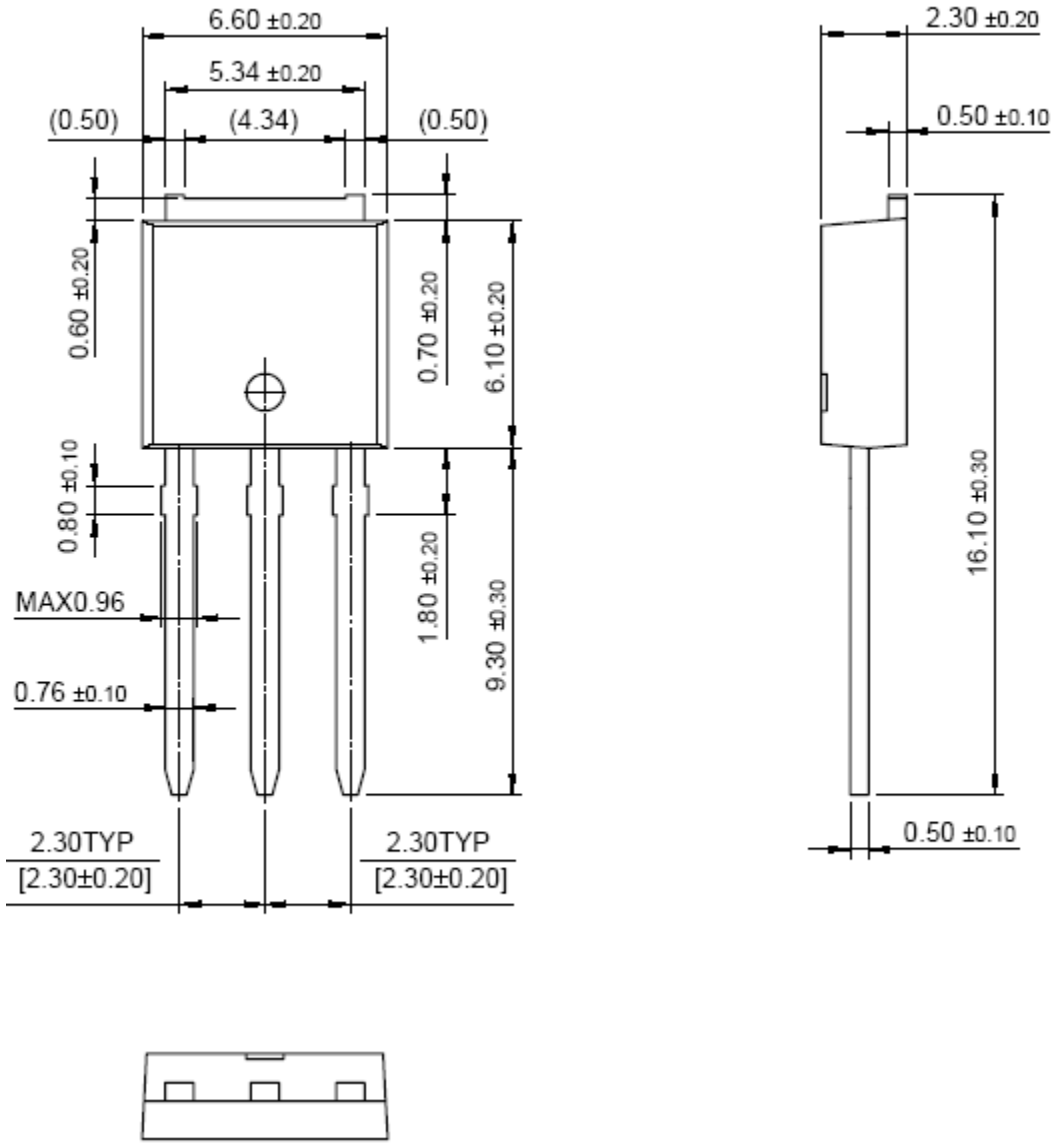


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

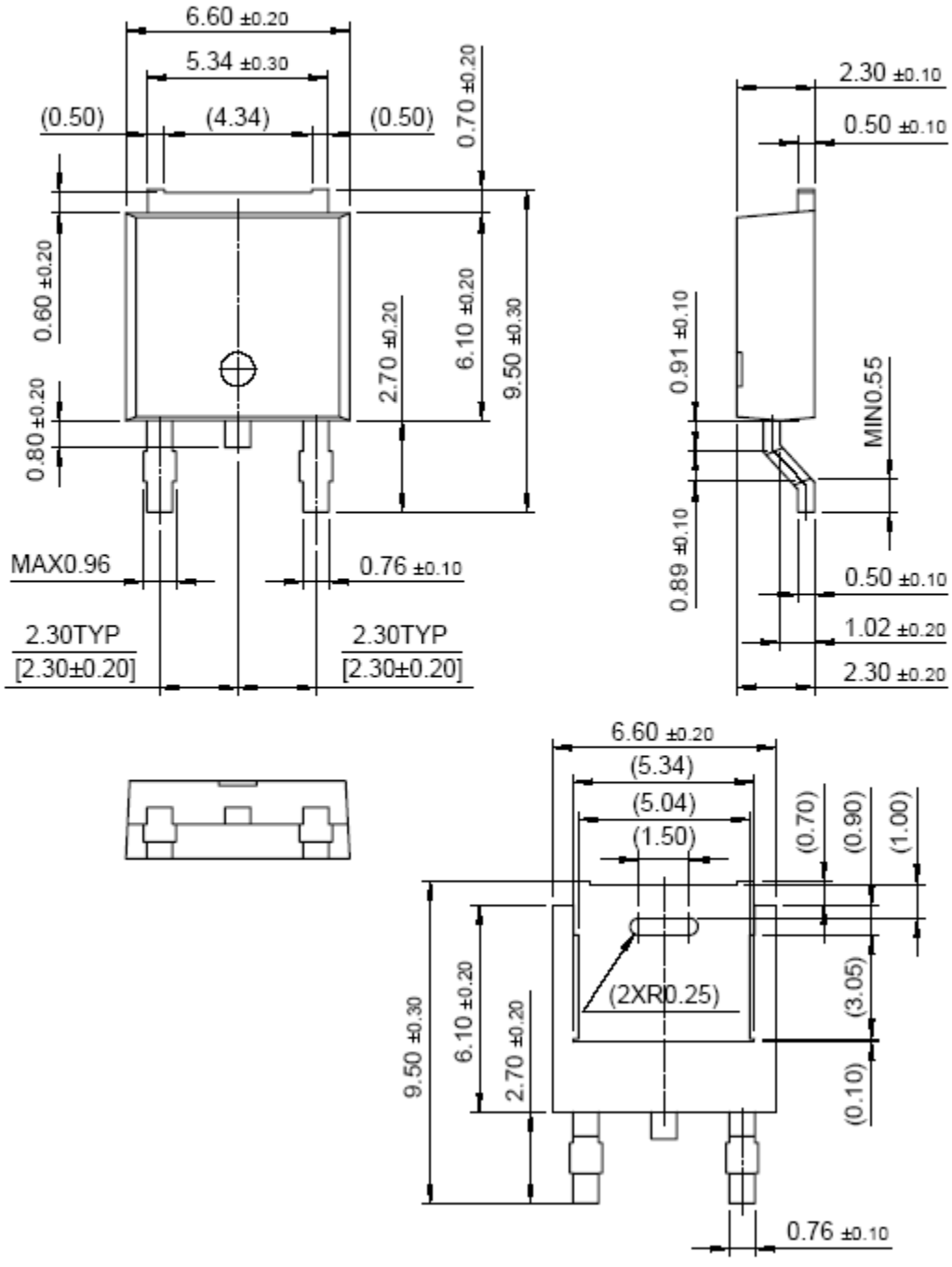
Package Dimension

IPAK



Package Dimension

DPAK



Reliability Qualification

A. High Temperature Reverse Bias (HTRB)

The purpose of this test is to determine the sensitivity of the product to mobile ion contamination and related failure mechanisms.

Conditions: MIL-STD-750C 1038, JIS C 7021 B-3

T_A=150℃ V_{DS}=80% max rated V_{DS}

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

B. High Temperature Gate Bias (HTGB)

The purpose of this test is to determine the sensitivity of the product to mobile ion contamination between gate and source and related failure mechanisms.

Conditions: MIL-STD-750C 1038, JIS C 7021 B-3

T_A=150℃ V_{DS}= V_{GSS} max

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

C. Temperature Humidity Bias (THB)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components.

The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place. with time, this is a catastrophically destructive test.

Conditions: JESD22-A101, JIS C 7021 B-11

T_A=85℃ RH=85% V_{DS}=80% max rated V_{DS}

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

Reliability Qualification (Continued)

D. High Temperature Storage (HTS)

The purpose of this test is to expose time/temperature failure mechanisms and to evaluate long-term strong stability.

Conditions: MIL-STD-750C 1031.4, JIS C 7021 B-10

$T_A=T_{stg}$(max) 150 ℃

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

E. Pressure Cooker Test (PCT)

Autoclave (ACLV)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: MIL-STD-750C 1071.2, JIS C 7021 A-6

T_A=121℃±2℃ RH=100% P=1 atmosphere (15psig)

Sample Size	#of Fail	Cum. Fail%	48hrs
22	0	0.0%	0

F. Temperature Cycle Air-to Air (T/C)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperature and the transition between temperature extreme, and to exposure excessive thermal mismatch between materials.

Conditions: JESD22-A104, JIS C 7021 A-4

Air to air, −65℃~150℃, 10 minutes dwell time at each temperature

Sample Size	#of Fail	Cum. Fail%	100cycles	200cycles
22	0	0.0%	0	0