Green Package

PFU6N40EG/PFD6N40EG

400V N-Channel MOSFET

FEATURES

- Originative New Design
- 100% EAS Test
- Rugged Gate Oxide Technology
- Extremely Low Intrinsic Capacitances
- Remarkable Switching Characteristics
- Unequalled Gate Charge : 10.5 nC (Typ.)
- Extended Safe Operating Area
- Lower $R_{DS(ON)}$: 0.7 Ω (Typ.) @V_{GS}=10V

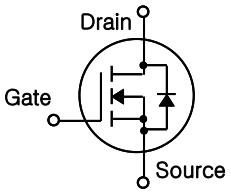
APPLICATION

- Electronic lamp ballasts based on half bridge topology
- PFC (Power Factor Correction)
- SMPS (Switched Mode Power Supplies)

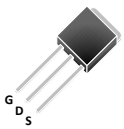
BV_{DSS} = 400 V

$R_{DS(ON)}$ = 0.7 Ω

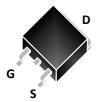
I_D = 4.8 A



I-PAK(TO-251)



D-PAK(TO-252)



Absolute Maximum Ratings

T_C=25°C unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	400	V
I_D	Drain Current – Continuous (T_C = 25°C)	4.8	A
	Drain Current – Continuous (T_C = 100°C)	3.1	A
I_{DM}	Drain Current – Pulsed (Note 1)	19.3	A
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	270	mJ
I_{AR}	Avalanche Current (Note 1)	6.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation (T_C = 25°C)	50	W
	- Derate above 25°C)	0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\Theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	°C/W
$R_{\Theta CS}$	Thermal Resistance, Case-to-Sink	--	50	
$R_{\Theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	

Electrical Characteristics T_C=25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.5	--	4.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.0 A	--	0.7	0.95	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	400	--	--	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25°C	--	0.4	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 400 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 320 V, T_C = 125°C	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	580	754	pF
C_{oss}	Output Capacitance		--	80	104	pF
C_{rss}	Reverse Transfer Capacitance		--	6	15	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 200 V, I_D = 6.0 A, R_G = 25 Ω (Note 4,5)	--	13.5	27	ns
t_r	Turn-On Rise Time		--	6.6	13	ns
$t_{d(off)}$	Turn-Off Delay Time		--	27	54	ns
t_f	Turn-Off Fall Time		--	5.5	11	ns
Q_g	Total Gate Charge	V_{DS} = 320V, I_D = 6.0 A, V_{GS} = 10 V (Note 4,5)	--	10.5	15	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		--	3.9	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	6.0	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	24	
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 6.0 A, V_{GS} = 0 V	--	--	1.5	V
trr	Reverse Recovery Time	I_S = 6.0 A, V_{GS} = 0 V di_F/dt = 100 A/μs (Note 4)	--	200	--	nS
Qrr	Reverse Recovery Charge		--	1.1	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=6.0A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. I_{SD}≤6.0A, di/dt≤300A/as, V_{DD}≤BV_{DSS}, Starting T_J=25°C
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

Typical Characteristics

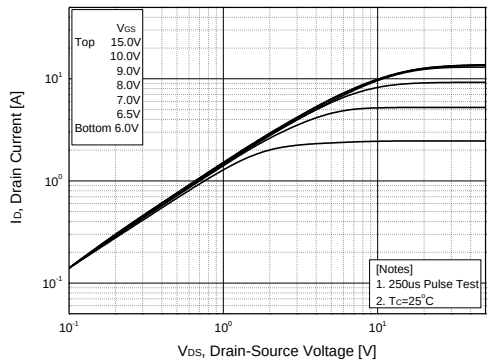


Figure 1. On Region Characteristics

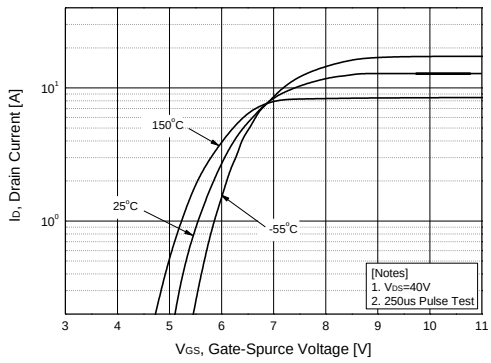


Figure 2. Transfer Characteristics

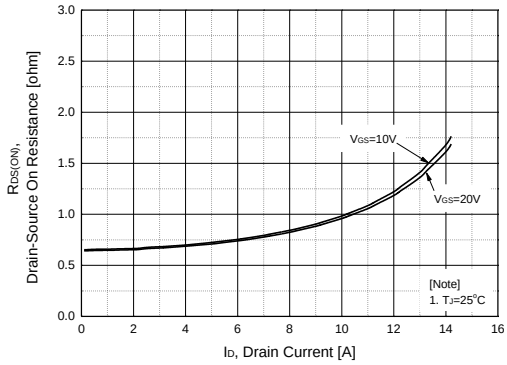


Figure 3. On Resistance Variation vs. Drain Current and Gate Voltage

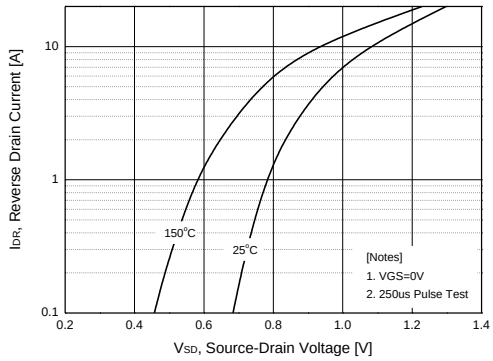


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

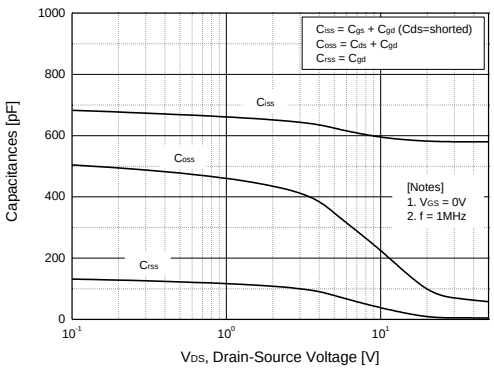


Figure 5. Capacitance Characteristics

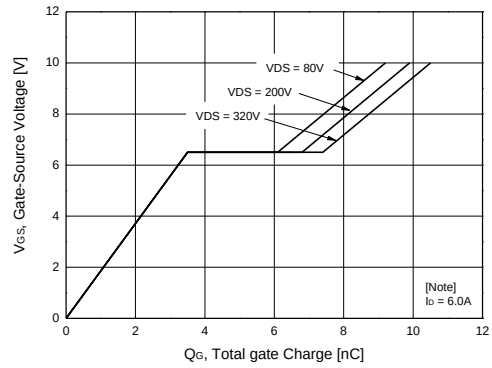


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

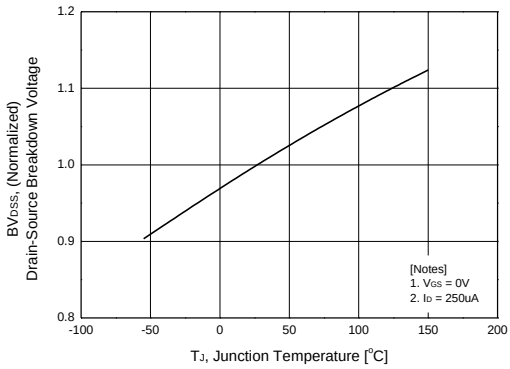


Figure 7. Breakdown Voltage Variation vs Temperature

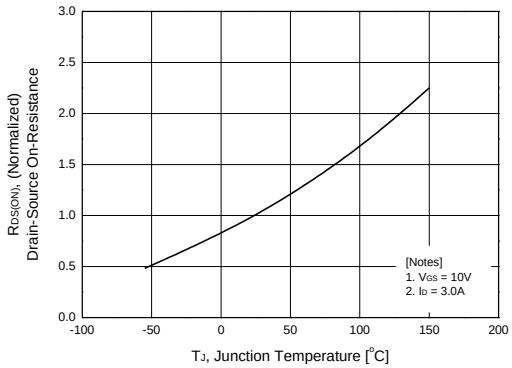


Figure 8. On-Resistance Variation vs Temperature

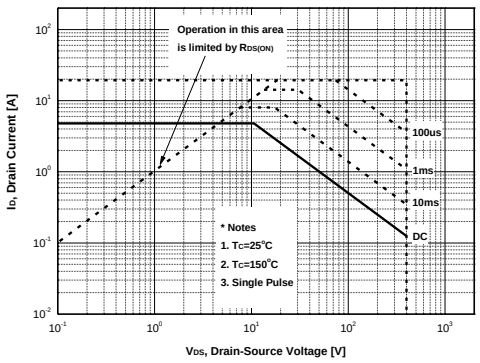


Figure 9. Maximum Safe Operating Area

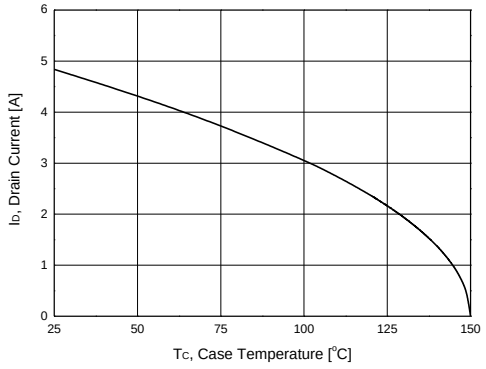


Figure 10. Maximum Drain Current vs. Case Temperature

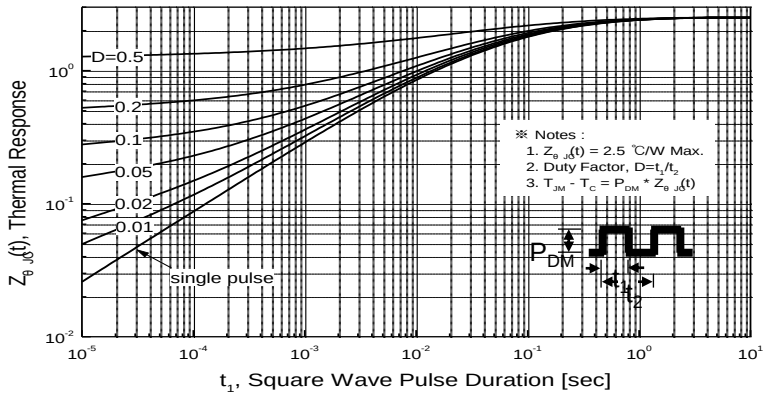


Figure 11. Transient Thermal Response Curve

Characteristics Test Circuit & Waveform

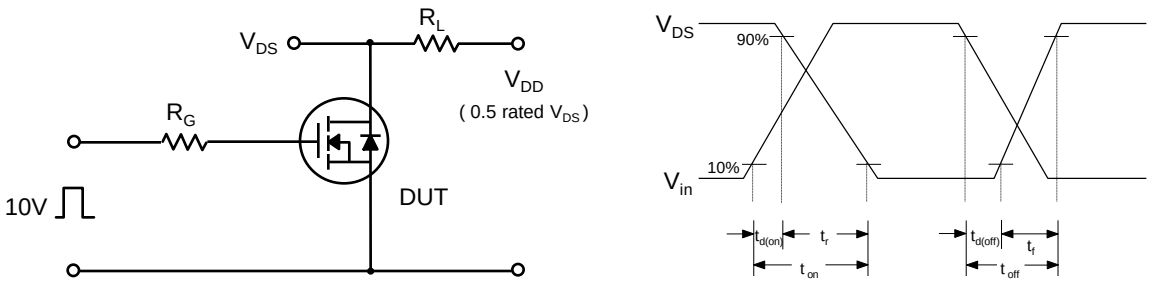


Fig 14. Resistive Switching Test Circuit & Waveforms

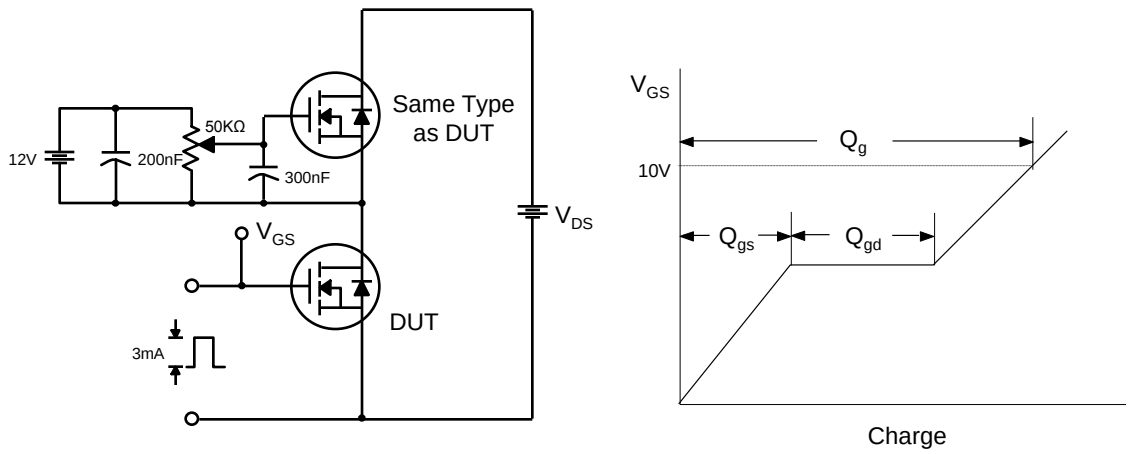


Fig 15. Gate Charge Test Circuit & Waveform

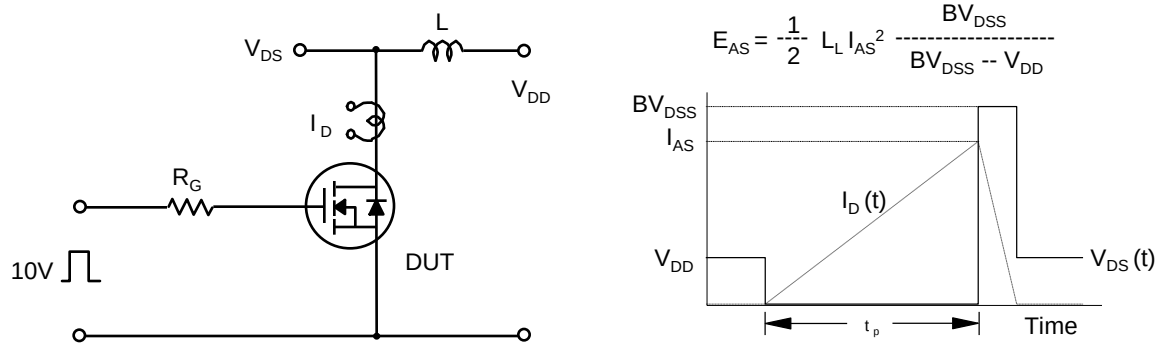


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)

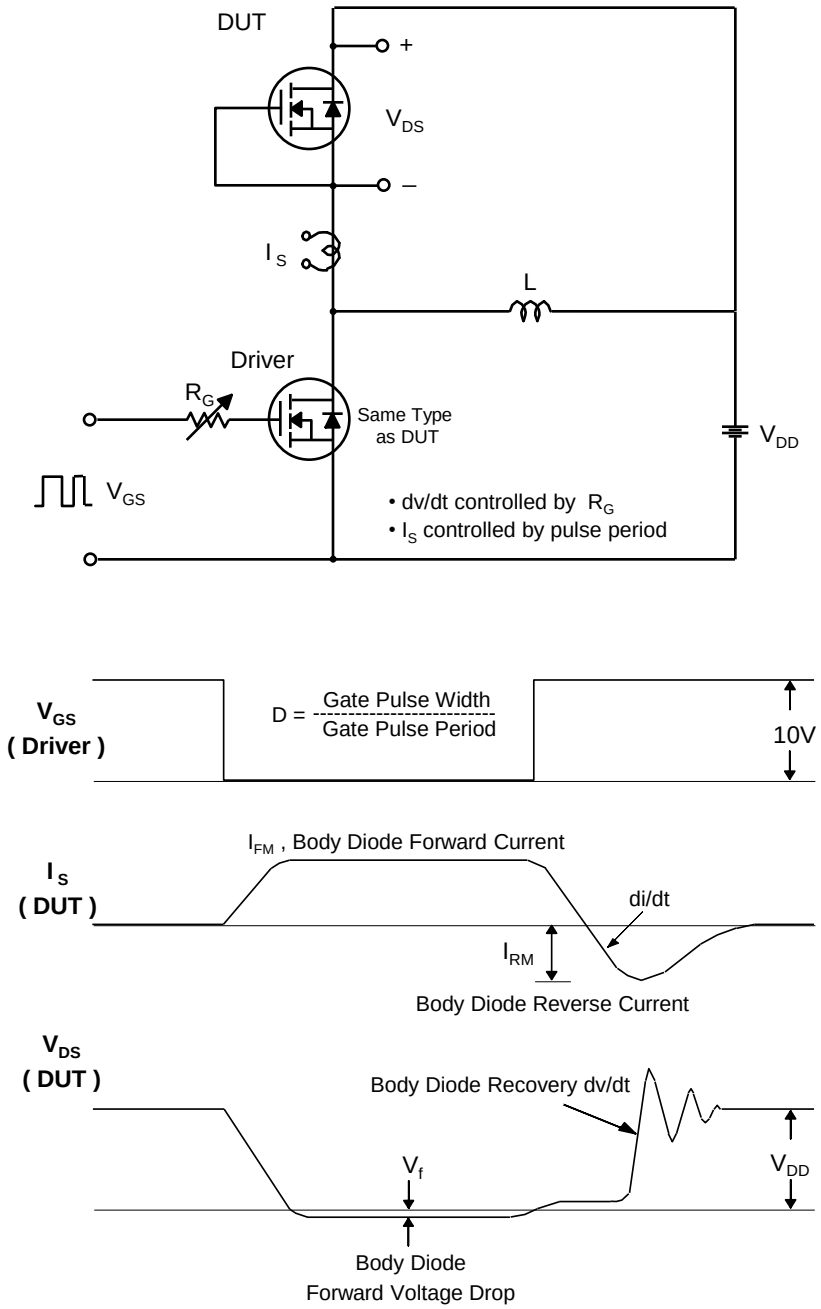
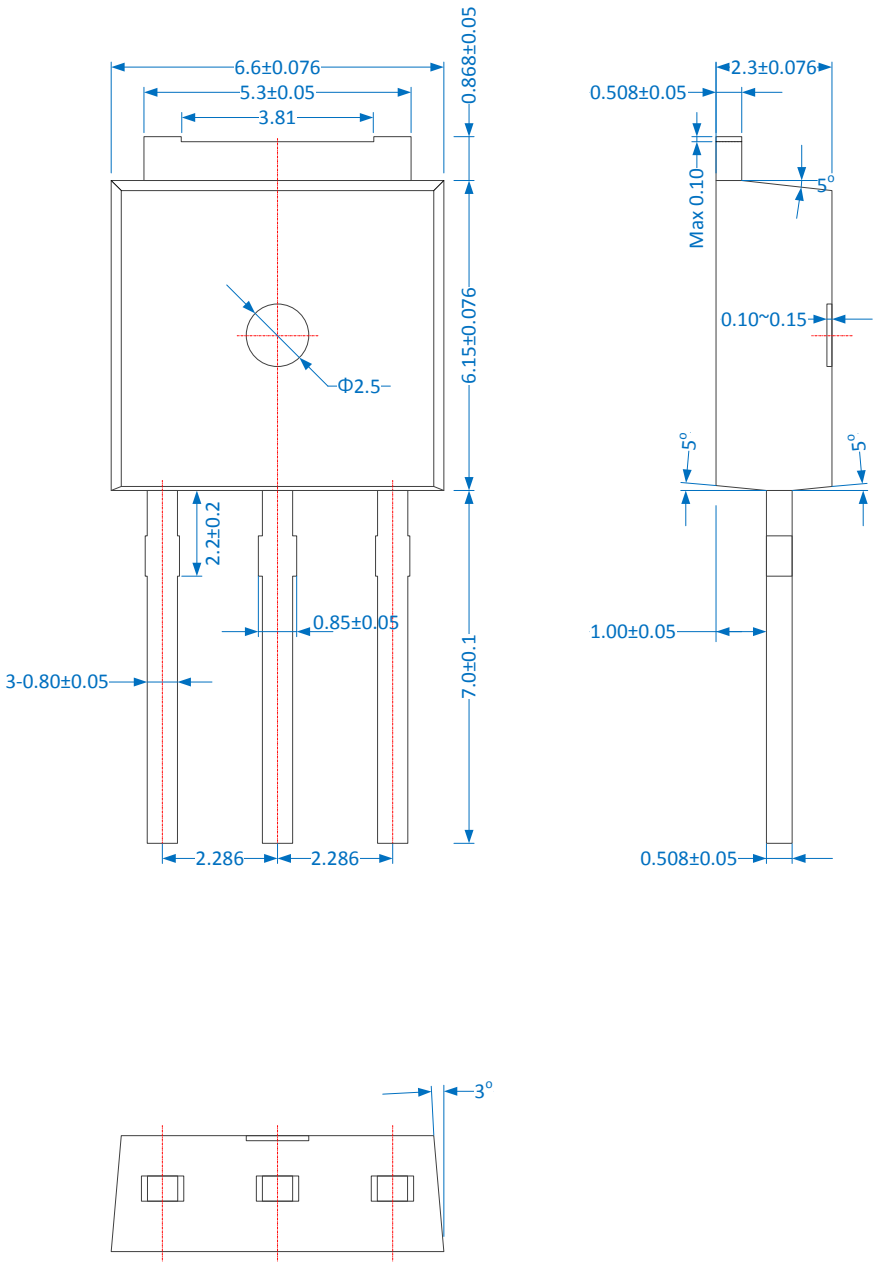


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Package Dimension

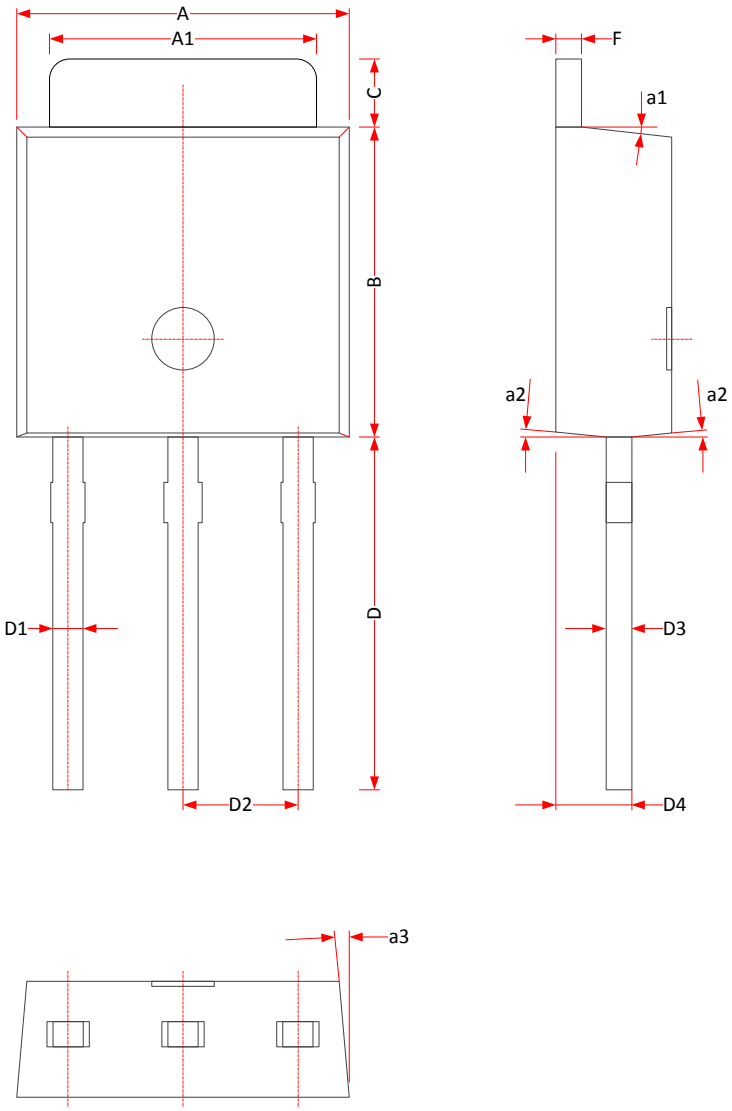
I-PAK(TO-251) ⓩ



Package Dimension

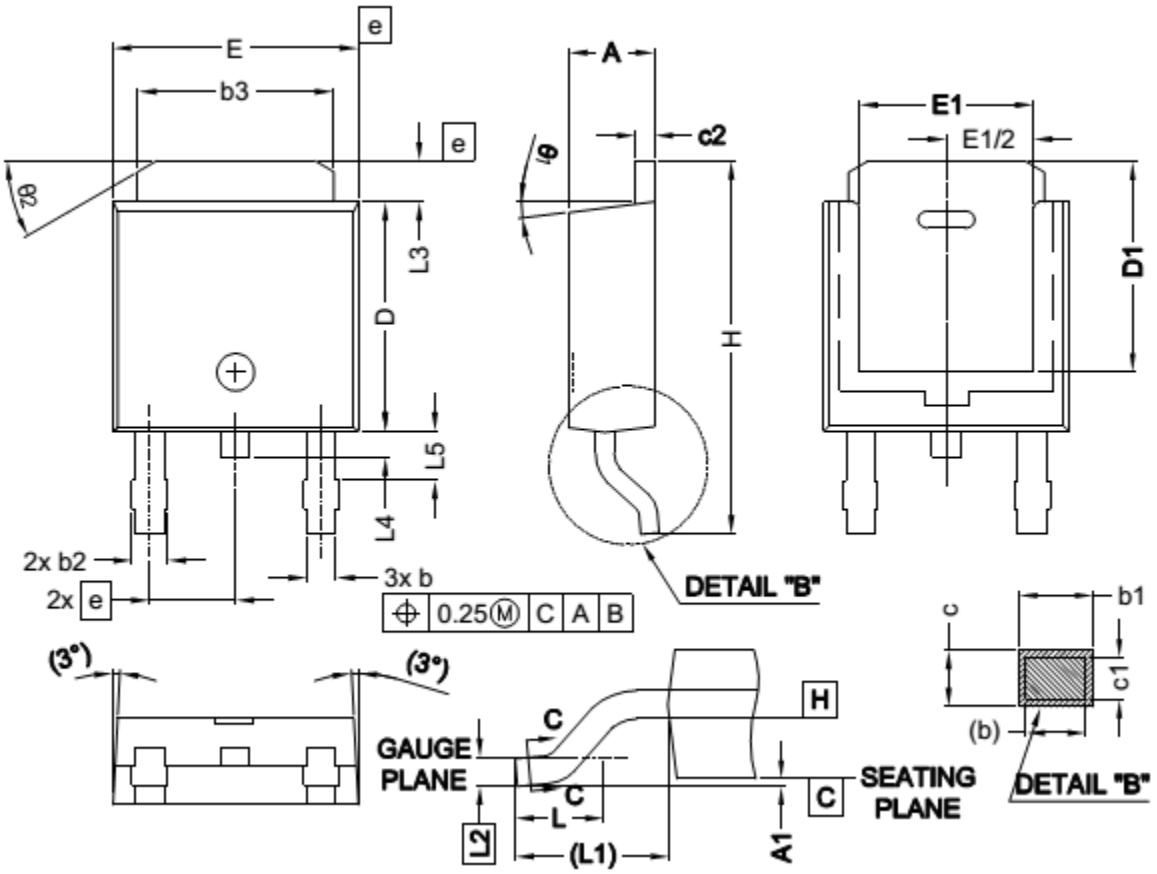
I-PAK(TO-251) ⓗ

Symbol	Millimeters
A	6.40 ~ 6.60
A1	5.30 ~ 5.50
B	5.40 ~ 5.70
C	1.35 ~ 1.65
D	7.40 ~ 8.00
D1	0.60 ~ 0.75
D2	2.30
D3	0.49 ~ 0.59
D4	1.72 ~ 1.82
E	2.20 ~ 2.40
F	0.55 ~ 0.65
a1	5 deg
a2	5 deg
a3	2 deg



Package Dimension

D-PAK(TO-252) ⓐ



SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	ϕ1	0°	15°
A1	-	0.13	E1	4.32	-	ϕ2	25°	35°
b	0.640	0.884	e	2.29 BSC				
b1	0.65	0.79	H	9.94	10.34			
b2	0.760	1.124	L	1.50	1.78			
b3	4.95	5.46	L1	2.74 REF				
c	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.40	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.140	1.492			
D1	5.21	-	ϕ	0°	10°			

Package Dimension

D-PAK(TO-252) ⓩ