

FQP18N50V2/FQPF18N50V2 500V N-Channel MOSFET

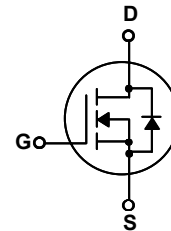
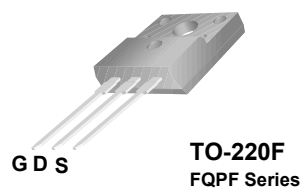
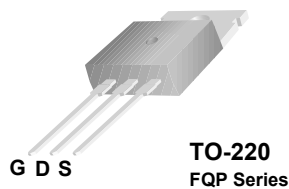
Features

- 550V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 0.265\Omega$ @ $V_{GS} = 10\text{V}$
- Low gate charge (typical 42 nC)
- Low C_{rss} (typical 11 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



Absolute Maximum Ratings

| Symbol | Parameter | FQP18N50V2 | FQPF18N50V2 | Units |
|----------------|---|--|-------------|------------------|
| V_{DSS} | Drain-Source Voltage | 500 | | V |
| I_D | Drain Current | - Continuous ($T_C = 25^\circ\text{C}$) | 18 | 18* |
| | | - Continuous ($T_C = 100^\circ\text{C}$) | 12.1 | 12.1* |
| I_{DM} | Drain Current - Pulsed (Note 1) | 72 | 72* | A |
| V_{GSS} | Gate-Source Voltage | ± 30 | | V |
| E_{AS} | Single Pulsed Avalanche Energy (Note 2) | 330 | | mJ |
| I_{AR} | Avalanche Current (Note 1) | 18 | | A |
| E_{AR} | Repetitive Avalanche Energy (Note 1) | 25 | | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 4.5 | | V/ns |
| P_D | Power Dissipation ($T_C = 25^\circ\text{C}$) | 208 | 69 | W |
| | | - Derate above 25°C | 1.67 | 0.55 |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | | $^\circ\text{C}$ |
| T_L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | FQP18N50V2 | FQPF18N50V2 | Units |
|-----------------|---|------------|-------------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.6 | 1.8 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink | 0.5 | -- | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 62.5 | 62.5 | $^\circ\text{C}/\text{W}$ |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|-------------|---------|-----------|------------|----------|
| PV218N50 | FQP18N50V2 | TO-220 | - | - | 50 |
| PFV218N50 | FQPF18N50V2 | TO-220F | - | - | 50 |

Electrical Characteristics T_C = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|--|------|-------|-------|-------|
| Off Characteristics | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} = 0 V, I _D = 250 μA | 500 | -- | -- | V |
| ΔBV _{DSS} /ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 250 μA, Referenced to 25°C | -- | 0.5 | -- | V/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 500 V, V _{GS} = 0 V | -- | -- | 1 | μA |
| | | V _{DS} = 400 V, T _C = 125°C | -- | -- | 10 | μA |
| I _{GSSF} | Gate-Body Leakage Current, Forward | V _{GS} = 30 V, V _{DS} = 0 V | -- | -- | 100 | nA |
| I _{GSSR} | Gate-Body Leakage Current, Reverse | V _{GS} = -30 V, V _{DS} = 0 V | -- | -- | -100 | nA |
| On Characteristics | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 250 μA | 3.0 | -- | 5.0 | V |
| R _{DS(on)} | Static Drain-Source On-Resistance | V _{GS} = 10 V, I _D = 9 A | -- | 0.225 | 0.265 | Ω |
| g _{FS} | Forward Transconductance | V _{DS} = 40 V, I _D = 9 A (Note 4) | -- | 16 | -- | S |
| Dynamic Characteristics | | | | | | |
| C _{iss} | Input Capacitance | V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz | -- | 2530 | 3290 | pF |
| C _{oss} | Output Capacitance | | -- | 300 | 390 | pF |
| C _{riss} | Reverse Transfer Capacitance | | -- | 11 | 14.3 | pF |
| C _{oss} | Output Capacitance | V _{DS} = 400 V, V _{GS} = 0 V, f = 1.0 MHz | -- | 76 | -- | pF |
| C _{oss eff.} | Effective Output Capacitance | V _{DS} = 0V to 400 V, V _{GS} = 0 V | -- | 150 | -- | pF |
| Switching Characteristics | | | | | | |
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 250 V, I _D = 18 A, R _G = 25 Ω (Note 4, 5) | -- | 40 | 90 | ns |
| t _r | Turn-On Rise Time | | -- | 150 | 310 | ns |
| t _{d(off)} | Turn-Off Delay Time | | -- | 95 | 200 | ns |
| t _f | Turn-Off Fall Time | | -- | 110 | 230 | ns |
| Q _g | Total Gate Charge | V _{DS} = 400 V, I _D = 18 A, V _{GS} = 10 V (Note 4, 5) | -- | 42 | 55 | nC |
| Q _{gs} | Gate-Source Charge | | -- | 12 | -- | nC |
| Q _{gd} | Gate-Drain Charge | | -- | 14 | -- | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| I _S | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 18 | A |
| I _{SM} | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 72 | A |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0 V, I _S = 18 A | -- | -- | 1.4 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0 V, I _S = 18 A, di _F / dt = 100 A/μs (Note 4) | -- | 420 | -- | ns |
| Q _{rr} | Reverse Recovery Charge | | -- | 5.4 | -- | μC |

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 1.83mH, I_{AS} = 18A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 18A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

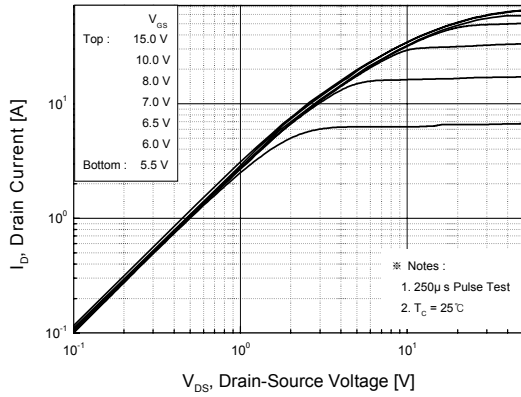


Figure 2. Transfer Characteristics

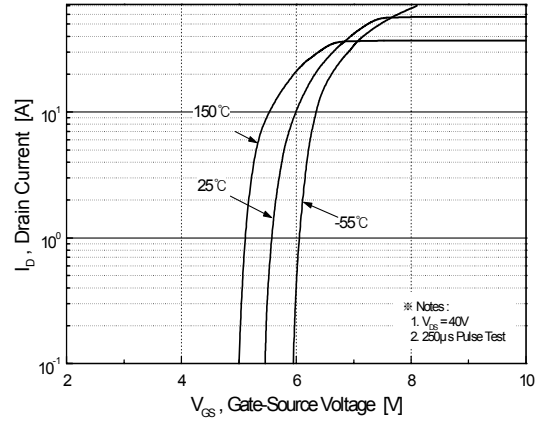


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

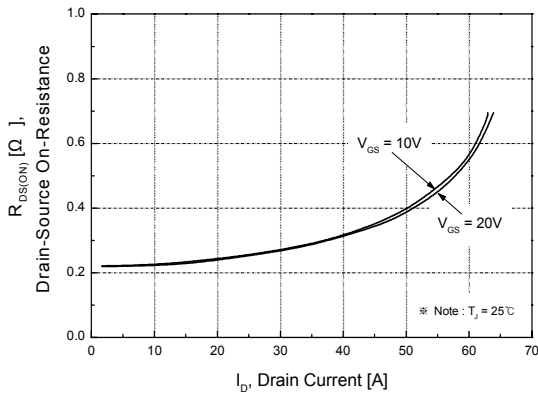


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

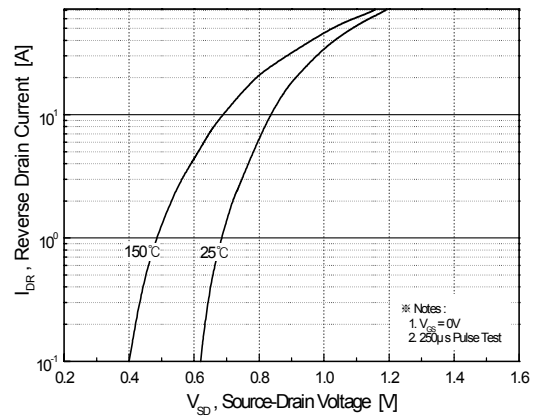


Figure 5. Capacitance Characteristics

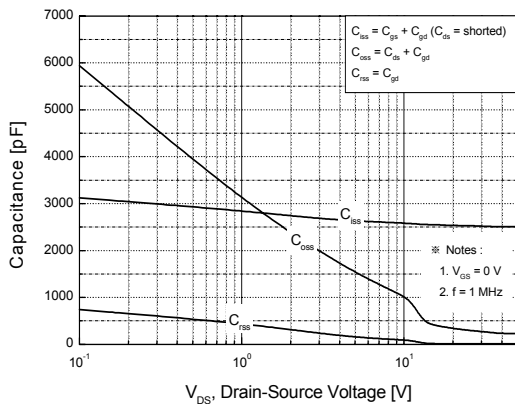
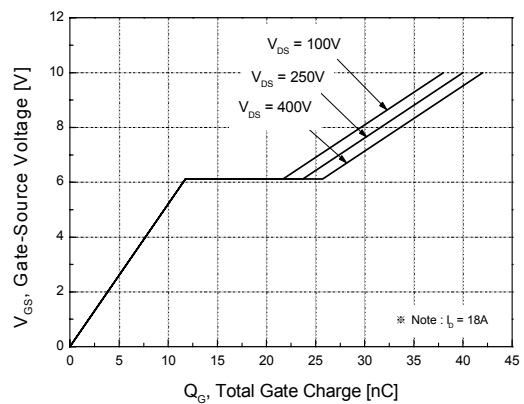


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

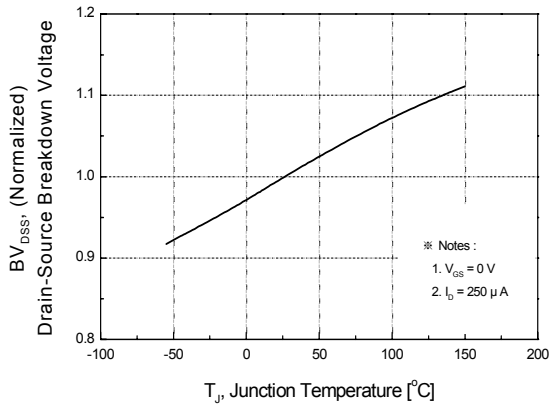


Figure 8. On-Resistance Variation vs. Temperature

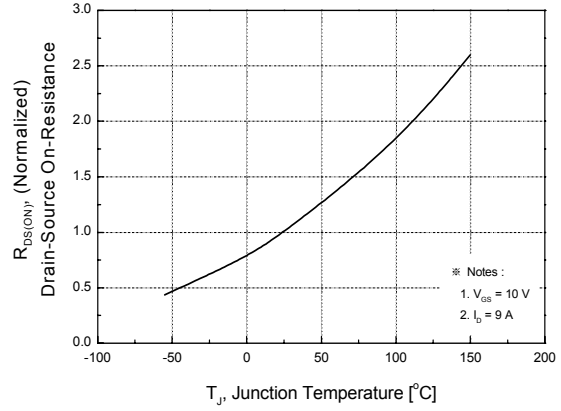


Figure 9-1. Maximum Safe Operating Area for FQP18N50V2

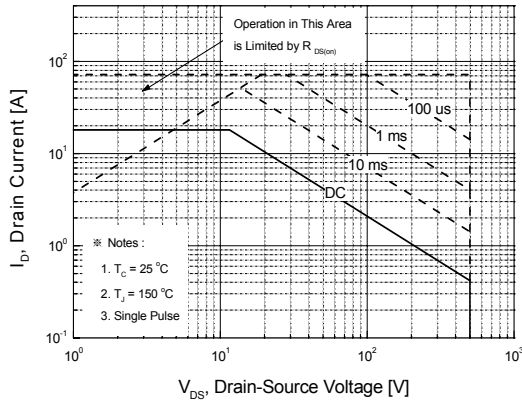


Figure 9-2. Maximum Safe Operating Area for FQPF18N50V2

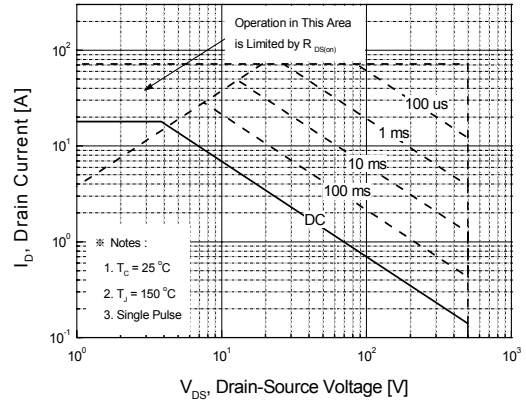
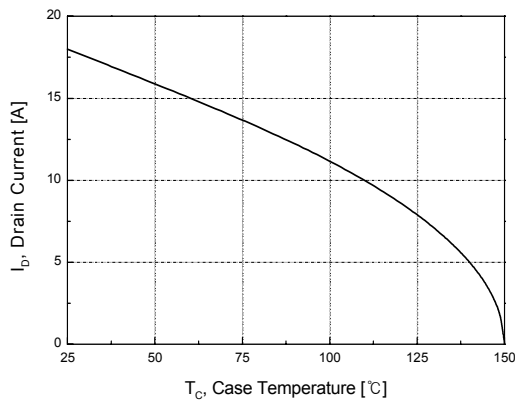


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FQP18N50V2

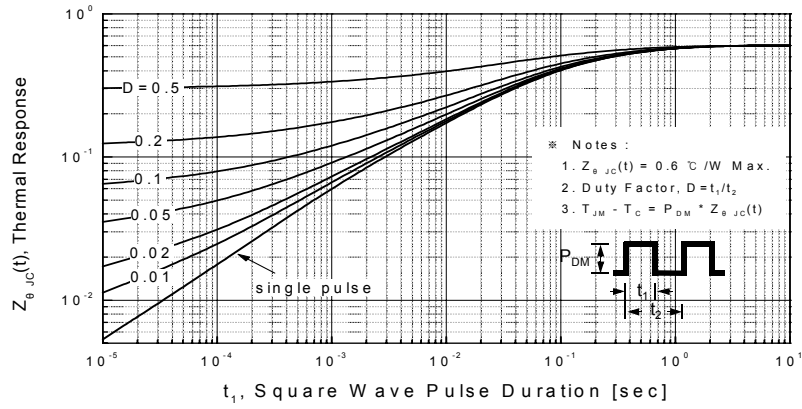
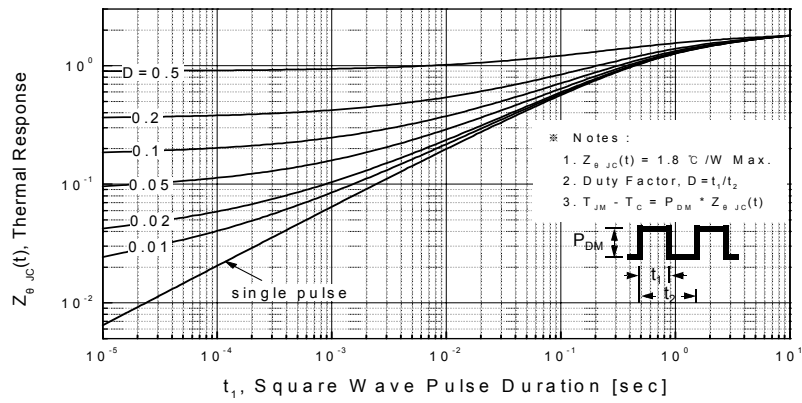
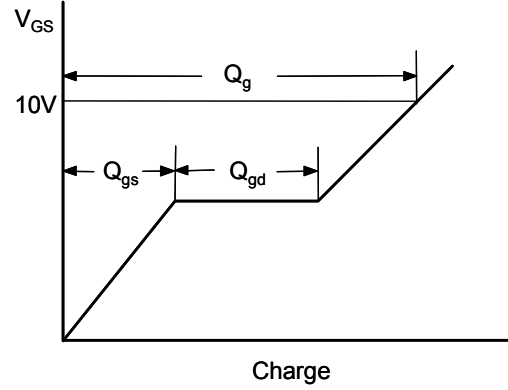
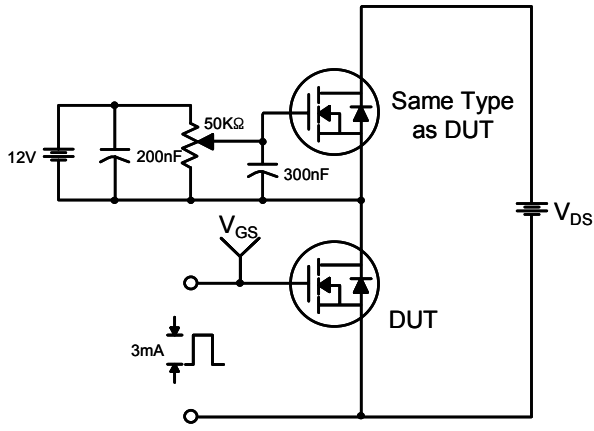


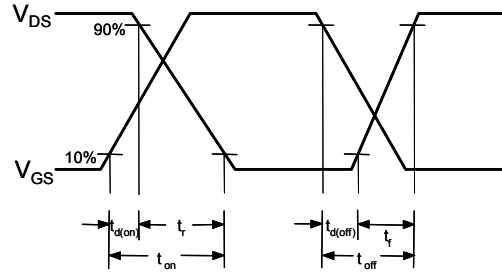
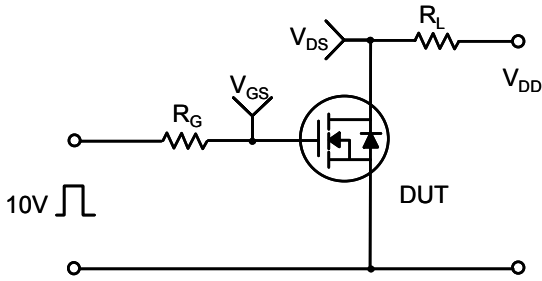
Figure 11-2. Transient Thermal Response Curve for FQPF18N50V2



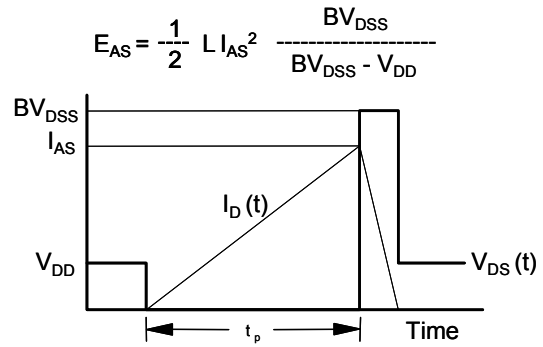
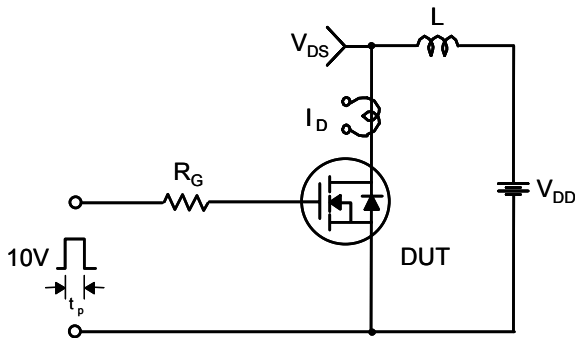
Gate Charge Test Circuit & Waveform



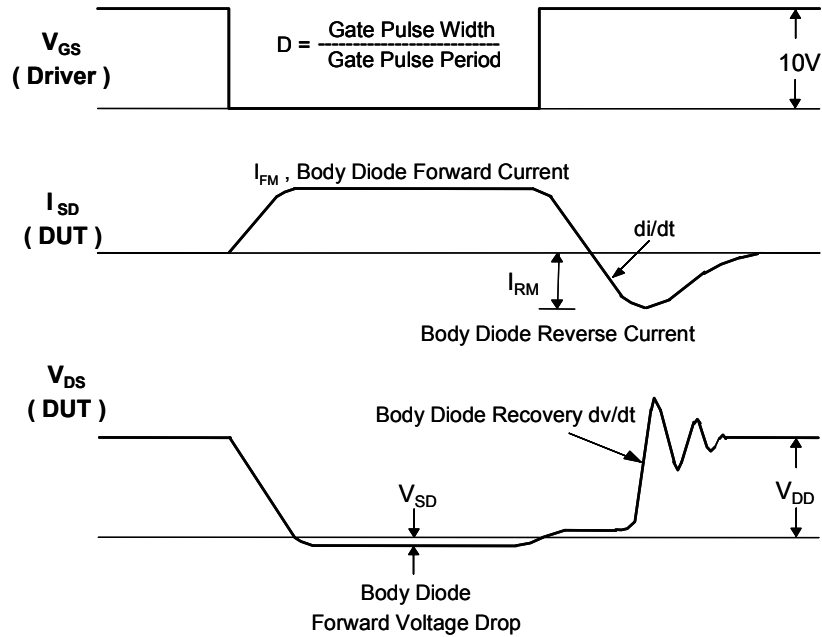
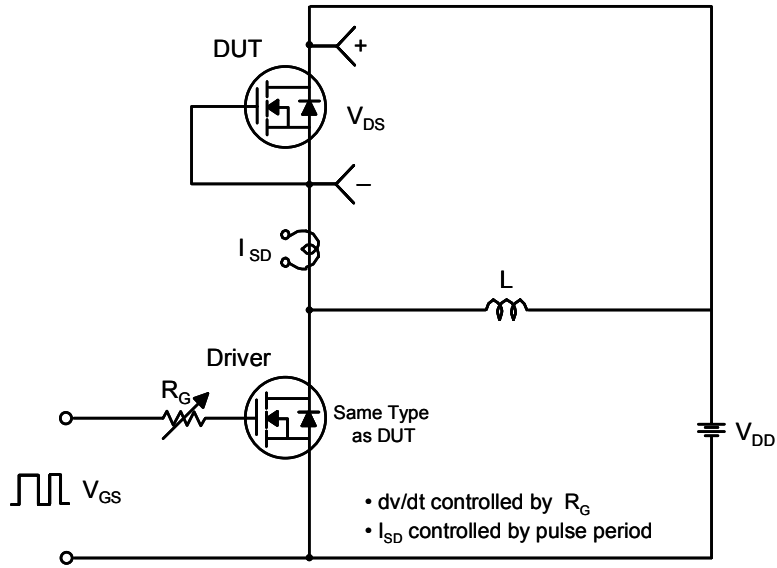
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

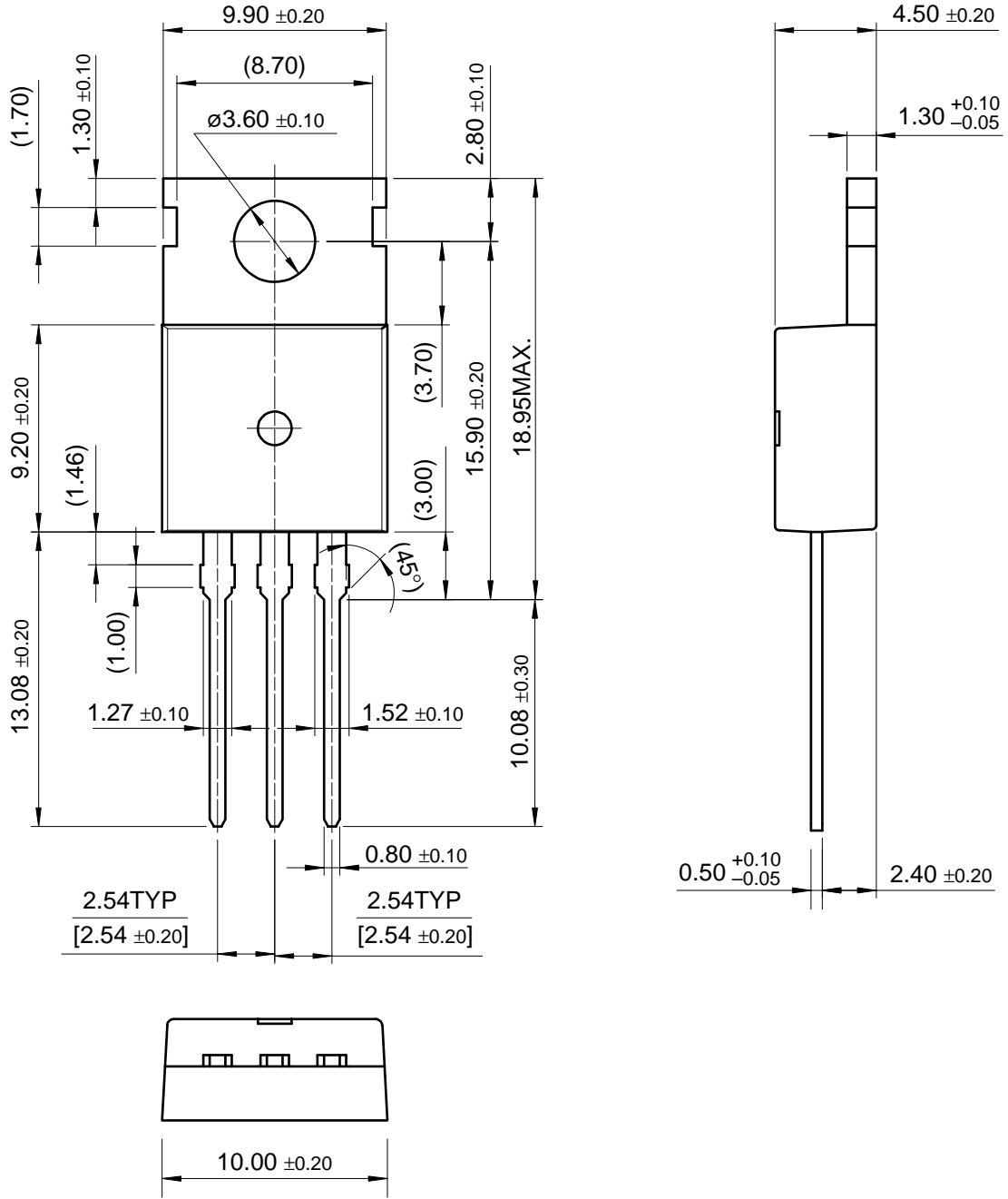


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

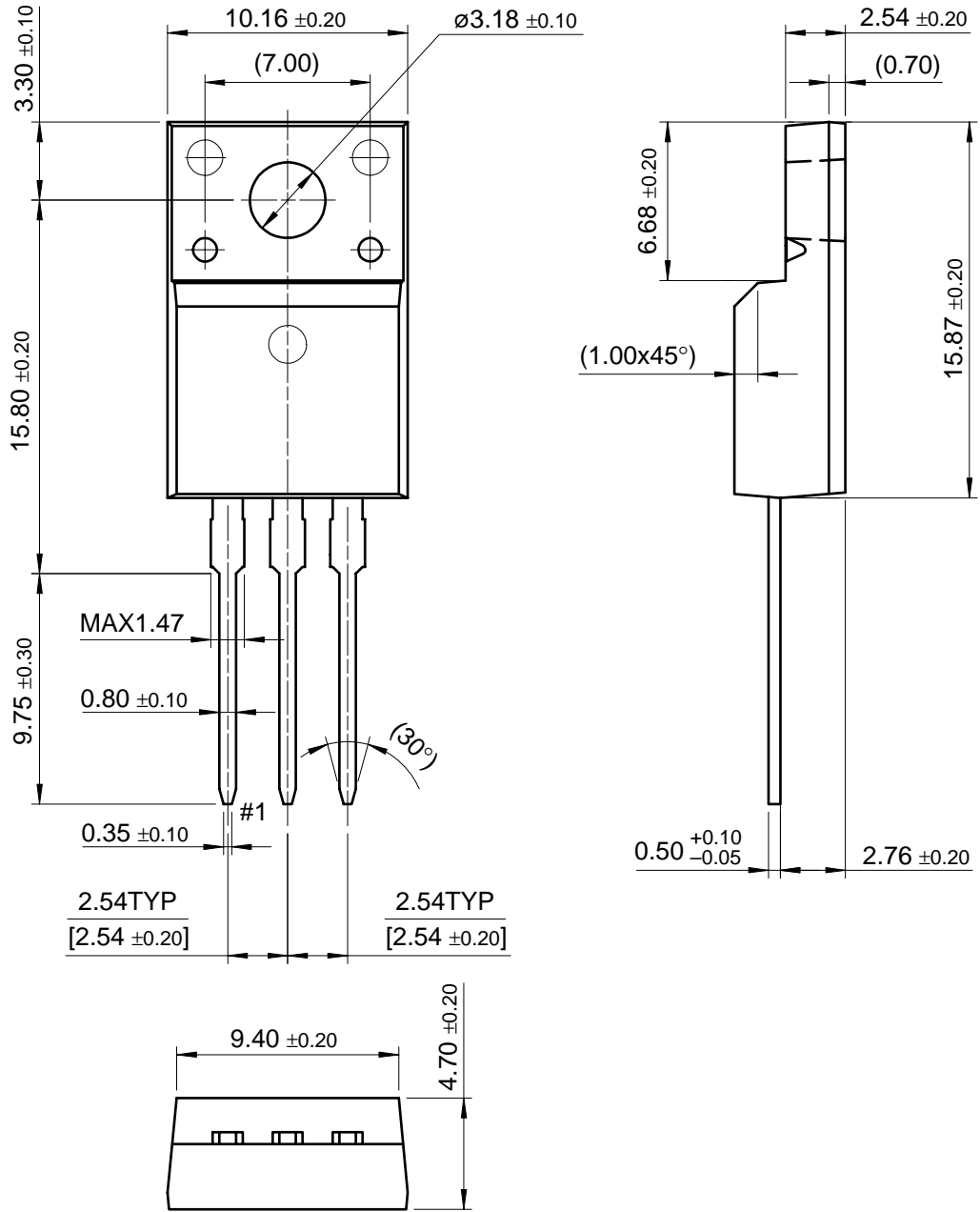
TO-220



Dimensions in Millimeters

Mechanical Dimensions (Continued)

TO-220F



Dimensions in Millimeters

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