Recommendations for Printed Circuit Board Assembly of Infineon PG-LQFP-64-6, -8 -11/ PG-LQFP-100-2/PG-LQFP-100-3/ PG-LQFP-144-4 Packages

Never stop thinking

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1 Package Description

The exposed die pad PG-LQFP-64/100/144 (**P**lastic **G**reen - **L**ow profile **Q**uad **F**lat **P**ackage), (**Figure 1**) is based on a plastic encapsulated LQFP package. Additionally it has an exposed paddle on the bottom of the package, which is achieved by an appropriate down-set. The die paddle is typically also soldered to the printed circuit board (PCB) to provide the primary heat removal path as well as excellent electrical grounding to the PCB.

"**G**" denotes "green" LQFP packages, which means lead-free package material set (RoHS compliant).

Features

- Optimized electrical performance
- Enhanced thermal performance through exposed die pad structure
- Gullwing leads and exposed die pad are Sn- or NiPd(Au-Ag-alloy)-plated
- Thin packages (low profile)
- Package outline according JEDEC MS-026

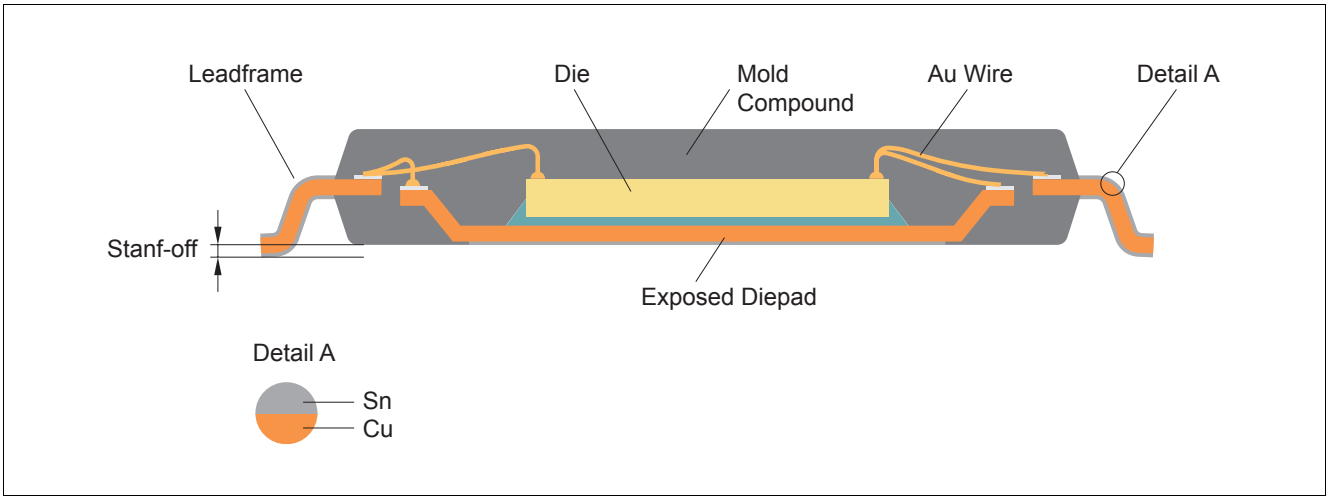

Figure 1 PG-LQFP with exposed die pad and external Sn-plating

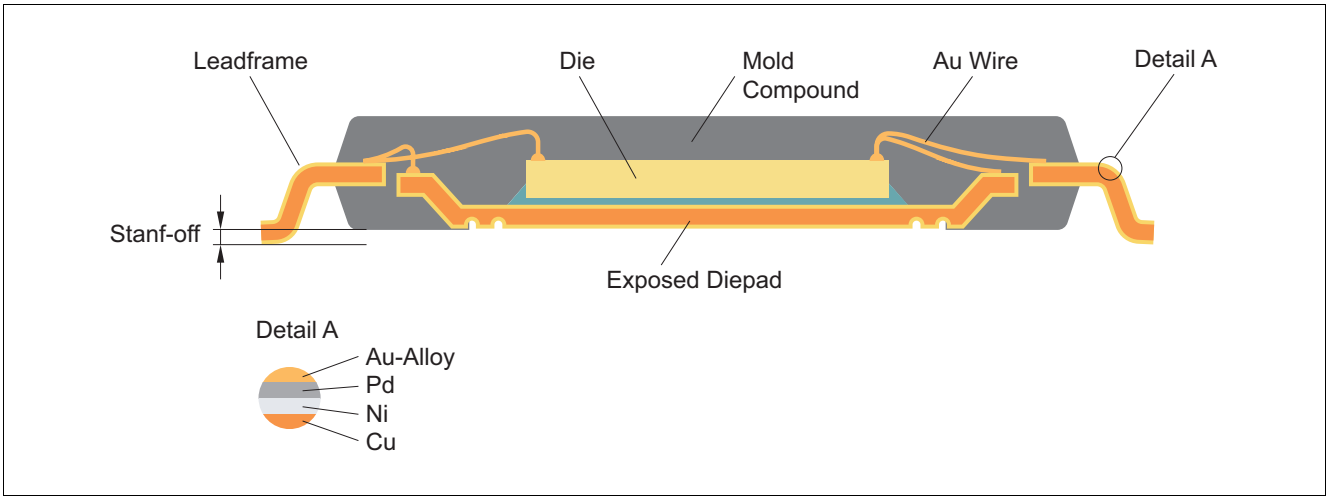

Figure 2 PG-LQFP with exposed die pad and overall NiPd(Au-Ag-alloy)-plating

2 Package Handling

2.1 ESD Protective Measures

Semiconductor devices are normally Electrostatic Discharge Sensitive Devices (ESDS devices) requiring specific precautionary measures regarding handling and processing. Discharging of electrostatically charged objects over an Integrated Circuit (IC) can be caused by human touch or by processing tools, resulting in high-current and/or high-voltage pulses that can damage or even destroy sensitive semiconductor structures. On the other hand, ICs may also be charged during processing. If discharging takes place too quickly (“hard” discharge), it may cause load pulses and damage, too. ESD protective measures must therefore prevent contact with charged parts as well as electrostatic charging of the ICs. Protective measures against ESD must be taken during handling, processing, and the packing of ESDS devices. A few hints are provided below on handling and processing.

2.1.1 ESD Protective Measures in the Workplace

- Standard marking of ESD protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Earth (“ground”) bonding points for wrist straps
- Trolleys or carts with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields

2.1.2 Equipment for Personal

- Dissipative/conductive footwear or heel straps
- Suitable smocks
- Wrist straps with safety resistors
- Gloves or finger coats that are ESD-proven (with specified volume resistivity)

Regular training of staff to avoid ESD failures using this equipment is recommended.

2.1.3 Production Installations and Processing Tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers on sliding tracks
- All parts reliably connected to ground potential
- No potential difference between individual machine and tool parts
- No sources of electrostatic fields

Detailed information on ESD-protective measures may be obtained from the ESD Specialist through Area Sales Offices. Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

2.2 Packing of Components

Different packings such as fixtures for feeding components in an automatic pick&place machine (tape&reel, trays,…) and surrounding bags and boxes to prevent damage during transportation or storage are available depending on component and customer needs. Please refer to product and package specifications (on the IFX homepage) and our sales department to get information about what packing is available for a given product.

Generally the following list of standards dealing with packing should be considered if applicable for a given package and packing:

IFX packings according to the IEC 60286-* series

IEC 60286-3 Packaging of components for automatic handling – Part 3:
Packaging of surface mount components on continuous tapes

IEC 60286-4 Packaging of components for automatic handling – Part 4:
Stick magazines for dual-in-line packages

IEC 60286-5 Packaging of components for automatic handling – Part 5:
Matrix trays

Moisture-Sensitive Surface Mount Devices (SMDs) are packed according to IPC/JEDEC J-STD-033*: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Detailed Packing Drawings: Packing Information (Internet)

Other References

ANSI/EIA-481-* Standards Proposal No. 5048, Proposed Revision of ANSI/EIA-481-B 8 mm through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling (if approved, to be published as ANSI/EIA-481-C)

EIA-783 Guideline Orientation Standard for Multi-Connection Package
(Design Rules for Tape and Reel Orientation)

2.3 Moisture-Sensitive Components (MSL Classification)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. Penetration of moisture into the package molding compound is generally caused by exposure to ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus it is necessary to dry moisture-sensitive components, seal them in a moisture-resistant bag, and only remove them immediately prior to assembly to the Printed Circuit Board (PCB). The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines eight different MSLs (**Table 1**). Please refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of our products. IPC/JEDEC-J-STD-20 specifies the maximum reflow temperature that shall not be exceeded during board assembly at the customer’s facility.

Table 1 Moisture Sensitivity Levels (according to IPC/JEDEC J-STD-033*)

Level	Floor Life (out of bag)	
	Time	**Conditions**
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSLs, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth. In addition, packing material (e.g. trays, tubes, reels, tapes,…) may not withstand higher baking temperatures. Please refer to imprints/labels on the respective packing to determine allowable maximum temperature.

For Pb-free components, two MSLs can be given: One for a lower reflow peak temperature (tin-lead) and one for a higher reflow peak temperature (lead-free). Each one is valid for the respective application.

2.4 Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination, and package cracking effects.

These standards should be taken into account:

IEC 60721-3-0 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; introduction

IEC 60721-3-1 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; Section 1: Storage

IEC 60721-3-2 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; Section 2: Transportation

IEC 61760-2 Surface mounting technology - Part 2:
Transportation and storage conditions of surface mounting devices (SMD) – Application guide

IEC 62258-3 Semiconductor Die Products - Part 3:
Recommendations for good practise in handling, packing and storage

ISO 14644-1 Clean rooms and associated controlled environments Part 1:
Classification of airborne particulates

Table 2 General Storing Conditions – Overview

Product	Condition for Storage
Wafer/Die	N2 or MBB[1)] (IEC 62258-3)
Component - moisture sensitive	MBB (JEDEC J-STD-033*)
Component - not moisture sensitive	1K2 (IEC 60721-3-1)

1) MBB = Moisture Barrier Bag

Maximum Storage Time

The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

Internet Links to Standards Institutes

American National Standards Institutes (ANSI)

Electronics Industries Alliance (EIA)

Association Connecting Electronics Industries (IPC)

2.5 Handling Damage and Contamination

Automatic or manual handling of components in or out of the component packing may cause mechanical damage to package leads and/or body.

QFP components in the packing are ready to use.

Any contamination applied to component or packing may cause or induce processes that (together with other factors) may lead to a damaged device. The most critical issues are:

- Solderability problems
- Corrosion
- Electrical shorts (due to conductive particles)

2.6 Component Solderability

The sufficiently thick and wettable metal surfaces (final plating) or solder depots/balls of most semiconductor packages assure good solderability, even after a long storage time. **Note that the cut edges of the pins should be ignored in any assessment of solderability.** Suitable methods for the assessment of solderabiltiy can be derived from JESD22B 102 or IEC60068-2-58.

QFP components are Sn- or NiPd(Au-Ag-alloy)-plated and are compatible with SnPb-containing and Pb-free soldering.

3 Printed Circuit Board (PCB)

3.1 General Remarks

Generally the printed circuit board design and construction is a key factor for achieving a high board assembly yield and also sufficient reliability. Examples are PCB pad designs for the leads and for the large central exposed pad, which is generally recommended to be soldered to the PCB for having optimum thermal, electrical, and board level reliability performance. Also via design and board finish has to be considered.

We want to emphasize, that this document is just a guideline to support our customers in board design. Additionally studies at the customers may be necessary for optimization, which take into account the actual PCB manufacturer's capability, the customer's SMT process, and product specific requirements.

3.2 PCB Pad Design

Concerning the PCB pad design for the lead lands please refer to the **Footprint** of the respective package.
It can be found in the Infineon Internet under
->products ->packages -> respective package (e.g. PG-LQFP-100-3) -> footprint.

(http://www.infineon.com/packages)

As a general guideline see IPC 7351/7355. (Generic Requirements for Surface Mount Design and Land Pattern Standard)

The exposed die pad of LQFP packages has got a surface finish which is the same as for the leads. In most applications the die pad allows to transfer a large amount of heat into the PCB to achieve higher thermal performance. Therefore it should be soldered to the board onto the "thermal" pad. This also increases solder joint reliability and for some applications/products the electrical performance. We recommend using die pad size on the exposed die pad LQFP package as maximum "thermal" pad size on the PCB slightly smaller size of the "thermal" pad is also possible.

Land pattern design for lead attachment on the PCB should be the same as that for conventional, non thermally/electrically enhanced packages.

Figure 3 shows a schematic of the bottom view of an exposed die pad.

Figure 4 shows a schematic drawing of the PCB metal design for the pads and defines the important geometric parameters.

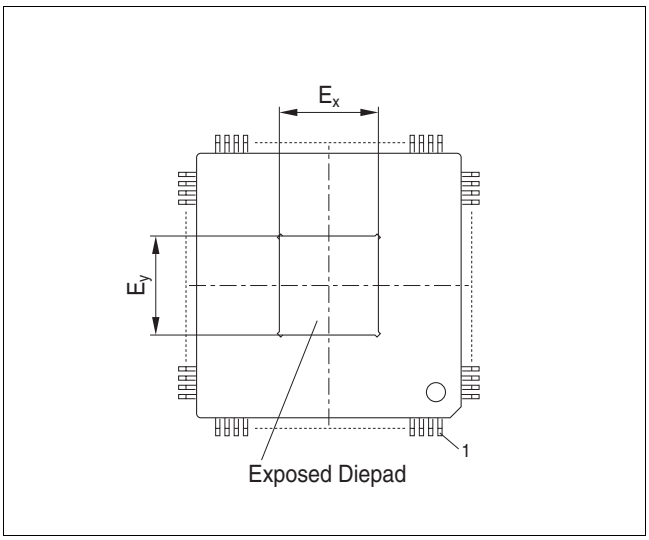

Figure 3 Bottom View Exposed Die Pad

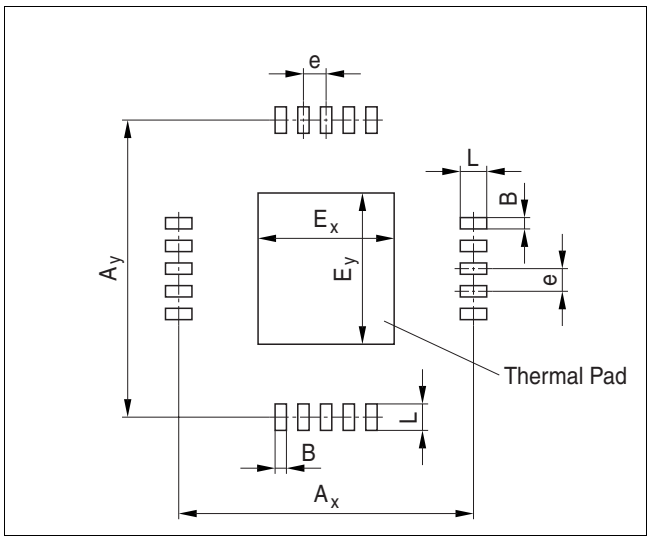

Figure 4 Schematic Drawing of PCB Pad Design Recommendation

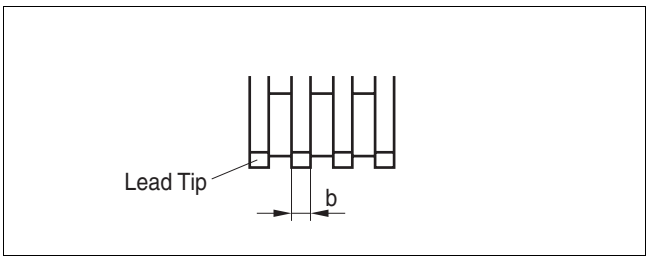

Figure 5 Package Lead Width b

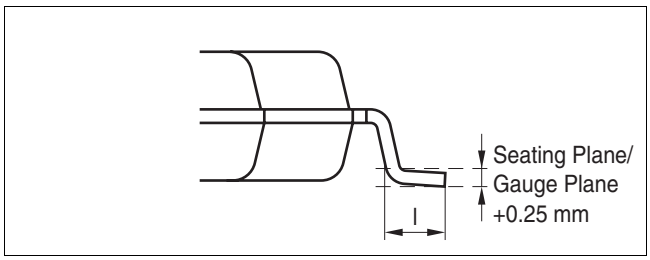

Figure 6 Package Lead Length l

In **Table 3** the details of the appropriate package specific dimensions are given.

Table 3 Recommended PCB Pad Dimensions for QFP-Packages (all dimensions in mm)

Package Name	QFP perimeter lead size on package		QFP perimeter pad size on PCB		Pad mean distances / Die Pad dimensions		Pad pitch	Pad Number (per side)	
	l	b	L	B	A_x /E_x	A_y /E_y	e	n_x	n_y
PG-LQFP-64-6	0.6	0.2	1.35	0.29	11.45/3	11.45/3.13	0.5	16	16
PG-LQFP-64-6	0.6	0.2	1.35	0.29	11.45/5.6	11.45/5.6	0.5	16	16
PG-LQFP-64-6	0.6	0.2	1.35	0.29	11.45/6	11.45/6	0.5	16	16
PG-LQFP-64-8	0.6	0.2	1.35	0.29	11.45/5	11.45/5	0.5	16	16
PG-LQFP-64-8	0.6	0.2	1.35	0.29	11.45/6	11.45/6	0.5	16	16
PG-LQFP-64-11	0.6	0.2	1.35	0.29	11.45/6.3	11.45/6.3	0.5	16	16
PG-LQFP-100-2	0.6	0.22	1.35	0.29	15.45/5.9	15.45/5.7	0.5	25	25
PG-LQFP-100-3	0.6	0.22	1.35	0.29	15.45/9.5	15.45/9.5	0.5	25	25
PG-LQFP-100-3	0.6	0.22	1.35	0.29	15.45/5.9	15.45/5.7	0.5	25	25
PG-LQFP-100-3	0.6	0.22	1.35	0.29	15.45/4.8	15.45/4.8	0.5	25	25
PG-LQFP-144-4	0.6	0.22	1.35	0.29	21.45/11.5	21.45/11.5	0.5	36	36
PG-LQFP-144-4	0.6	0.22	1.35	0.29	21.45/5	21.45/5	0.5	36	36
PG-LQFP-144-4	0.6	0.22	1.35	0.29	21.45/6	21.45/6	0.5	36	36
PG-LQFP-176-1	0.6	0.22	1.35	0.29	25.45	25.45	0.5	44	44
PG-LQFP-176-2	0.6	0.22	1.35	0.29	25.45	25.45	0.5	44	44
PG-LQFP-176-4	0.6	0.22	1.35	0.29	25.45/5.15	25.45/5.42	0.5	44	44
PG-LQFP-176-4	0.6	0.22	1.35	0.29	25.45/9.78	25.45/11	0.5	44	44

3.3 Solder Mask Layer

Generally, two basic types of solder pads are used.

- “Solder mask defined” (SMD) pad (**Figure 7**): The copper metal pad is larger than the solder mask opening above this pad. Thus the pad area is defined by the opening in the solder mask.

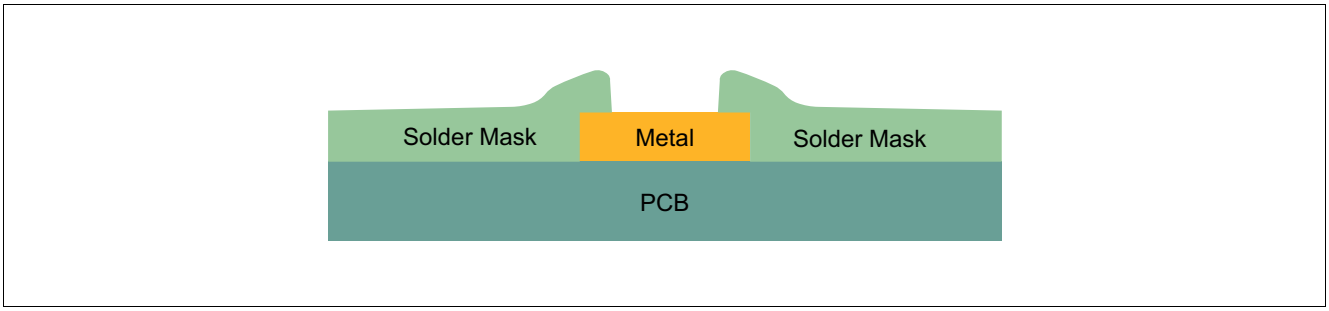

Figure 7 SMD Pad

- “Non solder mask defined” (NSMD) pad (**Figure 8**): Around each copper metal pad there is solder mask clearance. Dimensions and tolerances of the solder mask clearance have to be specified, that no overlapping of the solder pad by solder mask occurs (depending on PCB manufacturer’s tolerances, 75 µm is a widely used value).

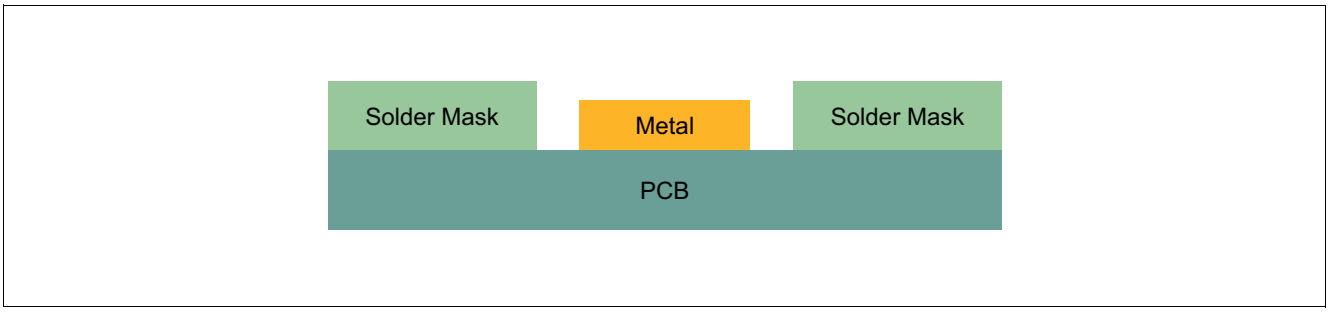

Figure 8 NSMD Pad

We recommend NSMD type for the lead solder pads, because the tolerances of the copper pads are lower than the solder masking process tolerances.

Between the lead pads on the PCB and the thermal pad in the center there should also be a ring of solder mask, which reduces the risk of solder bridging. If the distance between the lead pads and the metal of the thermal pad area is ≤ 300 µm, the solder mask should overlap the thermal pad metal area by ≥ 100 µm on each side.

3.4 Vias in Thermal Pad

Some products/applications require that the “thermal” pad is connected to inner copper layers of the PCB by vias. One reason may be to maximize the electrical performance especially for products operating with high frequency. Another reason may be the optimization of the thermal performance for products having high thermal power dissipation. In this case plated through-hole vias, which are (if possible fully) connected to inner and/or bottom copper planes of the board, help to distribute the heat into the board area, which penetrates from the chip over the package die pad and the solder joint to the thermal pad on the board.

The number of vias are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

A typical via hole diameter for such thermal vias is 0.4 mm. The number of vias in the thermal pad depends on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the printed circuit board. However an array of thermal vias with pitch 1.2 - 1.5 mm can be a reasonable starting point for most products/applications for further optimization.

If the vias remain open during board manufacturing, then solder may flow into the vias during LQFP board assembly (“solder wicking”). This could have the effects of large voids in the “thermal” solder joint under the die pad, and/or solder protruding from the other side of the board, which may disturb a second solder paste printing process on this other board side. If necessary, the solder wicking can be avoided by 2 ways.

Recommended solution: plugging of the vias (filling with epoxy) with additional plating, i.e. no stand-off, i.e no limitations regarding solder paste

Another option is tenting the vias with solder mask (e.g. with dry-film solder mask). Via tenting shall be done from top, because with via tenting from bottom side voiding rate is significantly higher. In this case it has to be taken into account that sufficient area is available for good wetability of the exposed die pad. The solder mask diameter should be at least 0.1 mm larger than the via diameter.

Note: These recommendations are to be used as a guideline only.

3.5 PCB Pad Finishes

The solder pads must have good wetability to the solder paste. In general all finishes are well proven for SMT assembly, but especially for fine pitch applications, like for LQFP packages, the quality of the plating/finish gets more important. Because of the uneven surface of Hot Air Solder Leveling (HASL) finish, lead-free or lead containing HASL is less preferred for LQFP assembly (especially for pitch < 0.65 mm) compared to completely “flat” platings like Cu-OSP (OSP: Organic Solderability Preservative) or electroless Sn or NiAu,.

From package point of view it is not possible to give a definite recommendation for PCB pad finish. It also depends strongly on board design, pad geometry, all components on board, and process conditions.

4 Board Assembly

4.1 General Remarks

Many factors within the board assembly process have influence on assembly yield and board level reliability. Examples are design and material of the stencil, the solder paste material, solder paste printing process, component placement, and reflow process. Additionally, studies at the customers may be necessary for optimization, which take into account the actual printed circuit board, the customer's SMT equipment, and product specific requirements.

Lead-free PG-LQFP with Sn plating can generally be assembled with either SnPb based or lead-free SnAgCu based solder paste and reflow processes.

4.2 Solder Stencil

The solder paste is applied onto the PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB.

While for a standard non exposed die pad leadframe package the stencil thickness depends only on lead pitch and coplanarity, the package standoff must also be considered for the exposed die pad packages. Thus for exposed die pad LQFP packages of pitch 0.5 mm it is recommended to use 125 - 150 µm thick stencils. To ensure a uniform and high solder paste transfer to the PCB, lasercut (mostly made from stainless steel) and electroformed stencils (Nickel) should be preferred. Rounding the corners of the apertures (radius ~50 µm) can support good paste release.

The apertures for the lead solder joints should be of the same size as the metal pads on the PCB (for recommendations see **Chapter 3**). The stencil in the thermal pad area shall be segmented in smaller, multiple openings (see schematic example of **Figure 9**). One large opening would result in excessive solder volume under the LQFP die pad compared to the lead pads as well as significantly higher voiding rate and higher risk of solder balling.

In our tests we printed a total area of about 70 - 80% of the thermal pad with solder paste. With this procedure we achieved good results in board assembly yield and reliability. The resulting solder joint stand-off at the exposed die pad was typically in the range of 100 µm. The most appropriate way of segmenting depends on the number and location of vias (if existing) and the solder resist layout on this thermal pad. In case of a regular thermal via matrix the stencil openings should be arranged in areas between the vias. In our evaluations we typically have used opening sizes in the range of 0.6 - 1 mm^2, depending on via density and thermal pad size.

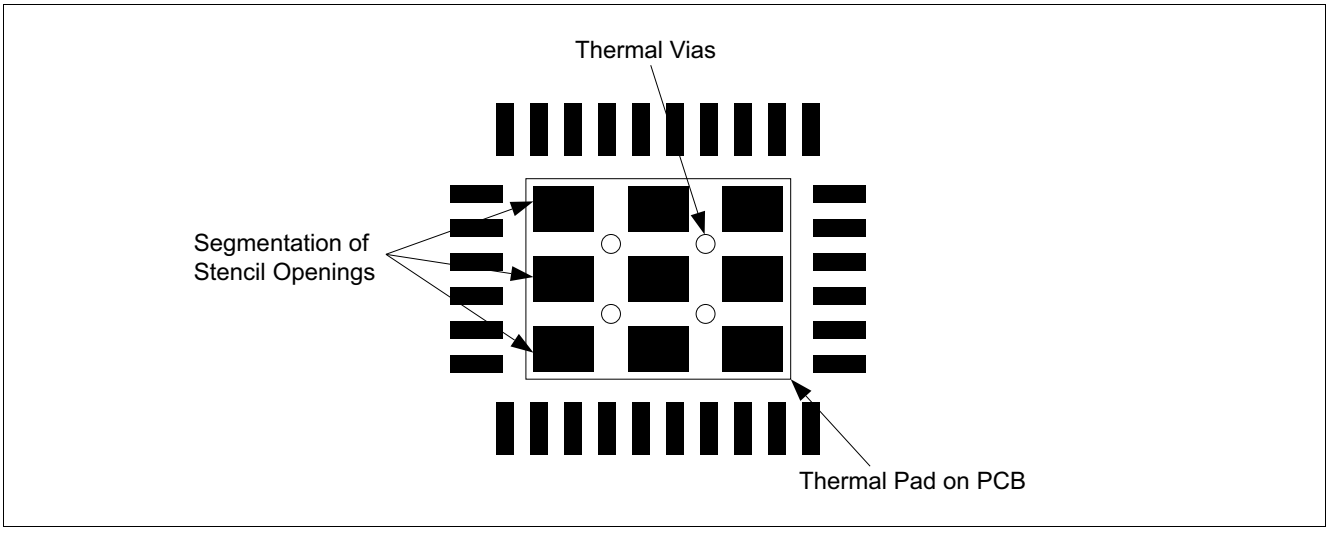

Figure 9 Example for Segmentation of Stencil Openings on Thermal Pad Area of PCB

4.3 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux and solvents. In term of mass, this means approximately 90 wt% alloy and 10 wt% flux system and solvents. The flux system has to remove oxides and contamination from the solder joints during the soldering process. The capacity for removing oxides and contamination is given by the respective activation level.

The contained solvent adjusts the viscosity needed for the solder paste application process. The solvent has to evaporate during reflow soldering.

The metal alloy in Pb-containing solder pastes is typically eutectic SnPb or nearly eutectic SnPbAg. Pb-free solder pastes contain so-called SAC-alloys (typically 1 - 4% Ag and < 1% Cu). A “no-clean” solder paste is preferred for packages such as QFPs with ePad where cleaning below the component is difficult.

The paste must be suitable for printing the solder stencil aperture dimensions; type 3 paste is recommended.

Solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

4.4 Component Placement

Although the self alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints exposed die pad LQFP packages have to be placed accurately according to their geometry. Positioning the packages manually is not recommended.

Component placement accuracies of ±50 µm are obtained with modern automatic component placement machines using vision systems. With these systems both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB or additionally on individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling a correct centering of the complete package.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for non solder mask defined pads). In consequence, for exposed die pad LQFP packages with 0.5 mm lead pitch the device pad to PCB pad misalignment has to be better than 50 µm to assure a robust mounting process. Generally this is achievable with a wide range of placement systems.

The following remarks are important:

- Especially on large boards local fiducials close to the device can compensate large PCB tolerances.
- It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- To ensure the identification of the packages by the vision system, an adequate lighting as well as the correct choice of the measuring modes is necessary. The accurate settings can be taken from the equipment manuals.
- Too much placement force can lead to squeezed out solder paste and causes solder joint shorts. On the other hand too low placement force can lead to insufficient contact between package and solder paste and this can lead to open solder joints or badly centered packages.

4.5 Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes have these features:

- Forced convection (max. qualified profile given by the JEDEC MSL classification)
- Vapor phase
- Infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of the QFP packages.

Wave soldering is not possible because the package has to be attached to the PCB by so-called SMD glue. In case of QFP packages with ePad this is not possible if the exposed pad is intended to be soldered to the PCB. Furthermore wave soldering is only possible if the products in QFP packages are qualified for wave soldering (so-called solder heat test).

During the reflow process, each solder joint has to be exposed to temperatures above the solder melting point or “liquidus” for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the packing for the peak package body temperature. When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components. The recommended type of process is forced convection reflow. Using a nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering tin-lead metal alloys.

The temperature profile of a reflow process is one of the most important factors of the soldering process. It is divided into several phases, each with a special function. **Figure 10** shows a general forced convection reflow profile for soldering QFP packages. **Table 4** shows an example of the key data of such a solder profile that has been used for the Sn-Pb and for the Pb-free alloy listed above. Individual parameters are influenced by various facts, not only by the package. It is essential to follow the solder paste manufacturer’s application notes, too. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to all components’ and materials’ demands. We recommend measuring the solder joints’ temperatures by thermocouples beneath the respective packages. Consider that components with large thermal masses do not heat up at the same speed as lightweight components, and the position and the surrounding of the package on the PCB as well as the PCB thickness can also influence the solder-joint temperature significantly. Therefore, these reflow profiles should serve as guidelines, but have to be further adjusted to each actual application.

Because the thermal impact of reflow is critical for Pb-free solder pastes, linear temperature profiles can be applied to achieve a shorter reflow time in total. When reducing the soaking time, it is very important to ensure a homogeneous temperature distribution on the PCB; in this case, a convection oven is recommended.

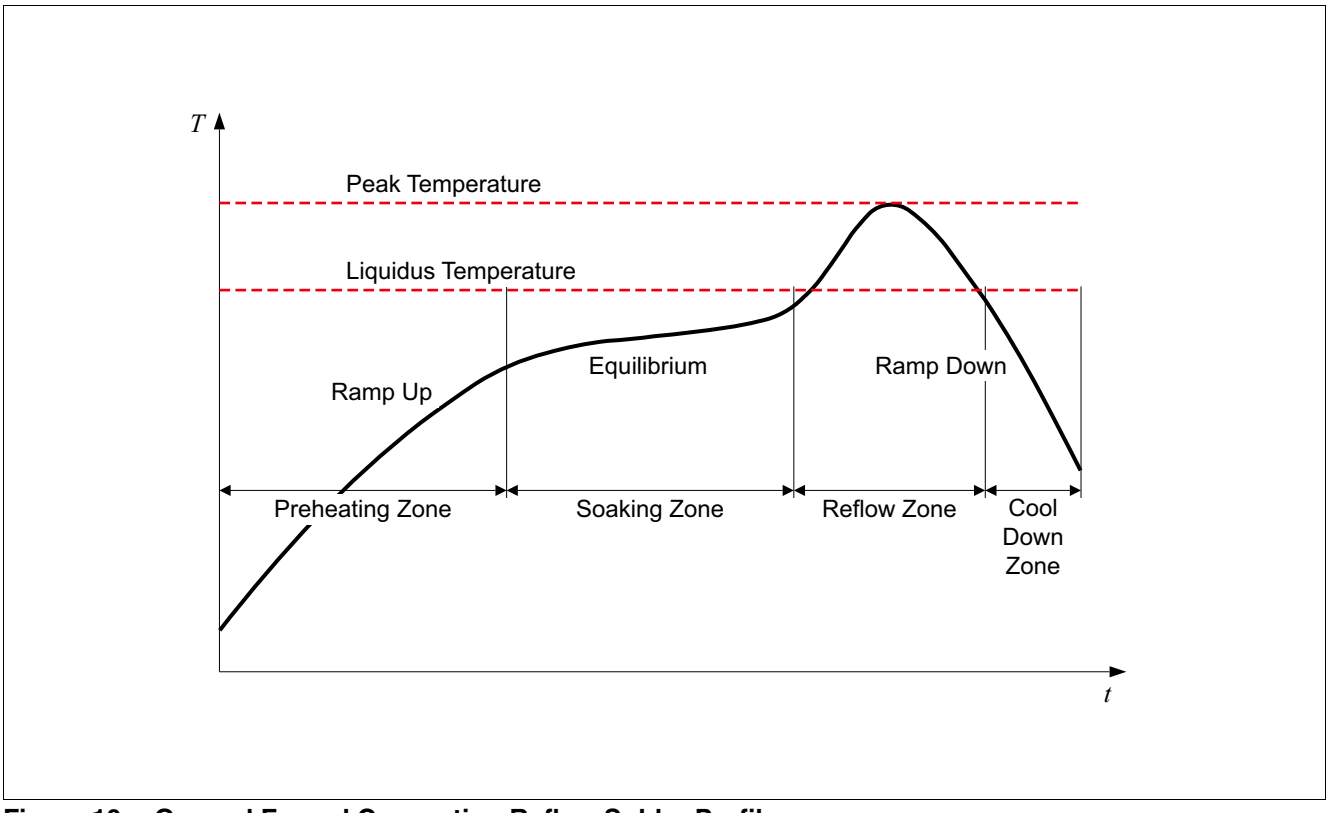

Figure 10 General Forced Convection Reflow Solder Profile

Table 4 Example for the Key Data of a Forced Convection Reflow Solder Profile

Parameter	Tin-lead Alloy (SnPb or SnPbAg)	Pb-free Alloy (SnAgCu)	Main Influences coming from …
Preheating rate	2.5 K/s	2.5 K/s	Flux system (Solder paste)
Soaking temperature	140 - 170°C	140 - 170°C	Flux system (Solder paste)
Soaking time	80 s	80 s	Flux system (Solder paste)
Peak temperature	225°C	245°C	Alloy (Solder paste)
Reflow time above melting point (liquidus)	60 s	60 s	Alloy (Solder paste)
Cool down rate	2.5 K/s	2.5 K/s	

Double-Sided Assembly

QFP packages are generally suitable for mounting on double-sided PCBs. First, the board assembly is done on one side of the PCB (including soldering). Afterwards, the second side of the PCB is assembled.

If the solder-joint thickness is a critical dimension, please be aware that solder joints of components on the first side will be reflowed again in the second reflow step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity forces the components nearer to the PCB surface). This shape will be frozen at temperatures below the melting point of solder and therefore result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

4.6 Cleaning

After the reflow soldering process some flux residues can be found around the solder joints. If a "no-clean" solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. However, if the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution have to be selected with consideration of the packages to be cleaned, the used flux in the solder paste (rosin-based, water-soluble, etc.), environmental and safety aspects. Removing/drying even of small residues of the cleaning solution should also be done very thorough. Contact the solder paste manufacturer for recommended cleaning solutions. Note: exposed die pad LQFP-packages are capable of being cleaned at the leads while cleaning of the die pad area is limited under the package body.

4.7 Inspection

After component placement:

A visual inspection after component placement can be done by microscope or AOI in order to check if the mounting was done completely or if severe misplacements occurred. The orientation of the component can also be checked.

After soldering:

A simple visual inspection of the solder joints can be done by optical microscope.

The only visible areas are leads and leadframe areas that extend beyond the package body.

Figure 11 shows an QFP-like SMD lead with ideal wetting. For QFPs, it is also recommended to assess the joint quality under leads, especially under the exposed pad with x-ray and/or cross sections.

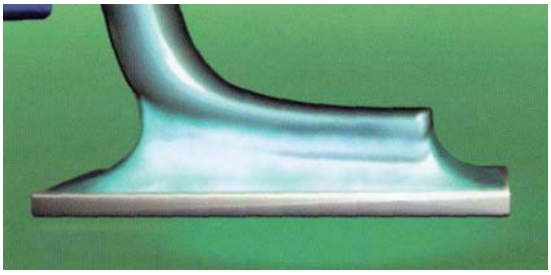

Figure 11 Example of an Ideally Wetted SMD Lead (source: IPC610)

If exposed die pads are soldered, the only reliable inspection method for the whole solder joint is by X-ray.

An automated visual inspection of the solder joints with conventional AOI systems is limited to the outer solder joints. Please keep in mind that the non-wetting of the punched or sawn lead tip is not a reject criterion. For packages with exposed pads the only reasonable method for efficient inline control is to use AXI (Automatic X-ray Inspection) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing and data transfer routines. These systems enable the user to reliably detect soldering defects such as poor soldering, bridging, voiding, and missing parts. For the acceptability of electronic assemblies, please refer also to the IPC-A-610 standard.

Cross-sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character. Nonetheless, these analysis methods must be used during engineering of new products to get detailed information about the solder joint quality.

Pb-free solder joints look different from Pb-containing (e.g. SnPb) solder joints. Tin-lead solder joints typically have a bright and shiny surface. Pb-free (SnAgCu) solder joints typically do not have a bright surface. Lead-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder, as the solder alloys used are not exactly eutectic, unlike 63Sn37Pb solder alloy. This means that SnAgCu-solders do not have a melting point but a melting range of several degrees. Although lead-free solder joints have this dull surface, this does not mean that lead-free joints are of lower quality or weaker than the Pb-containing joints.

Also NiPd(Au-Ag-alloy)-plated packages look different compared to wide spread Sn-plated.

It is therefore necessary to teach the inspection staff how these lead-free joints or NiPd(Au-Ag-alloy)-plated packages look like, and/or to adjust optical inspection systems to handle lead-free solder joints or NiPd(Au-Ag-alloy)-plated packages.

5 Rework

If a defect component is observed after board assembly the device can be removed and replaced by a new one. Repair of single solder joints is generally possible but requires proper tools for fine pitch applications while also the remarks in **Chapter 4.5** for temperature profile and exposure time to ambient atmosphere have to be respected.

5.1 Tooling

The rework process is commonly done on special rework equipment. There are a lot of systems available on the market, and for processing these packages the equipment should fulfill the following requirements:

- *Heating*: Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With free-programmable temperature profiles (e.g. by PC controller) it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from underside is recommended. Infrared heating can be applied, especially for preheating the PCB from underside, but it should be only supporting the hot air flow from the upside. Instead of air also nitrogen can be used.
- *Vision system*: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB a split optic should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- *Moving and additional tools*: The device should be relocatable on the whole PCB area. Placement accuracy is recommended to be better than ±100 µm. The system should have the capability of removing solder residues from PCB pads (e.g. special vacuum tools).

5.2 Device Removal

If it is intended to send a defect component back to the supplier, please note that during the removal of this component no further defects must be introduced to the device, because this may hinder the failure analysis at the supplier. This includes the following recommendations:

- *Moisture*: According to his moisture sensitivity level, possibly the package has to be dried before removal. If the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried according to the recommendations (see **Chapter 4.5**), otherwise too much moisture may have been accumulated and damage may occur (popcorn effect).
- *Temperature profile*: During soldering process it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (see **Chapter 4.5**).
- *Mechanics*: Be aware not to apply high mechanical forces for removal. Otherwise failure analysis of the package can be impossible or PCB can be damaged. For large packages pipettes can be used (implemented on most rework systems), for small packages tweezers may be more practical.

5.3 Site Redressing

After removing the defect component the pads on the PCB have to be cleaned from solder residues.
Don’t use steel brushes because steel residues can lead to bad solder joints. Before placing a new component it is recommended to apply solder paste on each PCB pad by printing (special micro stencil) or dispensing.
It is recommended to use only no-clean solder paste.

5.4 Reassembly and Reflow

After preparing the site, the new package can be placed onto the PCB. The package is positioned exactly above the PCB pads, in height just that there is no contact between the package and the PCB and the package is then dropped into the printed or dispensed flux or solder paste depot (Zero-force-placement). During soldering process it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (see **Chapter 4.5**).

6 List of References

IPC/EIA/JEDEC-J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications
IPC/EIA/JEDEC-J-STD-001	Requirements for Soldered Electrical and Electronic assemblies
IPC A-610	Acceptability of Electronic Assemblies
IPC/EIA/JEDEC J-STD-002	Solderability tests for Component Leads, Terminations, Lugs, Terminals and Wires
IPC/JEDEC J-STD-033/-020	Handling, Packing, Shipping and Use of Moisture / Reflow Sensitive Surface Mount devices / Moisture/reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
JESD22-B102	Test Method for Solderability
IEC 60068-2-58	Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices
IPC 7351/7355	Generic Requirements for Surface Mount Design and Land Pattern Standard

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