POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification for Approval

Customer : _____

Model Type : LCD Module

Model Number : PG12864ARS-ANN-G

Edi : 0

Customer Sign	Sales Sign	Approved By	Prepared By

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1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 128 dots *64 dots
- 1/64 Duty, 1/9 bias
- STN LCD, positive
- Reflective LCD, gray
- 6 o'clock viewing angle
- 8 bits parallel data input

1.2 Mechanical Specifications

- Outline dimension   :   93.0mm(L)*70.0mm(W)*9.7mm max.(H)
- Viewing area   :   72.0mm   *40.0mm
- Active area   :   66.52mm   *33.24mm
- Dot size   :   0.48mm * 0.48mm
- Dot pitch   :   0.52mm   * 0.52mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	V_{DD}	-	0	7.0	V
LCD drive Supply voltage	V_{DD}-V_{EE}	-	0	17	V
Input voltage	V_{IN}	-	0	V_{DD}+0.3	V
Operating temperature	T_{OPR}	-	-20	70	°C
Storage temperature	T_{STG}	-	-30	80	°C
Humidity*1	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	V_{DD}	-	4.5	5	5.5	V
"H" input voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
"L" input voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Supply current	I_{OP}	V_{DD}=5V	-	-	13	mA
LCD driving voltage	V_{LCD}	V_{DD}-V_O	-	13.6	-	V

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1.5 Optical Characteristics

1/64 duty, 1/9 bias, Vopr=13.6V, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	C≥2.0,∅=0°C	30°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	2	3	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-	140ms	200ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	300ms	500ms	Note 4

Note 1: Definition of angles θ and ∅

Light (when reflected)   z (θ=0°)
Y'(∅=180°)
Sensor
LCD panel
X'
X(∅=90°)
∅
Z'
Light (when transmitted)
Y(∅=0°)
(θ=90°)
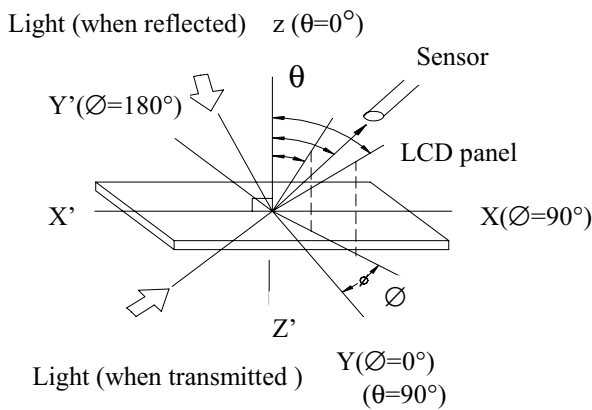
Note 2: Definition of viewing angles θ1 and θ2
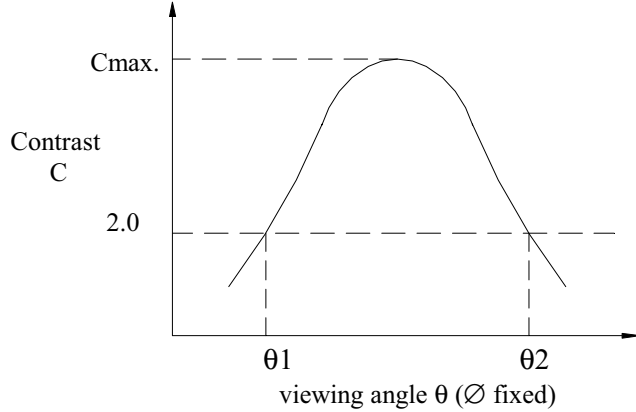
Cmax.
Contrast C
2.0
θ1
θ2
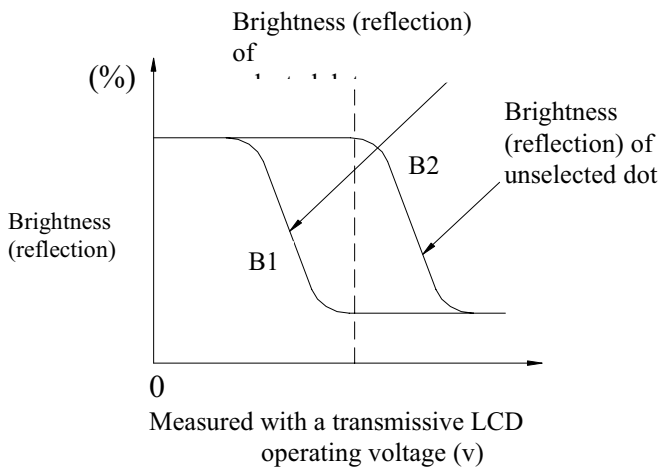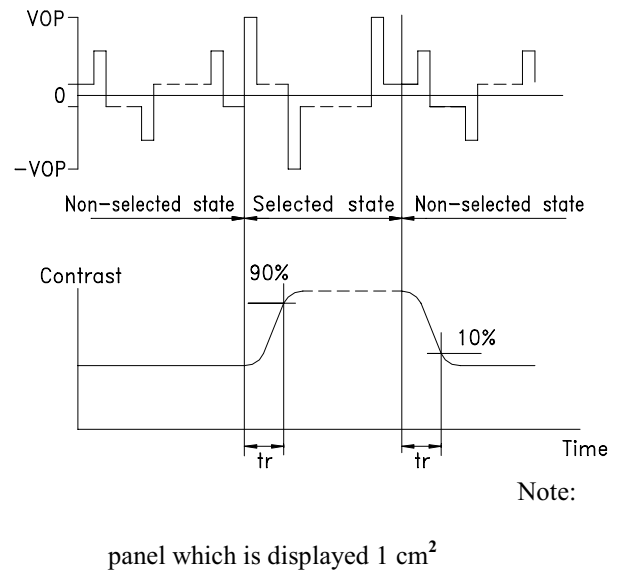viewing angle θ (∅ fixed)
Note :   Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

Brightness (reflection) of
(%)
Brightness (reflection)
B2
B1
Brightness (reflection) of unselected dot
0
Measured with a transmissive LCD operating voltage (v)

Note 4: Definition of response time

VOP
0
−VOP
Non−selected state | Selected state | Non−selected state
Contrast
90%
10%
tr
tr
Time
Note:

panel which is displayed 1 cm²

Vopr : Operating voltgae   fFRM : Frame frequency
ton   : Response time (rise)   toff : Response time (fall)

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2. MODULE STRUCTURE

2.1 Counter Drawing

*See Appendix

2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VSS	Signal ground (GND)
2	VDD	Power supply for logic (+5V)
3	Vo	Operating voltage for LCD (variable)
4	D/$\overline{\text{I}}$	Register selection input High =Data register Low =Instruction register (for write) 　　Busy flag address counter (for read)
5	R/$\overline{\text{W}}$	R/W signal input is used to select the read/write mode High =Read mode,　　Low =Write mode
6	E	Start enable signal to read or write the data
7-10	DB0~ DB3	Four low order bi-directional three-state data bus lines. Use for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation.
11-14	DB4~ DB7	For high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
15	CS1	Chip enable for D2 (segment 1 to segment 64)
16	CS2	Chip enable for D3 (segment 65 to segment 128)
17	$\overline{\text{RST}}$	Reset signal
18	Vout	Negative voltage power supply
19	NC	Non-connection
20	NC	Non-connection

Contrast Adjust

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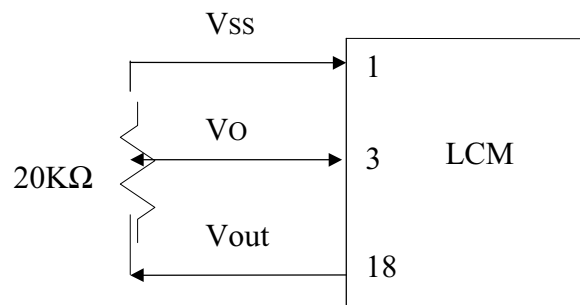
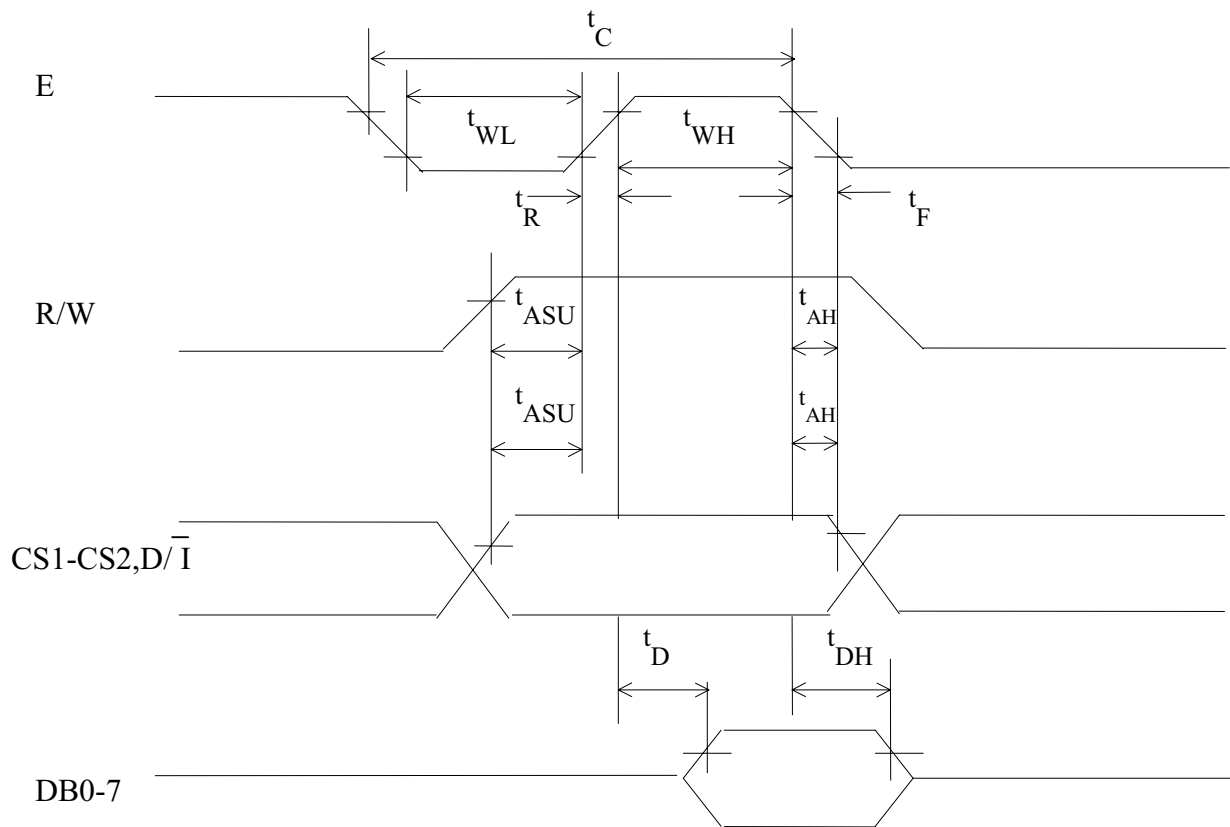## 2.3 Timing Characteristics
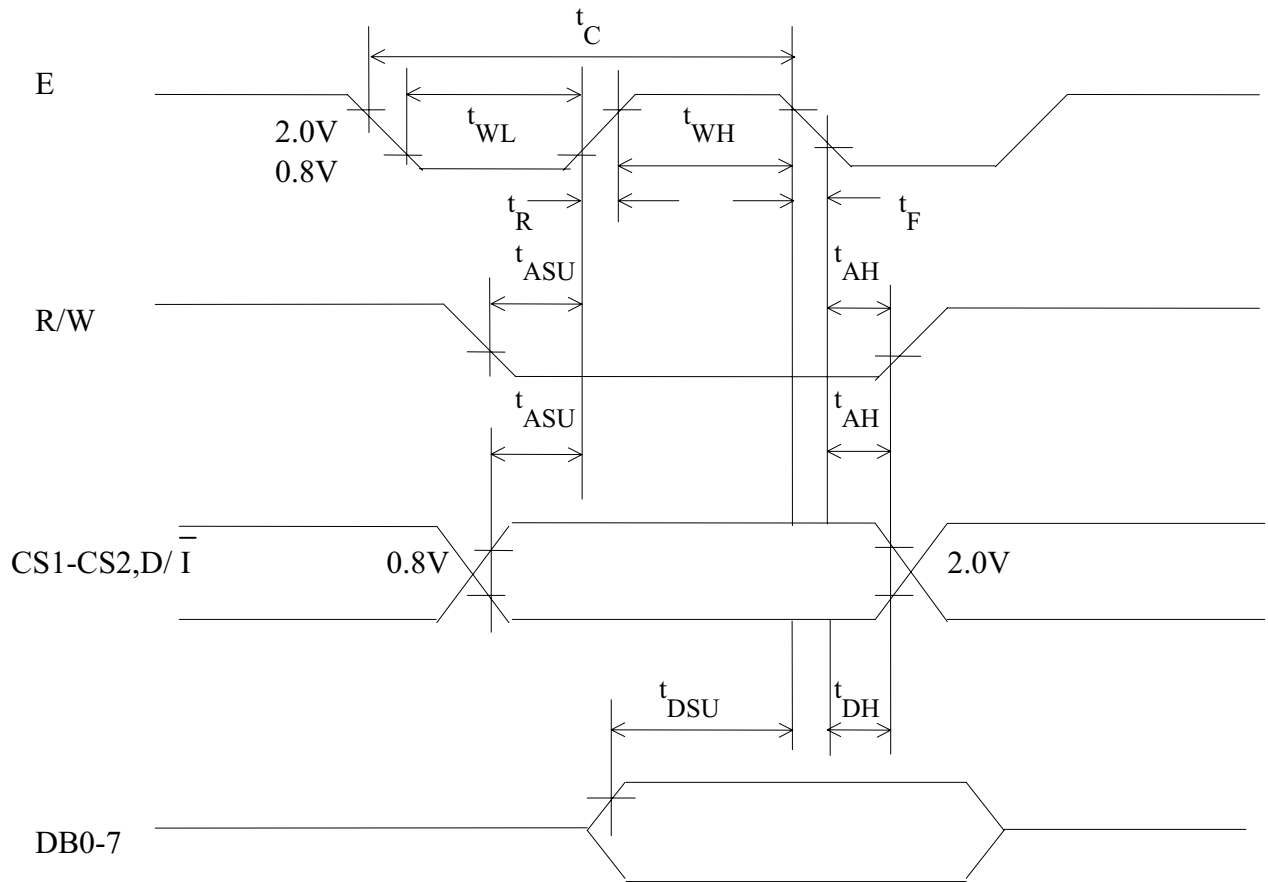
MPU write timing

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MPU read timing

Characteristic	Symbol	Min.	Typ	Max	Unit
E Cycle	tC	1000	-	-	ns
E High Level Width	tWH	450	-	-	ns
E Low Level Width	tWL	450	-	-	ns
E Rise Time	tR	-	-	25	ns
E Fall Time	tF	-	-	25	ns
Address Set-Up time	tASU	140	-	-	ns
Address Hold Time	tAH	10	-	-	ns
Data Set-Up Time	tSU	200		-	ns
Data Delay Time	tD	-	-	320	ns
Data Hold Time (Write)	tDHW	10	-	-	ns
Data Hold Time (Read)	tDHR	20	-	-	ns

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2.4 Display command

Instructions	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
					Code							
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected.	
Display start line	0	0	1	1	Display start line (0-63)						Specifies the RAM line displayed at the top of the screen.	
Set Page (x address)	0	0	1	0	1	1	1	Page (0-7)			Sets the page (X address) of RAM at the page (X address) register.	
Set Y address	0	0	0	1	Y address (0-63)						Sets the Y address in the Y address in the counter.	
Status read	1	0	Busy	0	ON/OFF	Reset	0	0	0	0	Reads the status. Reads 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Detailed Explanation

Display On/Off

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

MSB   LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

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- **Display Start Line**

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

MSB   LSB

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and
displayed at the top of the screen. Figure 1 shows examples of display (1/64 duty cycle) when the
start line=0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total
line number of LCD screen, from the line specified by display start line instruction, is displayed.
See figure 1.

Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

MSB   LSB

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing
or reading to or from MPU is executed in this specified page until the next page is set. See figure 2.

Set Y Address

	R/W	D/I	DB7						DB0
Code	0	0	0	1	A	A	A	A	A	A

MSB   LSB

Y
Y address AAAAAA (binary) of the display data RAM is set in the Y address Counter. After that,
address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read

	R/W	D/I	DB7						DB0
Code	1	0	Busy	0	ON/OFF	Reset	0	0	0	0

MSB   LSB

• Busy
When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is
1, so you should make sure that busy is 0 before writing the next instruction.

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• ON/OFF

Shows the liquid crystal display conditions: on condition or off condition.

When on/off is 1, the display is in off condition.
When on/off is 0, the display is in on condition.

• RESET

RESET=1 shows that the system is being initialized. In this condition, no instructions except status
 read can be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D
			MSB							LSB

Write 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by
 1 automatically.

Read Display Data
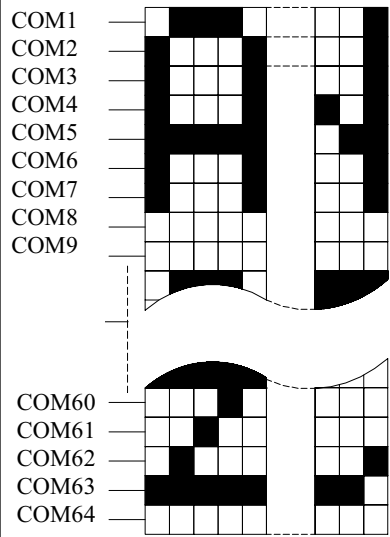
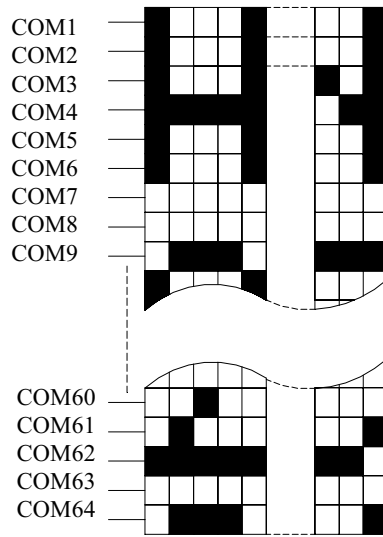|	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D
			MSB							LSB

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is
 increased by 1 automatically.
One dummy read is necessary right after the address setting. For details, refer to the explanation of
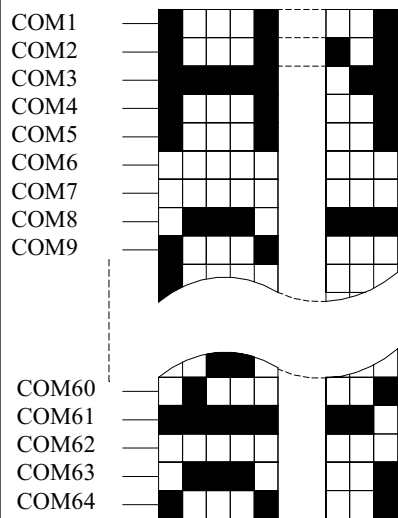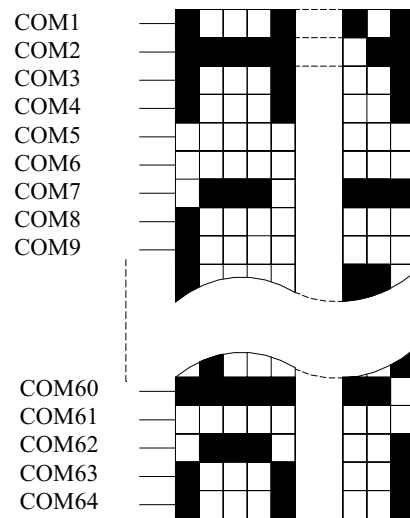 output register in "Function of Each Block".

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COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9

COM60
COM61
COM62
COM63
COM64

Start line = 0

COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9

COM60
COM61
COM62
COM63
COM64

Start line = 1

COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9

COM60
COM61
COM62
COM63
COM64

Start line = 2

COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9

COM60
COM61
COM62
COM63
COM64

Start line = 3

Figure 1 Relation between Start Line and Display

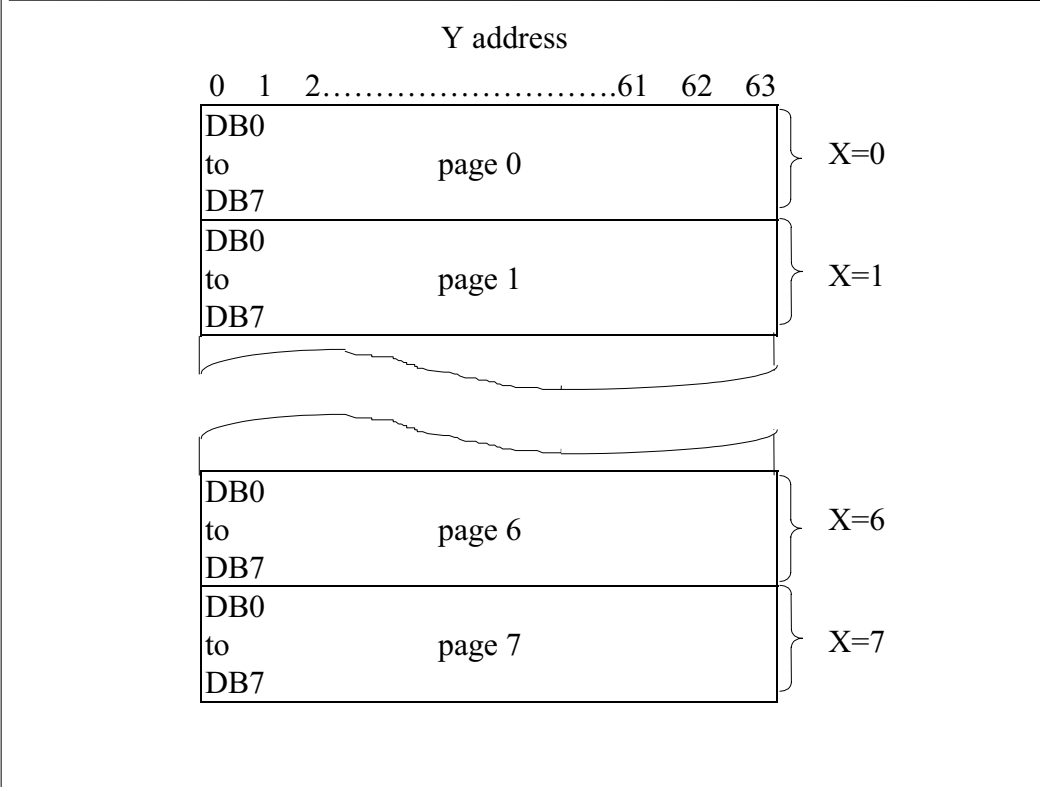|		
DB0 to DB7	page 0	X=0
DB0 to DB7	page 1	X=1
DB0 to DB7	page 6	X=6
DB0 to DB7	page 7	X=7

Y address

0   1   2………………………….61   62   63

Figure 2 Address Configuration of Display Data RAM

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