# POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

## Specification For Approval

Customer : 賀晟企業

Model Type : LCD Module

Sample Code : PG12864ARS-ANN-J-S0

Mass Production Code : _____

Edition : 0

| Customer Sign | Sales Sign | Approved By | Prepared By |
|---|---|---|---|
| | | 開發 90.5.14 蔡建忠 | 開發 90.5.14 |

**Display Start Line**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 1 | 1 | A | A | A | A | A | A |
| | | | MSB | | | | | | | LSB |

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 1 shows examples of display (1/64 duty cycle) when the start line=0-3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed. See figure 1.

**Set page (X address)**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 1 | 0 | 1 | 1 | 1 | A | A | A |
| | | | MSB | | | | | | | LSB |

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 2.

**Set Y Address**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 1 | A | A | A | A | A | A |
| | | | MSB | | | | | | | LSB |

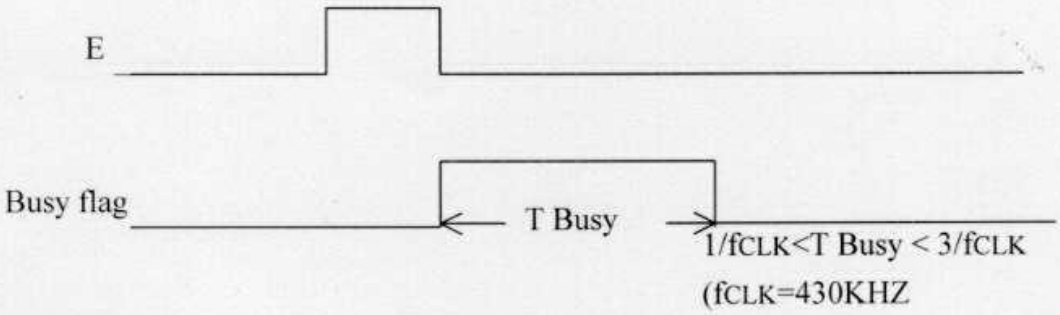
Y address AAAAAA (binary) of the display data RAM is set in the Y address Counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

**Status Read**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | BUSY | 0 | ON/OFF | REST | 0 | 0 | 0 | 0 |
| | | | MSB | | | | | | | LS |

• Busy

When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instruction.




• ON/OFF

Shows the liquid crystal display conditions: on condition or off condition.

When on/off is 1, the display is in off condition.
When on/off is 0, the display is in on condition.

• RESET

RESET=1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation condition.

**Write Display Data**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 1 | D | D | D | D | D | D | D | D |
| | | | MSB | | | | | | | LSB |

Write 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

**Read Display Data**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 1 | D | D | D | D | D | D | D | D |
| | | | MSB | | | | | | , | LSB |

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "Function of Each Block".

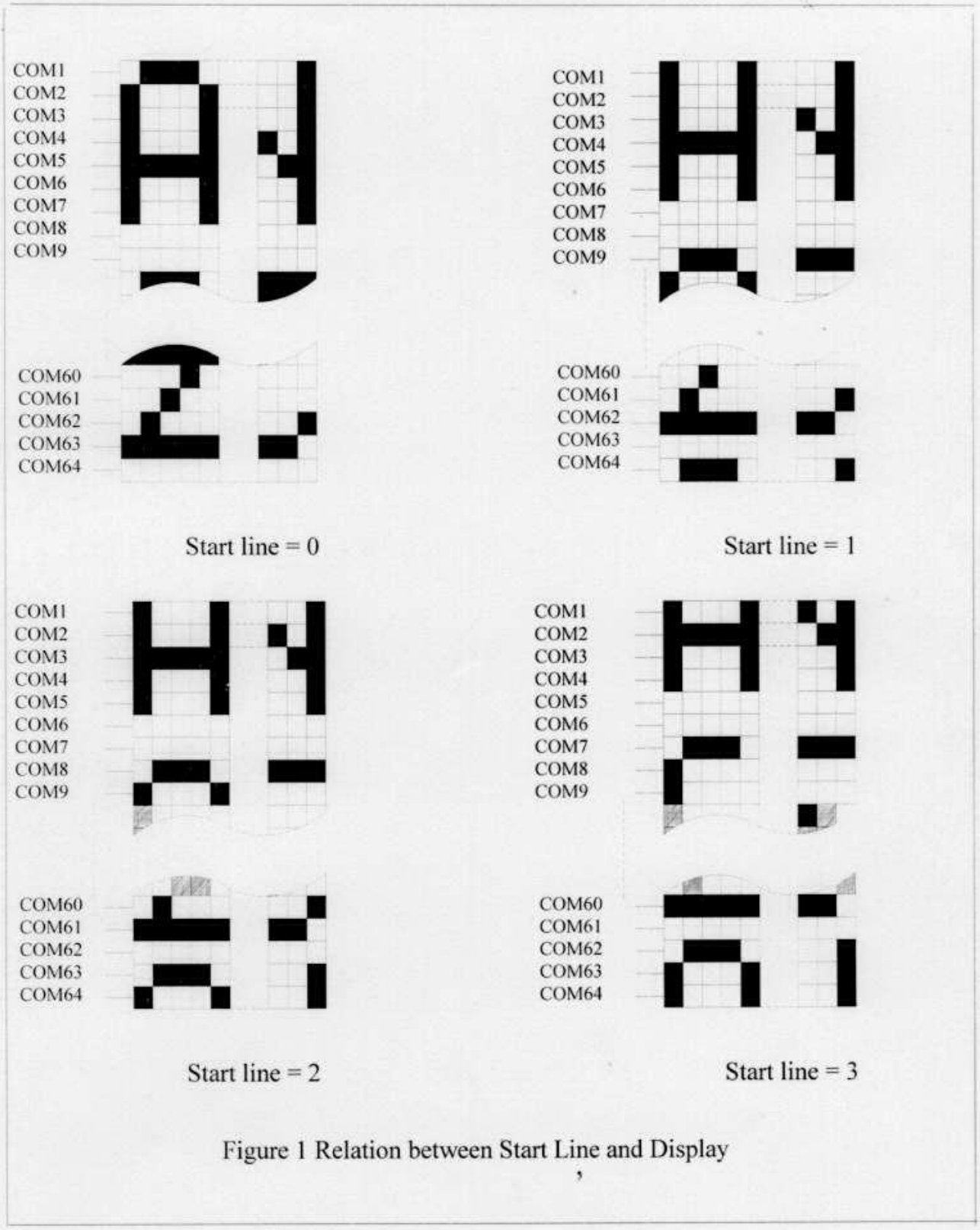



Figure 1 Relation between Start Line and Display

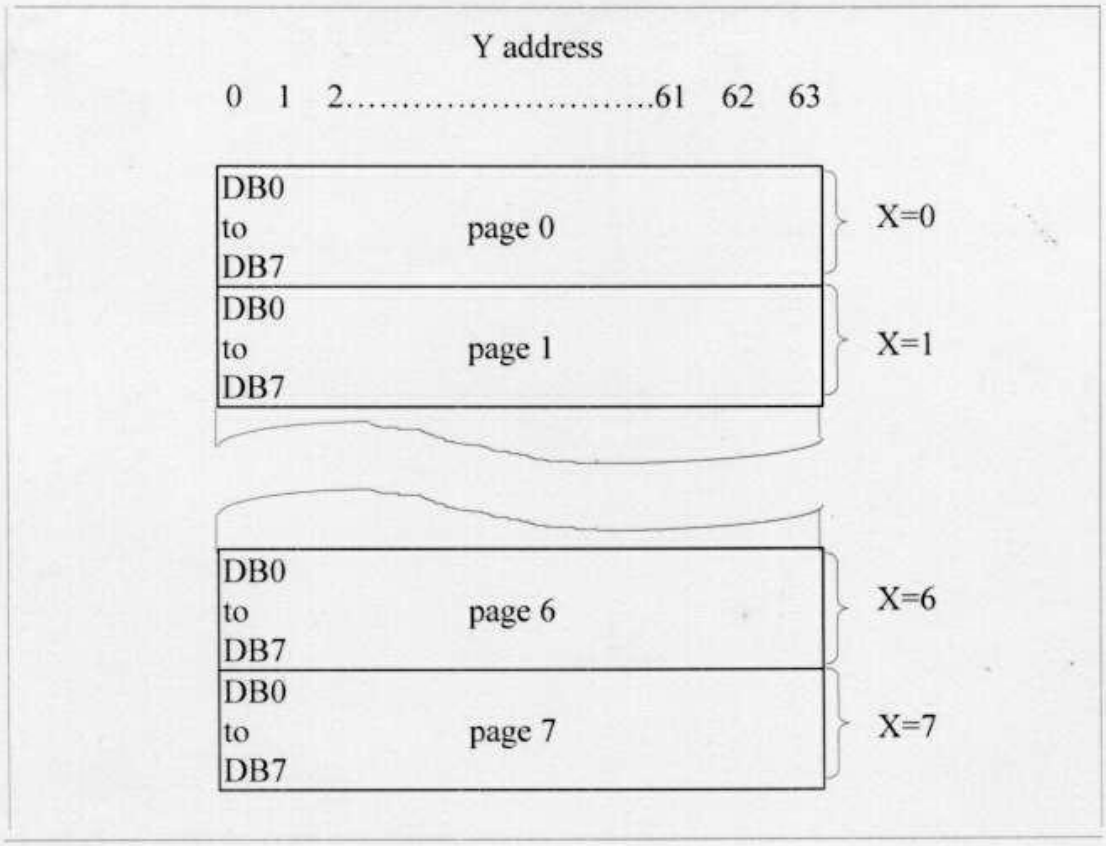
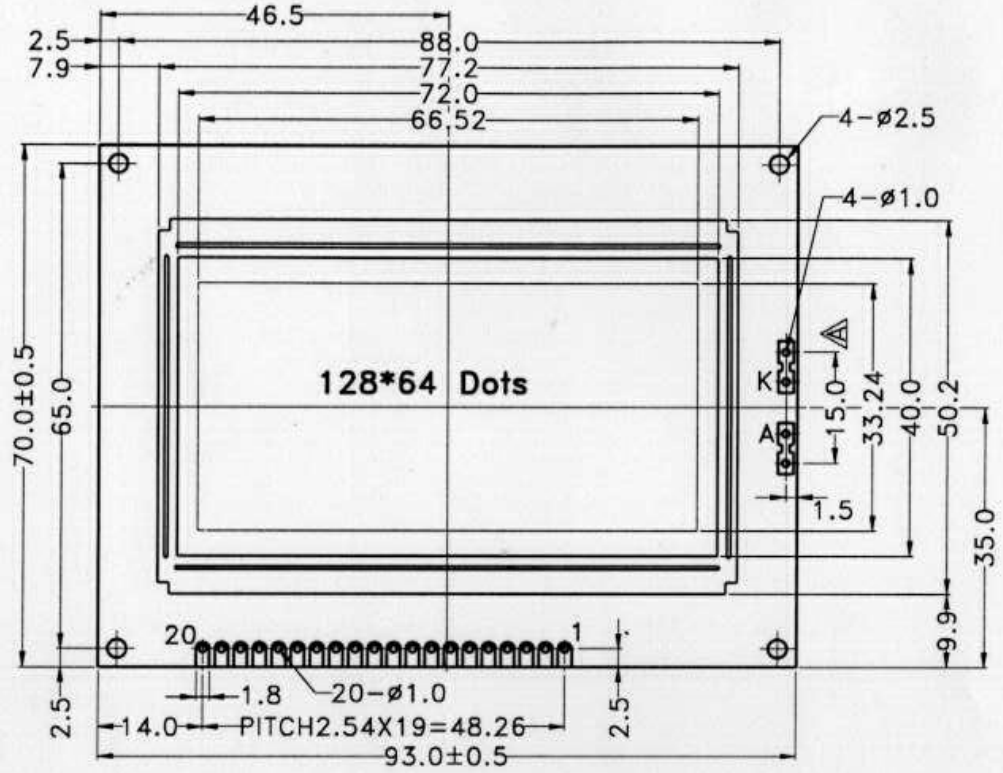


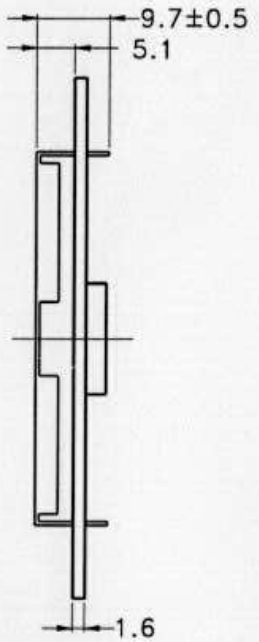

Figure 2 Address Configuration of Display Data RAM

Note: "128*64" consist of 2 "64*64"

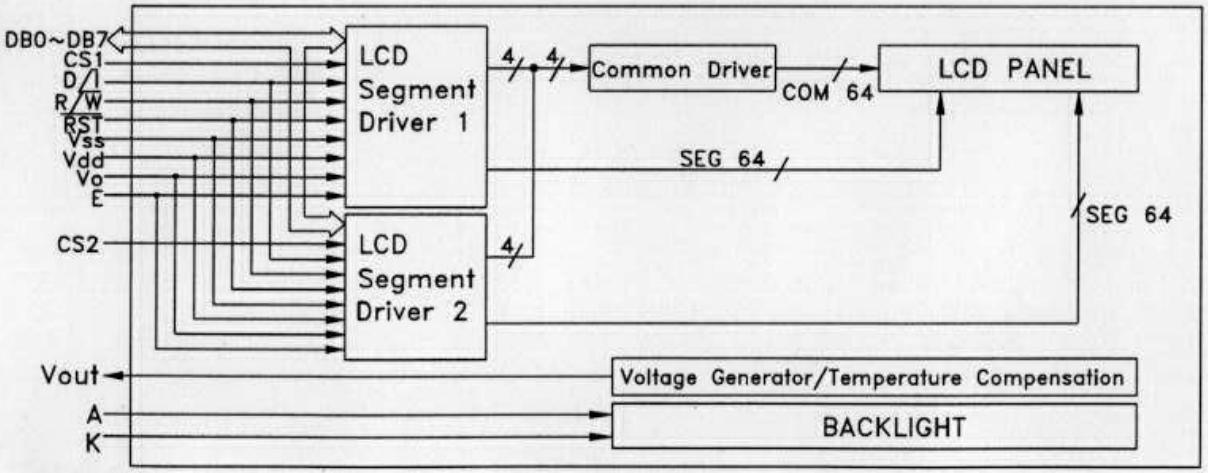
CS1⇒ Chip enable for left 64*64 (segment1 to segment 64)

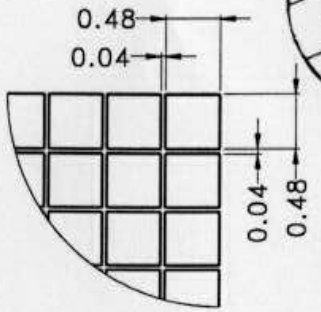
CS2⇒ Chip enable for right 64*64 (segment 65 to segment 128)




| PIN NO. | SIGNAL |
|---|---|
| 1 | Vss |
| 2 | Vdd |
| 3 | Vo |
| 4 | D/I |
| 5 | R/W |
| 6 | E |
| 7 | DB0 |
| 8 | DB1 |
| 9 | DB2 |
| 10 | DB3 |
| 11 | DB4 |
| 12 | DB5 |
| 13 | DB6 |
| 14 | DB7 |
| 15 | CS1 |
| 16 | CS2 |
| 17 | RST |
| 18 | Vout |
| 19 | A |
| 20 | K |




SCALE:15/1

The tolerance unless classified ±0.3mm



POWERTIP TECHNOLOGY

| | |
|---|---|
| SCALE: 1/1 | MODEL NAME PG 12864ARS-ANN-J |
| UNIT: mm | TITLE COUNTER DRAWING |
| EDI: A / PAGE: 1/1 | DRAWN NO. PG-95002-024 |
| APPROVED 郭貴文 | CHECKER 郭貴文 / DRAWN 開發 |

7/8-98'

# Out Going Inspection Specification

Inspection Standard：MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ。
Defect Level：Major Defect AQL 0.65; Minor Defect AQL 1.0。
Equipment：Gauge、MIL-STD、Powertip Tester、Sample。
Specification：

| N O | Item | Specification | Judge | Level |
|---|---|---|---|---|
| 1 | Part Number | Inconsistent with the P/N on the flow chart of production | N.G. | Major |
| 2 | Quantity | Inconsistent Q'TY with the flow chart of production | N.G. | Major |
| 3 | Electronic characteristics<br><br>A=( L + W )÷ 2 | Display short | N.G. | Major |
| | | Missing line | N.G. | Major |
| | | Dot missing A > 1/2 Dot size | N.G. | Major |
| | | No function | N.G. | Major |
| | | Out put data error | N.G. | Major |
| 4 | Appearance<br><br>A=( L + W )÷ 2<br><br>Dirty particle<br>( Include scratch、bubble ) | Material difference with flow chart | N.G. | Major |
| | | LCD Assembled in opposite direction | N.G. | Major |
| | | Bezel assembled in opposite direction | N.G. | Major |
| | | Shadow within LCD V./A + 1.0 mm | N.G. | Major |
| | | Dirty particle A > 0.4 mm | N.G. | Minor |
| | | Dirty particle length > 3.0mm<br>And 0.01mm < Width ≦ 0.05mm ( Width > 0.05mm Measure by area ) | N.G. | Minor |
| | | Without protective film | N.G. | Minor |
| | | Conductive rubber over bezel | N.G. | Minor |
| 5 | PCB Appearance<br><br>A=( L + W )÷ 2 | Burned PCB | N.G. | Major |
| | | Solder mask A > 1.0mm<br>( Finish coat not counted in ) | N.G. | Minor |
| | | A particle across the circuit | N.G | Minor |
| | | Circuit split > 1/2 Circuit width | N.G | Minor |
| | | More than three solder ball /splashes 0.13mm or less per 600mm$^2$ | N.G | Minor |

# CONTENTS

# 1. SPECIFICATIONS

## 1.1 Features

- Full dot-matrix structure with 128 dots *64 dots
- 1/64 Duty, 1/9 bias
- STN LCD, positive, gray
- Reflective LCD
- 12 o'clock viewing angle
- 8 bits parallel data input ,without controller IC

## 1.2 Mechanical Specifications

- Outline dimension : 93.0mm(L) *70.0mm(W)*10.2mm max.(H)
- Viewing area : 72.0mm *40.0mm
- Active area : 66.52mm *33.24mm
- Dot size : 0.48mm *0.48mm
- Dot pitch : 0.52mm *0.52mm

## 1.3 Absolute Maximum Ratings

| Item | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply Voltage | $V_{DD}$ | - | 4.5 | 5.5 | V |
| LCD drive Supply voltage | $V_{DD}$-$V_{EE}$ | - | 8.0 | 17 | V |
| Input voltage | $V_{IN}$ | - | -0.3 | $V_{DD}$+0.3 | V |
| Operating temperature | $T_{OPR}$ | - | -20 | 70 | °C |
| Storage temperature | $T_{STG}$ | - | -30 | 80 | °C |
| Humidity | HD | - | - | 90 | %RH |

## 1.4 DC Electrical Characteristics

$V_{DD}$=+5V±10%,$V_{SS}$=0V,TA=25°C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Logic Supply voltage | $V_{DD}$ | - | 4.5 | 5 | 5.5 | V |
| "H" input voltage | $V_{IH}$ | - | 0.7$V_{DD}$ | - | VDD | V |
| "L" input voltage | $V_{IL}$ | - | 0 | - | 0.3$V_{DD}$ | V |
| "H" output voltage | $V_{OH}$ | - | $V_{DD}$-0.4 | - | - | V |
| "L" output voltage | $V_{OL}$ | - | - | - | 0.4 | V |
| Supply current | $I_{DD}$ | $V_{DD}$=5V | - | 13 | 15.6 | mA |
| LCD driving voltage | $V_{OP}$ | $V_{DD}$-$V_O$ | ,13.2 | - | 14.0 | V |

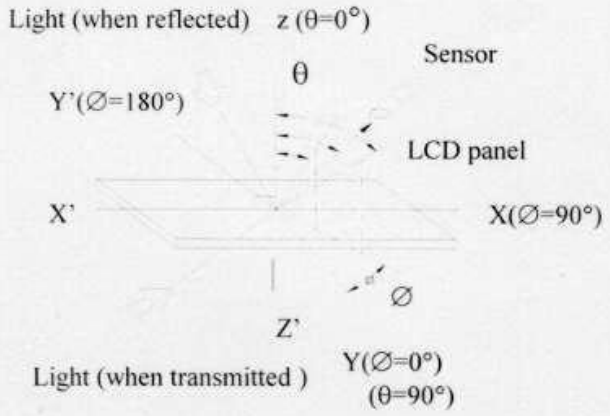
## 1.5 Optical Characteristics

1/128 duty, 1/12 bias, $V_{OPR}$=14.0V, Ta=25°C

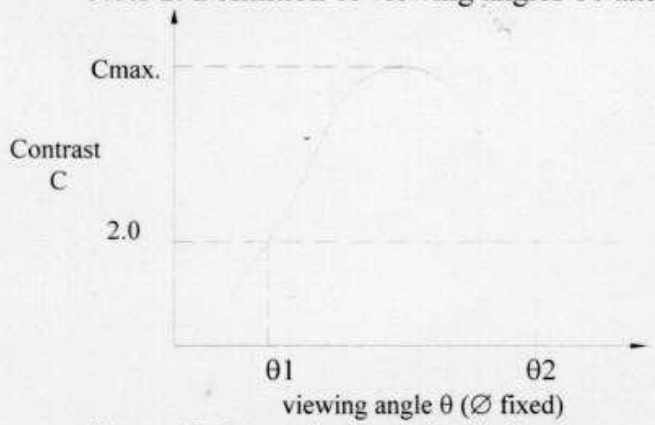
| Item | Symbol | Conditions | Min. | Typ. | Max | Reference |
|---|---|---|---|---|---|---|
| Viewing angle | θ | C≥2.0,∅=0° | 30° | - | - | Notes 1 & 2 |
| Contrast | C | θ=5°, ∅=0° | - | 3 | - | Note 3 |
| Response time(rise) | $T_r$ | θ=5°, ∅=0° | - | 140ms | 200ms | Note 4 |
| Response time(fall) | $T_f$ | θ=5°, ∅=0° | - | 300ms | 500ms | Note 4 |

| Parameter | Symbol | Temperature (°C) | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Driving voltage | $V_{OP}$ | -20 | 14.3 | 14.7 | 15.1 | V |
| | | 25 | 13.2 | 13.6 | 14.0 | |
| | | 70 | 12.0 | 12.4 | 12.8 | |

Note 1: Definition of angles θ and ∅



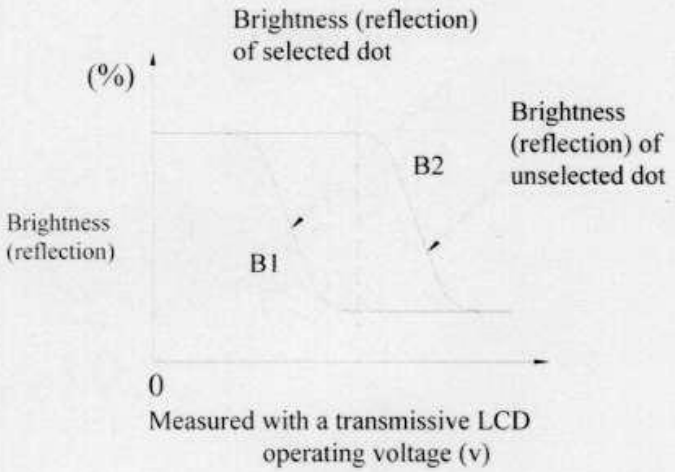

Note 2: Definition of viewing angles θ1 and θ2



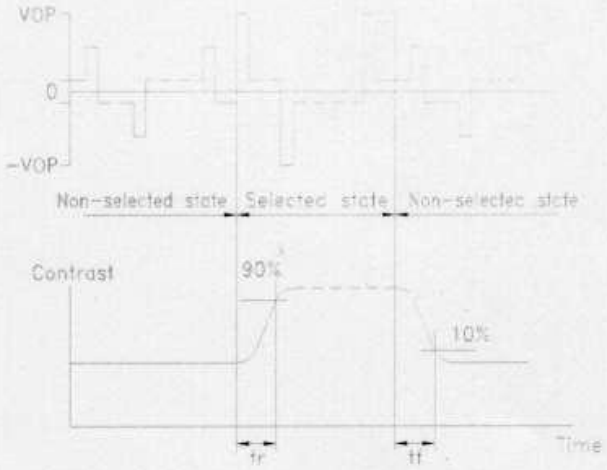

Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$




Note 4: Definition of response time




Note:

panel which is displayed 1 $cm^2$

$V_{OPR}$ : Operating voltage
$t_r$ : Response time (rise)
$f_{FRM}$ : Frame frequency
$t_f$ : Response time (fall)

# 2. MODULE STRUCTURE

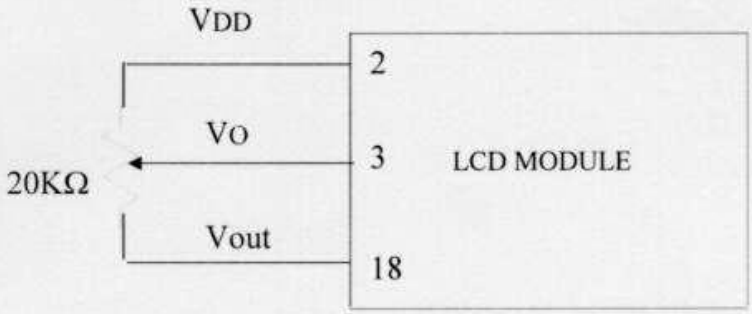
## 2.1 Counter Drawing

*See Appendix 1

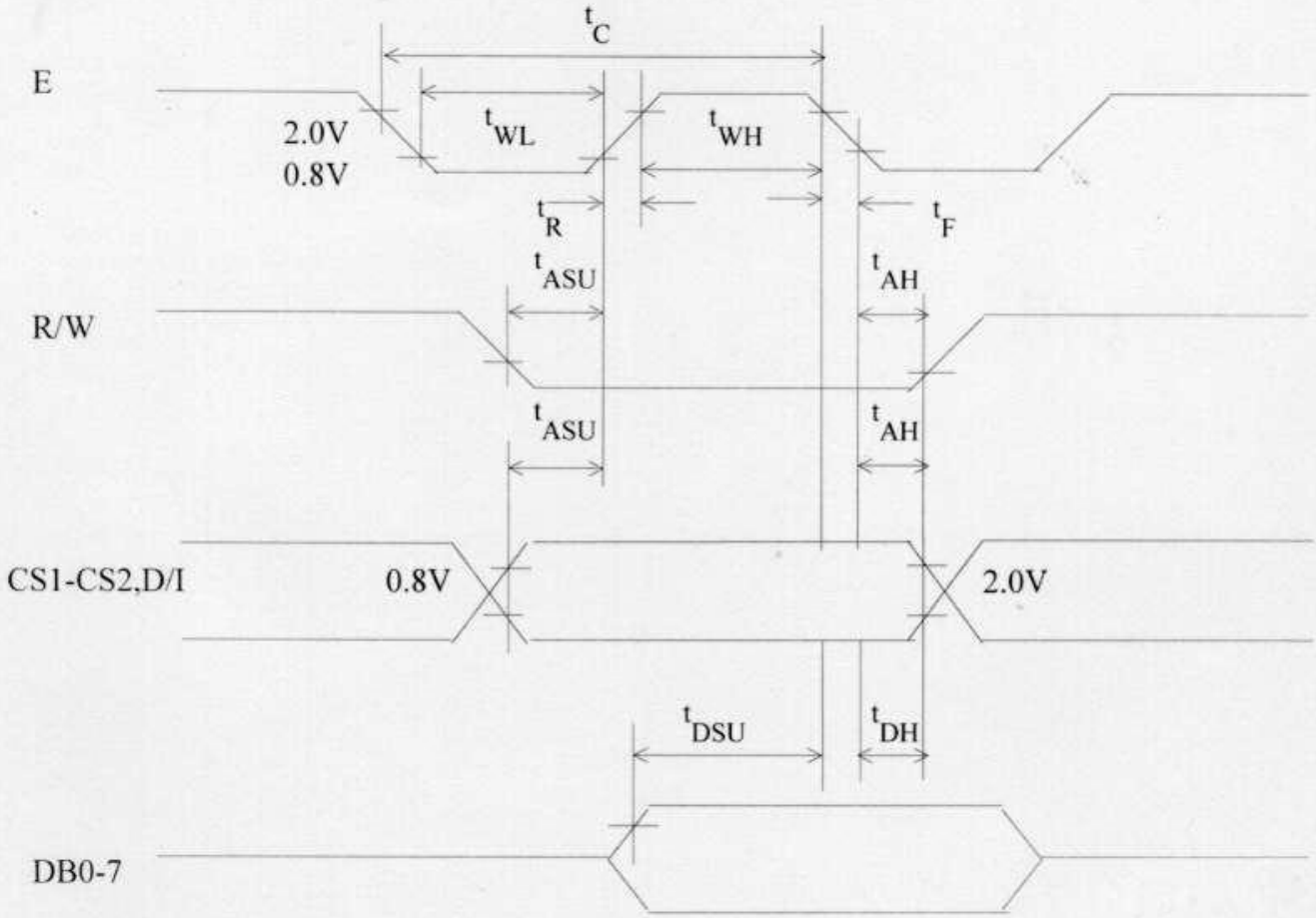
## 2.2 Interface Pin Description

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | $V_{SS}$ | Power Supply (Vss=0) |
| 2 | $V_{DD}$ | Power Supply ($V_{DD}$>$V_{SS}$) |
| 3 | $V_O$ | Operating voltage for LCD |
| 4 | D/$\overline{I}$ | Register selection input<br>High =Data register<br>Low =Instruction register (for write)<br>Busy flag address counter (for read) |
| 5 | R/$\overline{W}$ | R/$\overline{W}$ signal input is used to select the read/write mode<br>High =Read mode, Low =Write mode |
| 6 | E | Start enable signal to read or write the data |
| 7-10 | DB0~<br>DB3 | Four low order bi-directional three-state data bus lines. Use for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation. |
| 11-14 | DB4~<br>DB7 | Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module.<br>DB7 can be used as a busy flag. |
| 15 | CS1 | Chip enable for D2 (segment 1 to segment 64) |
| 16 | CS2 | Chip enable for D3 (segment 65 to segment 128) |
| 17 | $\overline{RST}$ | Reset signal |
| 18 | Vout | Negative voltage output |
| 19 | A | Power supply for LED backlight (+) |
| 20 | K | Power supply for LED backlight (-) |

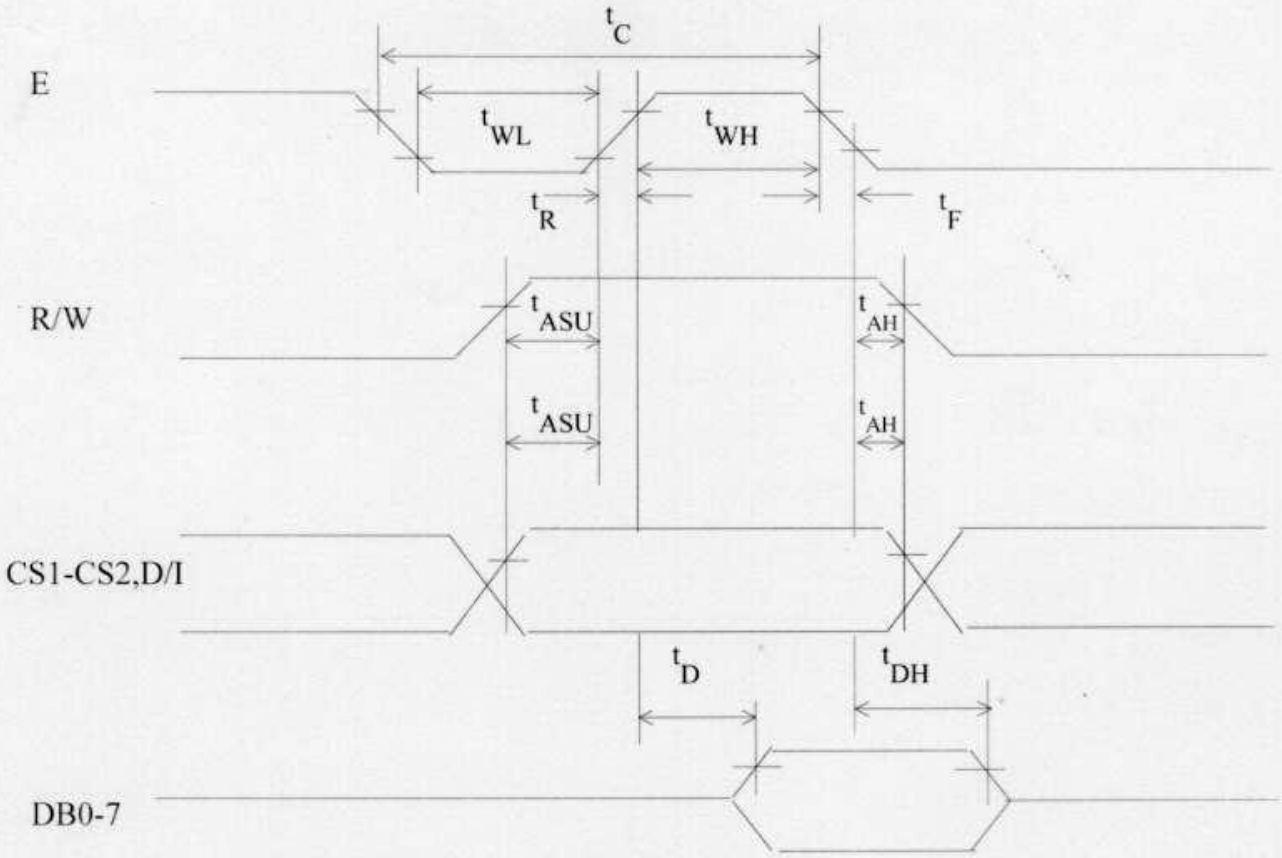
Contrast Adjust



## 2.3 Timing Characteristics




MPU write timing




MPU read timing

| Characteristic | Symbol | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|
| E Cycle | $t_C$ | 1000 | - | - | ns |
| E High Level Width | $t_{WH}$ | 450 | - | - | ns |
| E Low Level Width | $t_{WL}$ | 450 | - | - | ns |
| E Rise Time | $t_R$ | - | - | 25 | ns |
| E Fall Time | $t_F$ | - | - | 25 | ns |
| Address Set-Up time | $t_{ASU}$ | 140 | - | - | ns |
| Address Hold Time | $t_{AH}$ | 10 | - | - | ns |
| Data Set-Up Time | $t_{SU}$ | 200 | | - | ns |
| Data Delay Time | $t_D$ | - | - | 320 | ns |
| Data Hold Time (Write) | $t_{DHW}$ | 10 | - | - | ns |
| Data Hold Time (Read) | $t_{DHR}$ | 20 | - | - | ns |

## 2.4 Display command

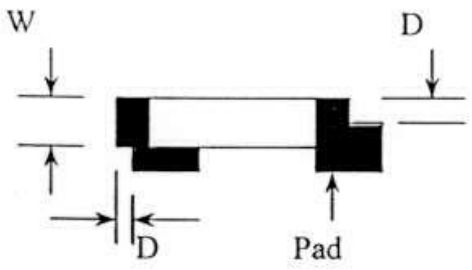
| Instructions | Code R/W | D/I | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Display on/off | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1/0 | Controls display on/off. RAM data and internal status are not affected. | |
| Display start line | 0 | 0 | 1 | 1 | Display start line (0-63) | | | | | | Specifies the RAM line displayed at the top of the screen. | |
| Set Page (x address) | 0 | 0 | 1 | 0 | 1 | 1 | 1 | Page (0-7) | | | Sets the page (X address) of RAM at the page (X address) register. | |
| Set Y address | 0 | 0 | 0 | 1 | Y address (0-63) | | | | | | Sets the Y address in the Y address in the counter. | |
| Status read | 1 | 0 | Busy | 0 | ON/OFF | Reset | 0 | 0 | 0 | 0 | Reads the status.<br>Reads 1: Reset<br>0: Normal<br>ON/OFF 1: Display off<br>0: Display on<br>Busy 1: Internal operation<br>0: Ready | |
| Write display data | 0 | 1 | Write data | | | | | | | | Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. | Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1. |
| Read display data | 1 | 1 | Read data | | | | | | | | Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus. | |

**Detailed Explanation**

**Display On/Off**

| | R/W | D/I | DB7 | | | | | | | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | D |
| | | | MSB | | | | | | | LSB |

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

| NO | Item | Specification | Judge | Level |
|---|---|---|---|---|
| 6 | Molding appearance<br>A=( L + W )÷ 2 | Too soft : Shape by touch changed | N.G. | Major |
| | | Insufficient epoxy : IC circuit or IC pad visible | N.G. | Minor |
| | | Excessive epoxy : Diameter > 20mm Or<br>High > 2.5mm | N.G. | Minor |
| | | Pin hole through to IC and A > 0.2mm | N.G. | Minor |
| 7 | Bezel appearance<br>A=( L + W )÷ 2 | Angle between frame and foot > 45° +10° | N.G. | Minor |
| | | Electroplate strip A > 1.0mm ( Top view only ) | N.G. | Minor |
| | | Rust ( Top view only ) | N.G. | Minor |
| | | Crack | N.G. | Minor |
| 8 | Backlight electric characteristics<br>A=( L + W )÷ 2 | Error backlight color | N.G. | Major |
| | | No function | N.G. | Major |
| | | Any LED dot no function | N.G. | Major |
| | | Solder connection of straight through termination does not meet minimum $270^0$ circumferential fillet or wetting | N.G. | Minor |
| | | 0.5mm>lead protrusion >2.3mm | N.G. | Minor |
| 9 | LCD Appearance | Polarize rise over V/A | N.G. | Minor |
| | | Rainbow A > 1/3 bezel V/A | N.G. | Minor |
| 10 | Assembly parts<br>A=( L + W )÷ 2 | Solder fillet extends onto the component body | N.G. | Minor |
| | | Error position not in center D > 1/2W<br>  <br> | N.G. | Minor |
| | | End joint width is less than 50% land dewetting or no wetted joint | N.G. | Minor |
| | | Component nick ,crack | N.G. | Minor |