POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

【產品規格書】

Customer : _____

Model Type : LCD Module

Sample Code : PG320240WRF-HNNHP2

Mass Production Code : _____

Edition : 0

Customer Sign	Sales Sign	Approved By	Prepared By

CONTENTS

1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 320 dots *240 dots
- 1/240 Duty, 1/14 bias
- FSTN LCD, positive, Black & White display
- Transflective LCD, 6 o'clock viewing angle
- 4 bits parallel data input
- With LED backlight

1.2 Mechanical Specifications

- Outline dimension : 92.0mm(W)*71.3mm(H)*7.9mm max.(D)
- Viewing area : 78.78mm *59.58mm
- Active area : 76.78mm *57.58mm
- Dot size : 0.22mm *0.22mm
- Dot pitch : 0.24mm *0.24mm
- Interface connector : 16-pin flat ribbon connector with 1mm pitch
- Driver ICs : TCP type

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	V_{DD}	Vss=0V	-0.3	7	V
	V_{EE}		-0.3	32	V
Input voltage	V_{IN}		-0.3	V_{DD}+0.3	V
Operating temperature	Topr		-20	70	°C
Storage temperature	Tstg		-30	80	°C
Humidity	H_D		20	70	%RH

1.4 DC Electrical Characteristics

V_{DD}=+5V±10% , V_{SS}=0V,Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	V_{DD}	-	2.5	5.0	5.5	V
"H" input voltage	V_{IH}	-	0.8 V_{DD}	-	-	V
"L" input voltage	V_{IL}	-	-	-	0.2 V_{DD}	V
"H" output voltage	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	-	V
"L" output voltage	V_{OL}	I_{OL}=+0.4mA	-	-	+0.4	V
Supply current	I_{DD}	V_{DD}=5V	-	1.4	1.6	mA

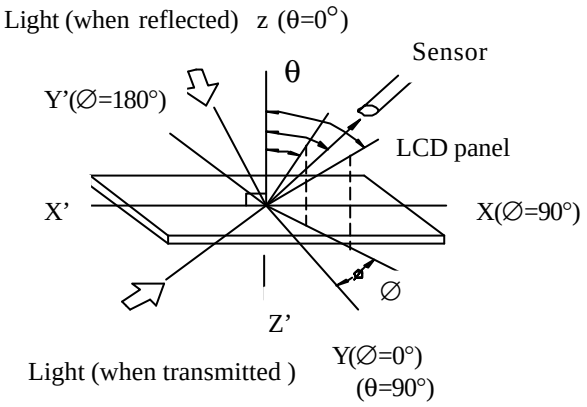
LCD driving voltage	VLCD	Ta=25°C	-	21.6	21.8	V

1.5 Optical Characteristics

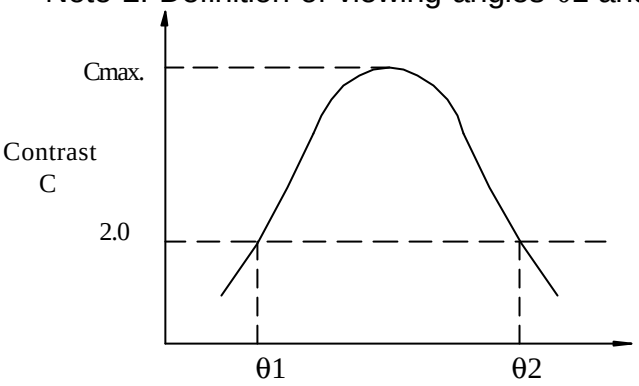
Vopr=24.8V, 1/240 duty, 1/17 bias, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	C≥2.0,∅=0°	-25°	-	25°	Notes 1 & 2
Contrast	C	θ=0°, ∅=0°	-	2.8	-	Note 3
Response time(rise)	tr	θ=0°, ∅=0°	-	150ms	169ms	Note 4
Response time(fall)	tf	θ=0°, ∅=0°	-	240ms	249ms	Note 4

Note 1: Definition of angles θ and ∅



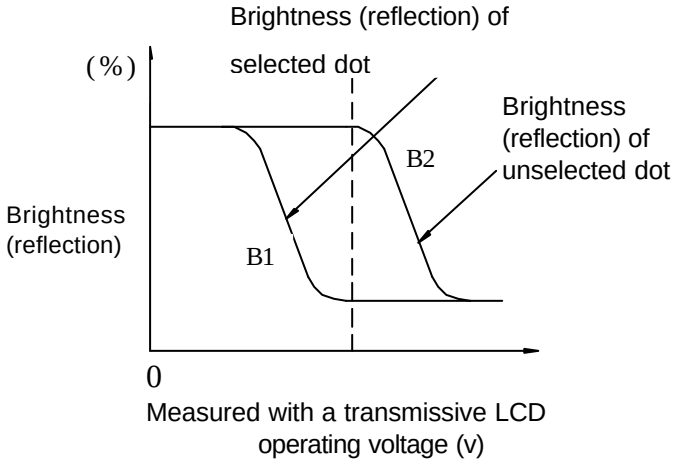
Note 2: Definition of viewing angles θ1 and θ2



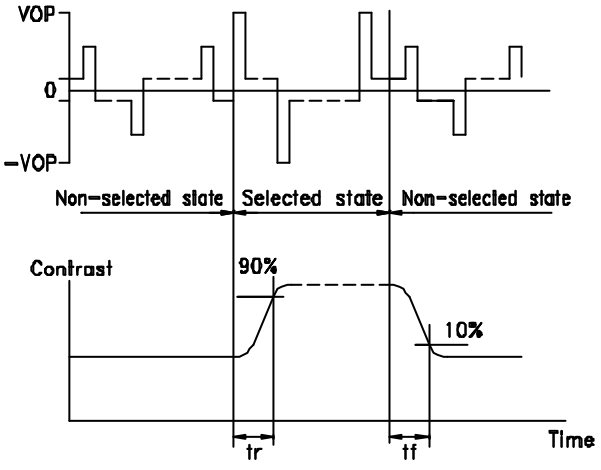
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note:

panel which is displayed 1 cm²

V_{OPR} : Operating voltage f_{FRM} : Frame frequency
t_{ON} : Response time (rise) t_{OFF} : Response time (fall)

1.6 Backlight Characteristic

The LCD Module is built-in an White LED backlight.

Absolute Maximum Ratings: (Ta=25°C)

Item	Symbol	Ratings	Unit
Peak forward current	IF	120	mA
Reverse voltage	VR	5	V
Power dissipation	Po	0.48	W
Operating temperature	Topr	-20 to +70	°C
Storage temperature	Tstg	-40 to +80	°C
Soldering temperature: 3 sec.		260	°C

Electrical/Optical specifications:

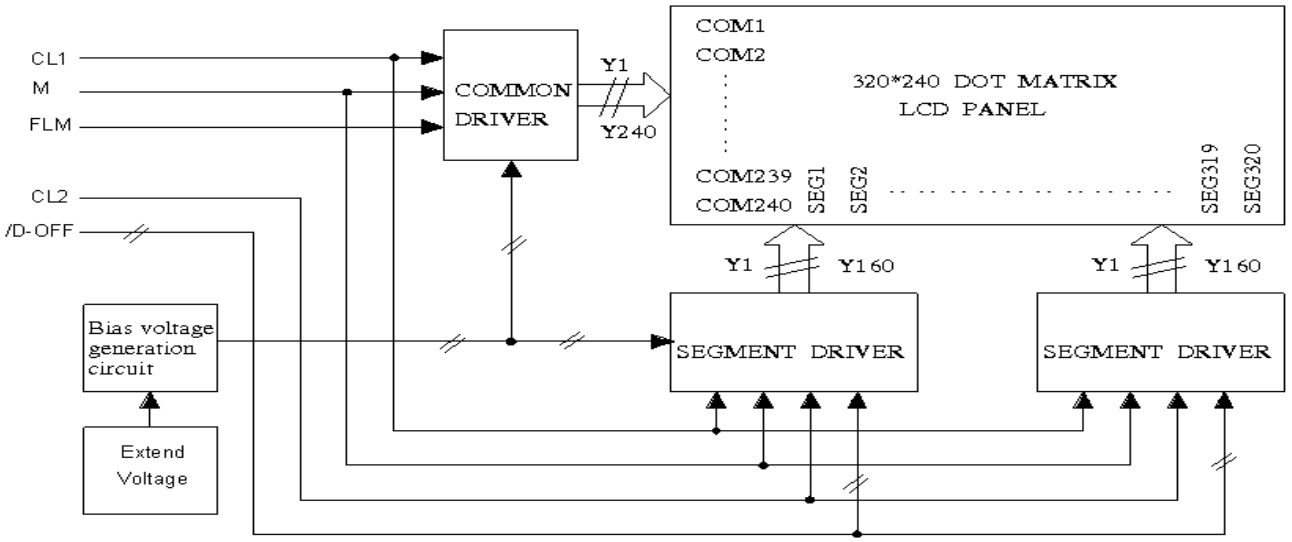
ITEM	Symbol	Condition	Min.	Typ	Max.	Unit
Forward Voltage	V_f	I_f= 60mA	-	3.3	4.0	V
Reverse Current	I_r	V_r= 5V	-	-	0.2	mA
Luminous Intensity (with LCD)	I_V	I_f= 80mA	5.0	8.0	-	cd/m^2
Color Coordinate	X	I_f= 60mA		0.29		
	Y			0.30		
Color	White					

2.MODULE STRUCTURE

The PG320240-H includes a common driver, two segment drivers, a bias voltage generation circuit, and LED backlight.

2.1 Driver ICS

- Segment driver : IST3021F3*2 or ST8016F3*2 or LH1565F3*2
- Common driver : IST3022F4*1 or ST8024F4*1 or LH1562F4*1
- Block diagram



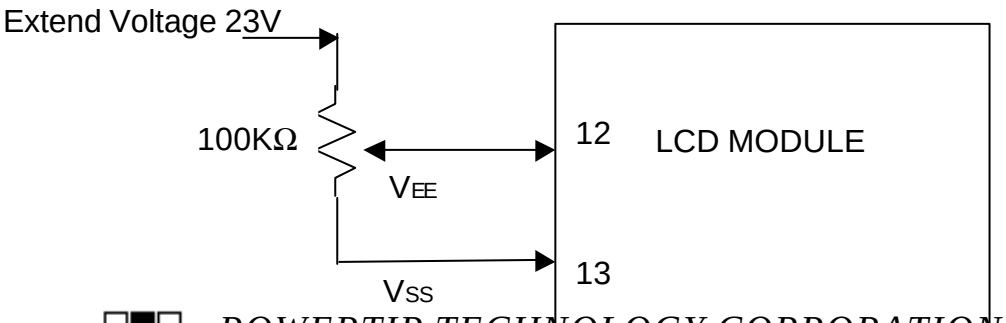
2.2 Interface Pin Description

PIN	SIGNAL NAME	DESCRIPTION
1	FLM	Indicates the beginning of each display cycle.
2	M	AC signal input for LC driving waveform
3	CL1	Bi-directional shift register shift clock pulse input pin.
4	CL2	Clock input pin for taking display data
5	/D-OFF	Control input pin for output deselect level
6	DB0	Display data input pin
7	DB1	Display data input pin
8	DB2	Display data input pin
9	DB3	Display data input pin
10	V_{DD}	Logic system power supply pin
11	V_{SS}	Ground pin
12	V_{EE}	LCD Operator Voltage
13	V_{SS}	Ground pin
14	NC	No connection
15	A	Power supply for LED Backlight (+)
16	K	Power supply for LED Backlight (-)

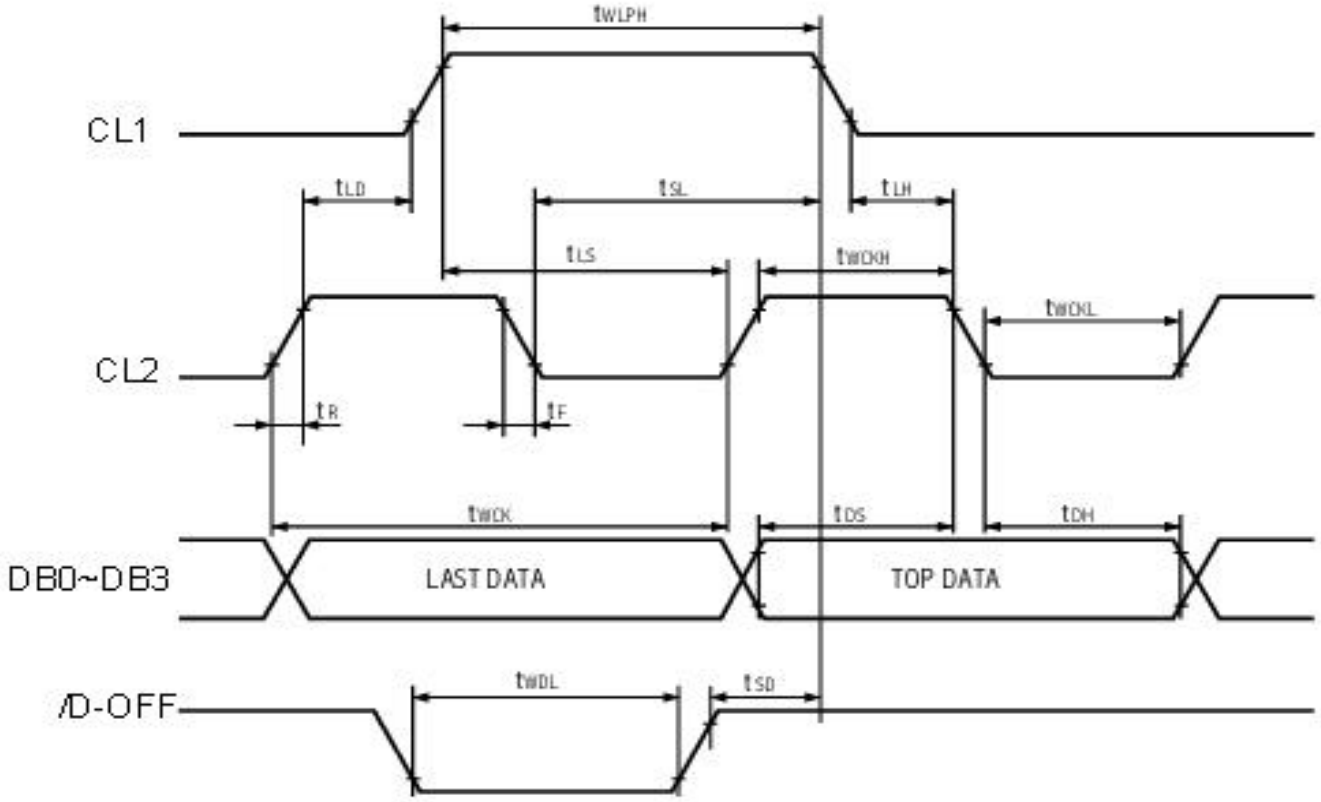
Note : FLM Recommended 55Hz ~ 75Hz

M Recommended 200Hz ~ 400Hz

Contrast Adjust



2.3 Timing Characteristics

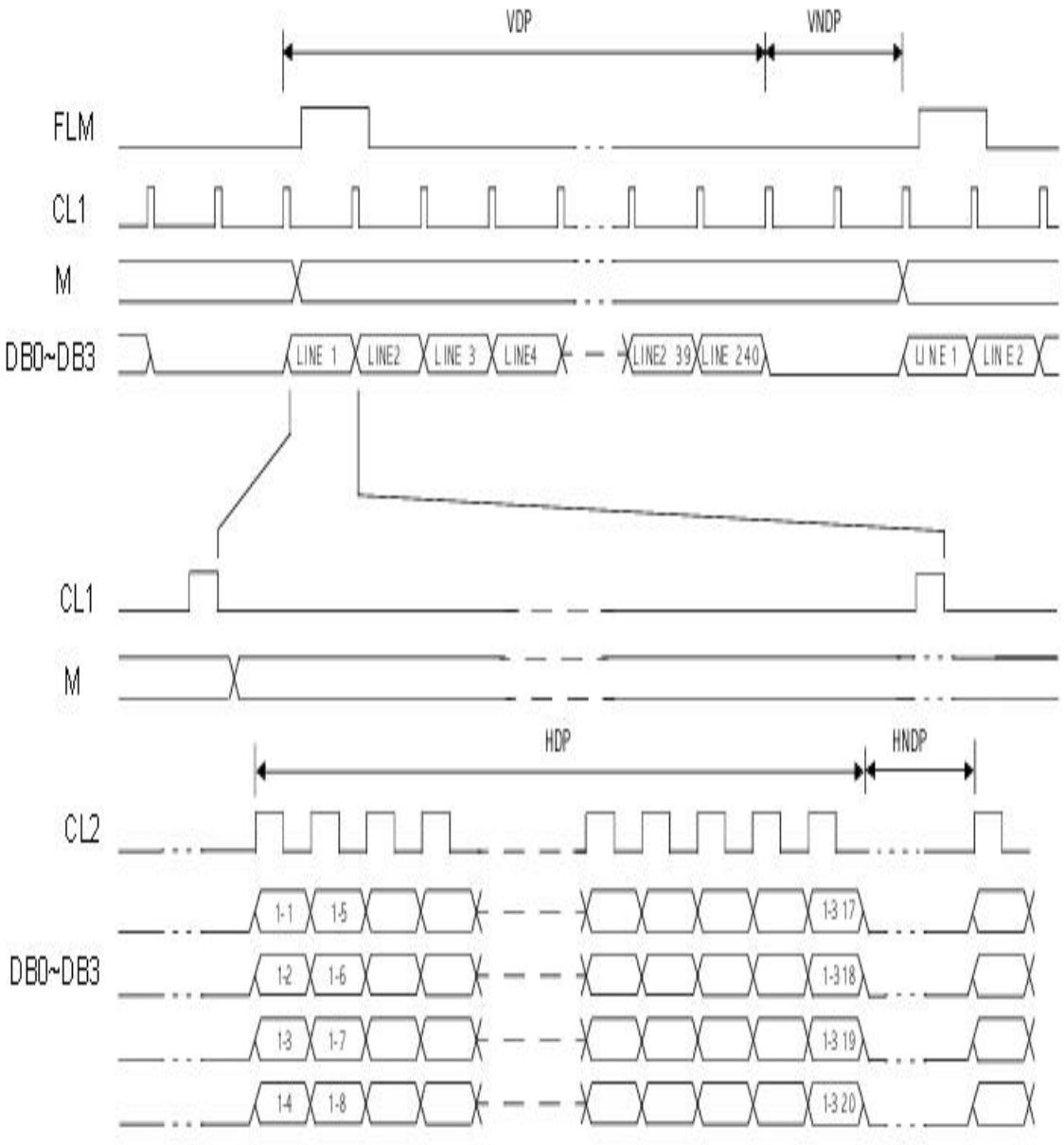


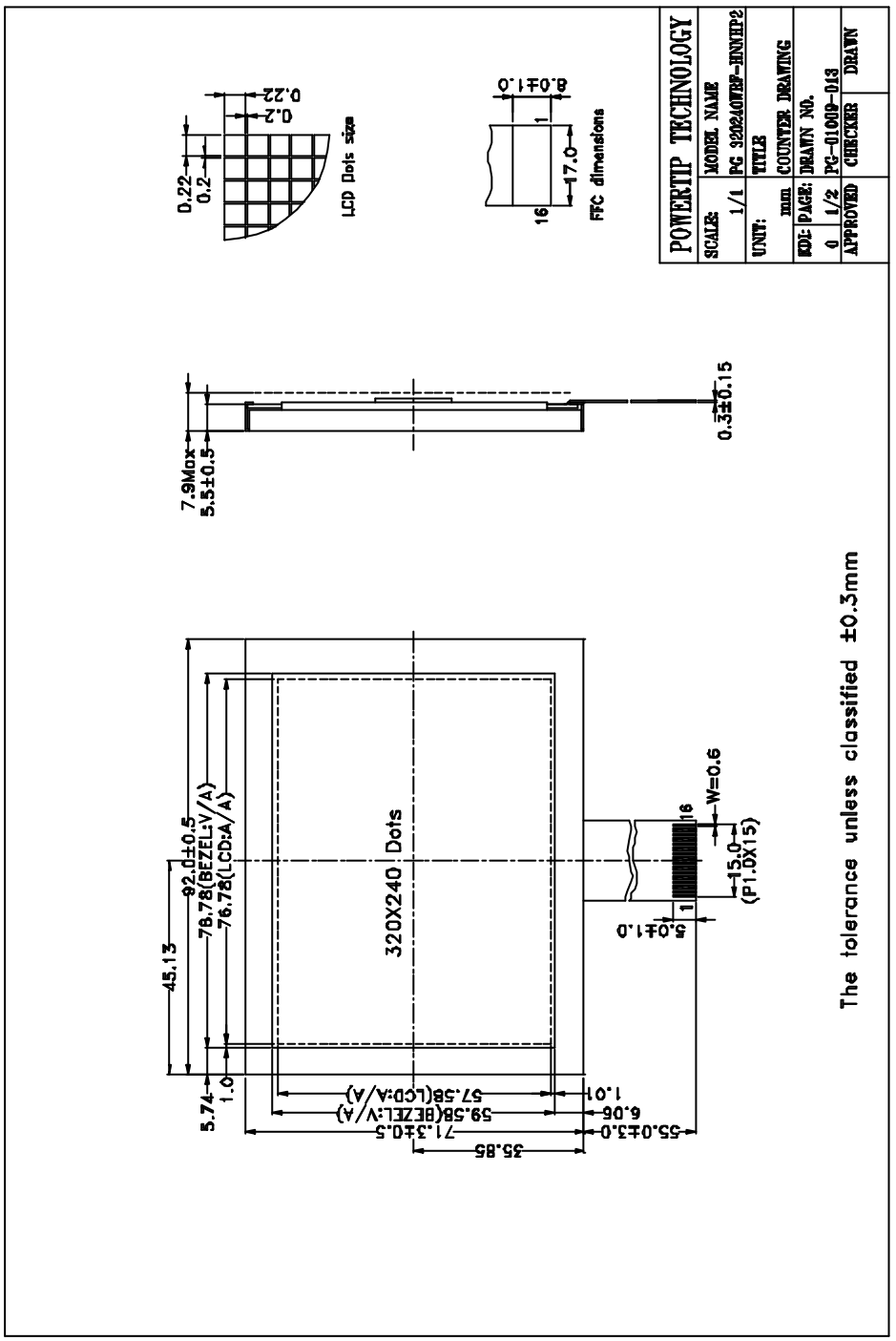
Vss=0V, Vdd=2.5V to 5.5V, Ta=25℃

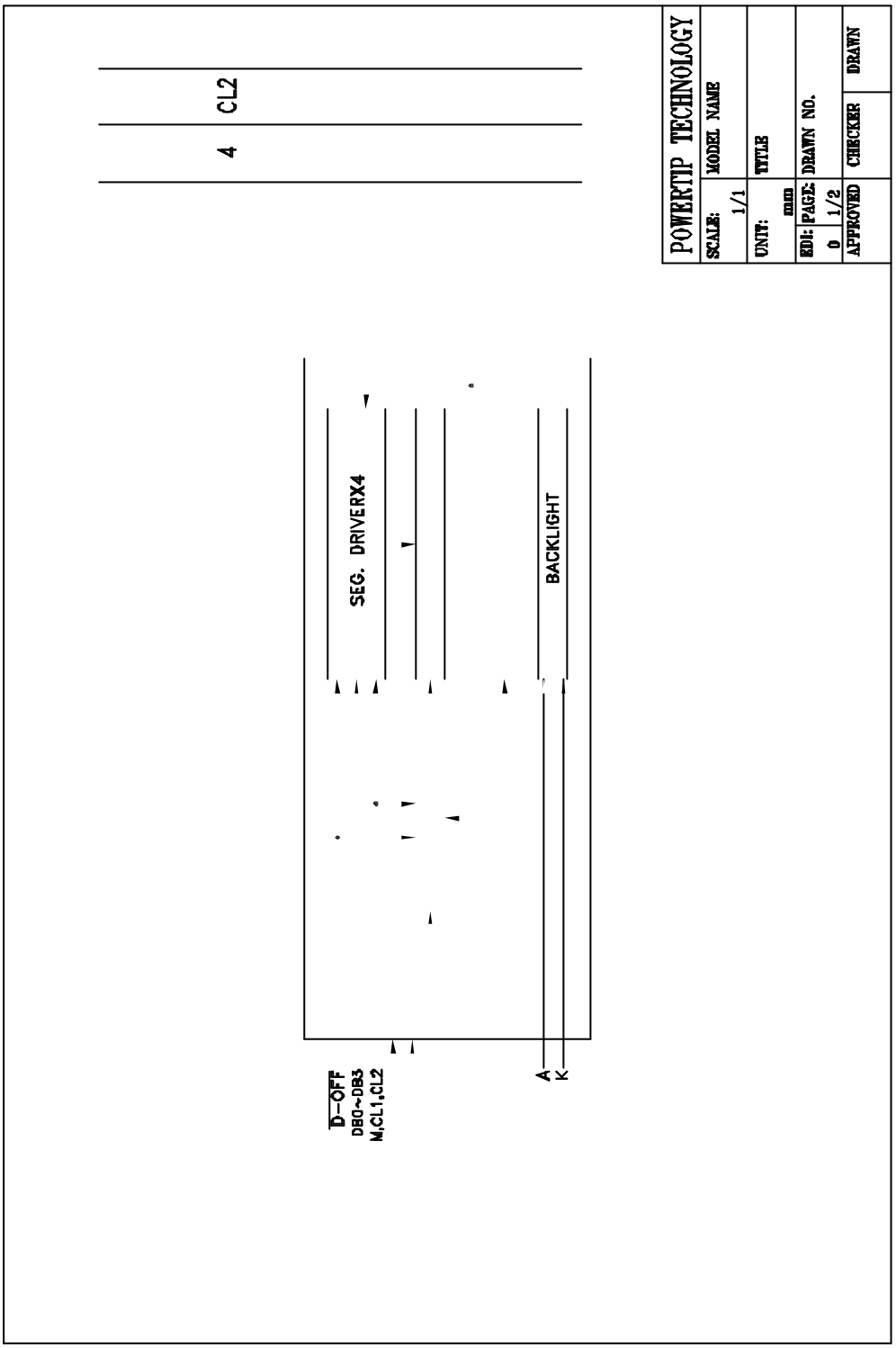
Parameter	Symol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{WCK}	$t_r, t_f \leqq 11$ ns	125			ns
Shift clock “H” pulse width	t_{WCKH}		51			ns
Shift clock “L” pulse width	t_{WCKL}		51			ns
Data setup time	t_{DS}		30			ns
Data hold time	t_{DH}		40			ns
Latch pulse “H” pulse width	t_{WLPH}		51			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		51			ns
Latch pulse rise to Shift clock rise time	t_{LS}		51			ns
Latch pulse fall to Shift clock fall time	t_{LH}		51			ns
Input signal rise time	t_r				50	ns

Input signal fall time	t_f				50	ns
/Dispoff removal time	t_{SD}		100			ns
/Dispoff “L” pulse width	t_{WDL}		1.2			us
Output delay time (1)	t_{pd1},t_{pd2}	CL=15 pF			1.2	us
Output delay time (2)	t_{pd3}	CL=15 pF			1.2	us

4 Bits Panel Timing


VDP
VNDP
FLM
CL1
M
DB0~DB3
LINE 1
LINE2
LINE 3
LINE4
LINE2 39
LINE 240
LINE 1
LINE 2
CL1
M
HDP
HNDP
CL2
DB0~DB3
1-1
1-5
1-317
1-2
1-6
1-318
1-3
1-7
1-319
1-4
1-8
1-320


POWERTIP TECHNOLOGY
SCALE: 1/1
MODEL NAME: PG 320240WRF-HNNHP2
UNIT: mm
TITLE: COUNTER DRAWING
DWG: 0
PAGE: 1/2
DRAWN NO.: PG-01009-013
APPROVED
CHECKER
DRAWN
LCD Dots size
FFC dimensions
7.9Max
5.5±0.5
0.3±0.15
320X240 Dots
92.0±0.5
78.78(BEZEL:V/A)
76.78(LCD:A/A)
45.13
5.74
1.0
57.58(LCD:A/A)
59.58(BEZEL:V/A)
71.3±0.5
55.0±3.0
35.85
1.01
6.06
W=0.6
15.0
(P1.0X15)
5.0±1.0
8.0±1.0
17.0
The tolerance unless classified ±0.3mm


POWERTIP TECHNOLOGY
SCALE: 1/1
MODEL NAME
UNIT: mm
TITLE
ED: 0
PAGE: 1/2
DRAWN NO.
APPROVED
CHECKER
DRAWN
4 CL2
SEG. DRIVERX4
BACKLIGHT
A
K
D-OFF
DB0~DB3
M,CL1,CL2