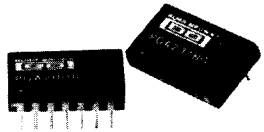
BURR-BROWN®

PGA200/201



Digitally-Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

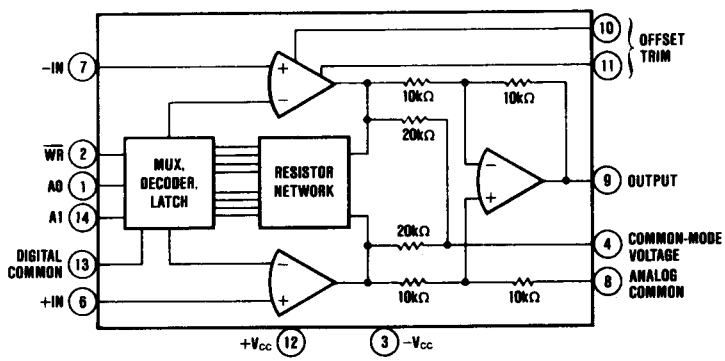
- DIGITALLY-PROGRAMMABLE GAIN
  - Decade Model - PGA200
    Gains of 1, 10, 100, 1000
  - Binary Model - PGA201
    Gains of 1, 8, 64, 512
- EXCELLENT GAIN ACCURACY (0.02%, max)
- LOW GAIN NONLINEARITY (0.012%, max; G = 1000)
- LOW GAIN DRIFT (10ppm/°C, max; G = 1000)
- 2-BIT LATCHED TTL-COMPATIBLE GAIN CONTROL
- LOW OFFSET VOLTAGE (25μV RTI, max; G = 1000)
- LOW OFFSET VOLTAGE DRIFT (0.30μV/°C, max; G = 1000)

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- SYSTEM DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION SYSTEM
- TEST EQUIPMENT

DESCRIPTION

The PGA200 is a hybrid IC instrumentation amplifier with digitally-controlled decade gain steps of 1, 10, 100, and 1000. The PGA201 differs only by providing binary steps of 1, 8, 64, and 512. Both have TTL-compatible latched inputs for microprocessor interface. The logic section has high input impedance and functions without a separate logic power supply. Precision laser-trimmed offset and gain permits use without external adjustments. High performance thin-film resistors with excellent tracking assure low gain drift and excellent stability.



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PDS-522B

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply unless otherwise noted.

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN								
Inaccuracy[2] G = 1			0.02	0.05		0.01	0.02	%
G = 10			0.02	0.05		0.01	0.02	%
G = 100			0.02	0.05		0.01	0.02	%
G = 1000			0.02	0.05		0.01	0.02	%
Nonlinearity, G = 1			0.002	0.005		0.001	0.002	%
G = 10			0.002	0.005		0.001	0.002	%
G = 100			0.003	0.007		0.002	0.003	%
G = 1000			0.012	0.025		0.011	0.012	%
Drift vs Temperature, G = 1			10	20		5	10	ppm/°C
G = 10			10	20		5	10	ppm/°C
G = 100			10	20		5	10	ppm/°C
G = 1000			10	20		5	10	ppm/°C
Stability vs Time			0.01			•		%/1khr
RATED OUTPUT								
Voltage	I_O = 5mA	10	12.5		•	•		V
Current	V_O = 10V	5	10.0		•	•		mA
Impedance			0.3			•		Ω
Capacitive Load			1000			•		pF
ANALOG INPUT CHARACTERISTICS								
Common-Mode Range		10			•			V
Absolute Maximum Voltage	No Damage			V_{CC}			•	V
Impedance, Differential			10^{10} ‖ 3			•		Ω ‖ pF
Common-Mode			10^{10} ‖ 3			•		Ω ‖ pF
OFFSET VOLTAGE (RTI)								
Initial Offset, max[3], G = 1			225	450		110	225	µV
G = 10			45	90		20	45	µV
G = 100			27	54		11	27	µV
G = 1000			25	50		10	25	µV
vs Temperature, G = 1			10	22		5	10	µV/°C
G = 10			2	4		0.75	1.5	µV/°C
G = 100			1	2		0.20	0.40	µV/°C
G = 1000			1	2		0.15	0.30	µV/°C
vs Time			1 + (20/G)			•		µV/mo
vs Supply	10 < V_{CC} < 18V		1 + (20/G)			•		µV/V
INPUT BIAS CURRENT								
Initial at 25°C	Each input		10	30		5	20	nA
vs Temperature			0.2			•		nA/°C
vs Supply			0.1			•		nA/V
Offset Current			10	30		5	20	nA
vs Temperature			0.5			•		nA/°C
COMMON-MODE REJECTION								
G = 1	DC to 60Hz,	80	95		•	•		dB
G = 10	1kΩ Source	96	110		•	•		dB
G = 100	Imbalance	106	120		•	•		dB
G = 1000		106	120		•	•		dB
INPUT NOISE[4]								
Input Voltage Noise, f_B = 0.1Hz to 10Hz			0.8			•		µV, p-p
Density, f_o = 10Hz			18			•		nV/√Hz
f_o = 100Hz			15			•		nV/√Hz
f_o = 1kHz			13			•		nV/√Hz
Input Current Noise, f_B = 0.1Hz to 10Hz			50			•		pA, p-p
Density, f_o = 10Hz			0.8			•		pA/√Hz
f_o = 100Hz			0.46			•		pA/√Hz
f_o = 1kHz			0.35			•		pA/√Hz
DYNAMIC RESPONSE								
±3dB Flatness	Small signal							
G = 1			500			•		kHz
G = 10			150			•		kHz
G = 100			30			•		kHz
G = 1000			2.4			•		kHz
±1% Flatness	Small signal							
G = 1			50			•		kHz
G = 10			25			•		kHz
G = 100			3			•		kHz
G = 1000			300			•		Hz

ELECTRICAL (CONT)

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DYNAMIC RESPONSE								
±1% Flatness	Small signal							
G = 1			50			•		kHz
G = 10			25			•		kHz
G = 100			53			•		kHz
G = 1000			300			•		Hz
Full Power	G = 1 to 100		6.4			•		kHz
Slew Rate	G = 1 to 100	0.2	0.4			•		V/µsec
Settling Time (0.1%), G = 1			35			•		µsec
G = 10			35			•		µsec
G = 100			50			•		µsec
G = 1000			480			•		µsec
Settling Time (0.01%), G = 1			40			•		µsec
G = 10			40			•		µsec
G = 100			80			•		µsec
G = 1000[5]			670			•		µsec
Overload Recovery Time	50% overdrive							
G = 1 to 100			12			•		µsec
G = 1000			22			•		µsec
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold				0.8			•	V
Input Low Current				30			•	µA
Input High Threshold		2.4			•			V
Input High Current				30			•	µA
T_{WW}, Write Pulse Width		300			•			nsec
T_S, Data Setup Time		180			•			nsec
T_H, Data Hold Time		30			•			nsec
POWER SUPPLY								
Rated Voltage			±15			•		V
Voltage Range		10		18	•		•	V
Quiescent Current			±10	±12		•	•	mA
TEMPERATURE RANGE								
Specification		−40		+85	•		•	°C
Operating		−55		+125	•		•	°C
Storage		−55		+150	•		•	°C

*Specifications same as for PGA200/201AG.

NOTES: (1) All specifications pertain to both PGA200 and PGA201. Values for gains of 10, 100, and 1000 for the PGA200 are the same for gains of 8, 64 and 512. (2) Measured with a 10kΩ load. (3) Adjustable to zero. This offset is the total offset including both input and output components referred to the input. (4) Noise due to the input stage. There is also an output component which becomes significant in low gain (see Typical Performance Curves). (5) Settling time of the average value of the output waveform since the noise floor in a gain of 1000 is on the order of 0.01% of full scale.

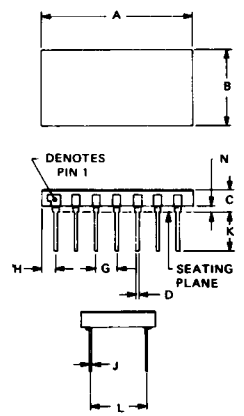
ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation 600mW
Analog And Digital Inputs ..... ±Vcc
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... +300°C
Output Short-Circuit Duration ..... Continuous To Ground
Junction Temperature ..... 175°C

PIN DESIGNATIONS

1. AO
2. $\overline{WR}$
3. −Vcc
4. Common-Mode Voltage
5. NC
6. +IN
7. −IN
8. Analog Common
9. Output
10. Offset Trim
11. Offset Trim
12. +Vcc
13. Digital Common
14. A1

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	.38	.89

BURN-IN SCREENING

Burn-in screening is an option available for the PGA200 and PGA201. Burn-in duration is 160 hours at +125°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ORDERING INFORMATION

Model	Package	Temperature Range
PGA200AG	Ceramic DIP	-55°C to +125°C
PGA200BG	Ceramic DIP	-55°C to +125°C
PGA201AG	Ceramic DIP	-55°C to +125°C
PGA201BG	Ceramic DIP	-55°C to +125°C

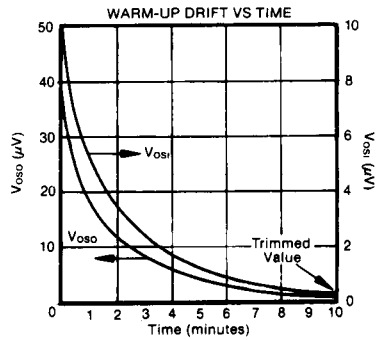
BURN-IN SCREENING OPTION
See text for details.

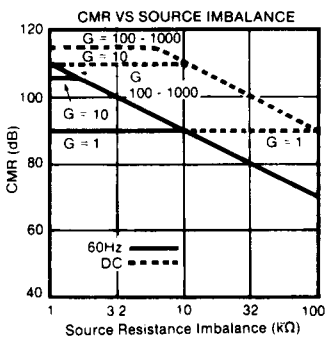
Model	Package	Burn-In Temp. (160h)[1]
PGA200AG-BI	Ceramic DIP	+125°C
PGA200BG-BI	Ceramic DIP	+125°C
PGA201AG-BI	Ceramic DIP	+125°C
PGA201BG-BI	Ceramic DIP	+125°C

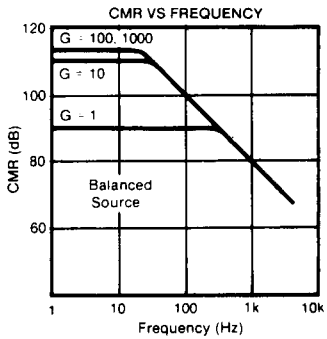
NOTE: Or equivalent combination. See text.

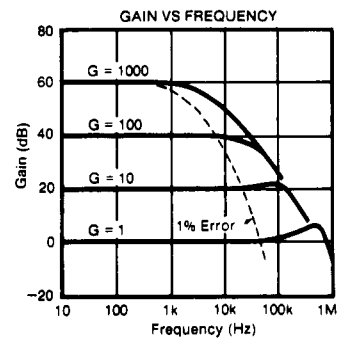
TYPICAL PERFORMANCE CURVES

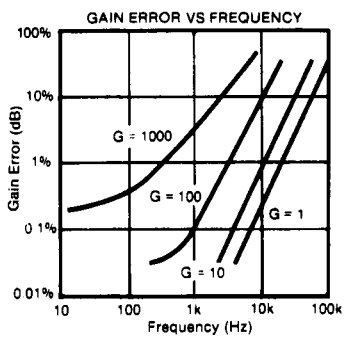
T_A = +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted.

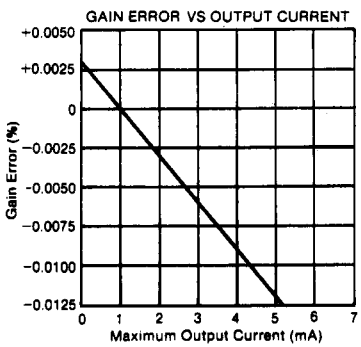


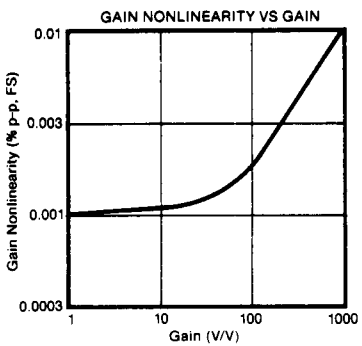


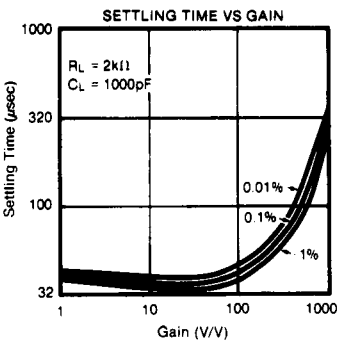


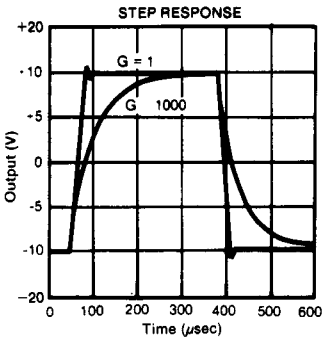


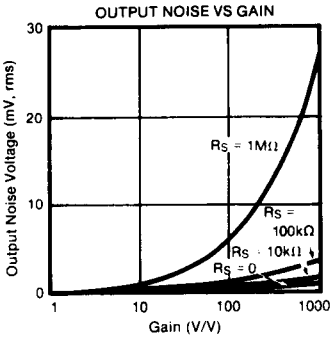


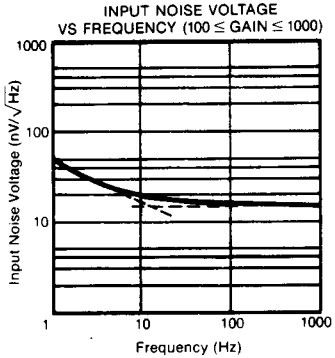


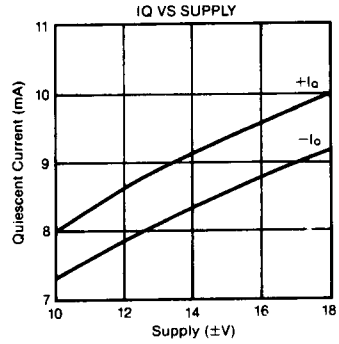












THEORY OF OPERATION

A simplified block diagram of the PGA200/201 appears on the first page. The diagram consists of three distinct parts. Together these parts form a high-perfomance, differential-input, digitally-programmable dedicated gain block. Each of the parts is optimized for a specific function.

The operational amplifiers are arranged on a monolithic substrate in the classical three-op-amp IA configuration. A nitride-passivated compatible thin-film bipolar process is used to achieve excellent offset and common-mode rejection stability over time and temperature. Advanced laser trimming techniques are used to minimize both the initial input offset and the input offset drift which are typically below 10μV and 0.15μ/V°C respectively. Additionally, careful layout techniques assure input stage thermal tracking with varying load conditions.

The gain-setting resistors are arranged on a separate substrate which is thermally isolated from the output stage. This results in minimum thermal interaction and a layout optimized for resistor tracking. All gains are dependent on the ratio of resistors which are composed of combinations of equal valued segments. The segmented approach provides the ultimate in accuracy and stability.

The latch and multiplexer, which set the gain, are implemented in CMOS. This provides high impedance logic inputs, low quiescent current and TTL compatibility without the need for a separate logic power supply. The logic threshold is internally derived from the +V_{CC} power supply and is referenced to digital common. The circuit is arranged so that multiplexer ON resistance is in series with the high input impedance of the input amplifiers and hence contributes negligible gain error.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors with connections made as close as possible to the amplifier supply terminals and load common connection.

Because the amplifier is direct-coupled, it must have a ground return path for the bias currents associated with the amplifier inputs at pins 6 and 7. If the ground return path is not inherent in the signal source (floating source), it must be provided externally. The ground return resistance (R_{gr}) should be kept as low as practical. The upper limit is approximately 50MΩ because of the input bias current of the amplifier and its common-mode voltage range.

In order to maintain linear operation of the input amplifiers the common-mode input voltage must be kept within the following limits:

$$-10V + (E_{in} \times G)/2 < E_{cm} < +10V - (E_{in} \times G)/2.$$

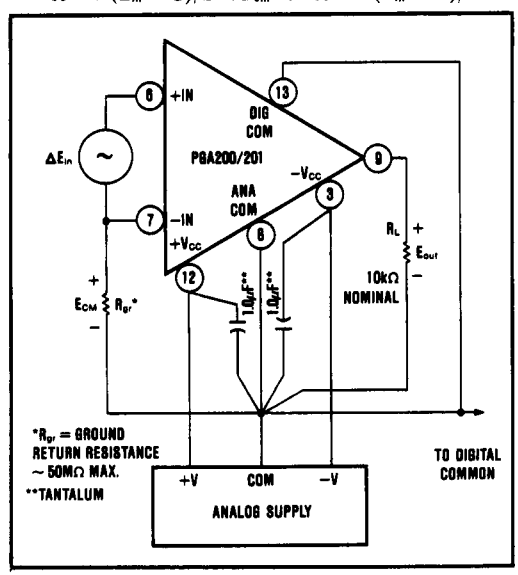


FIGURE 1. Power Supply and Signal Connections.

GAIN SETTING

Gain is determined by a 2-bit digital word applied to the A0 and A1 inputs (see Table I). The $\overline{WR}$ (pin 2) provides a latch function. When $\overline{WR}$ is a logic low, the latch is transparent and the gain directly follows the code on A0 and A1. When $\overline{WR}$ goes to a logic high, the gain is latched according to the previous state of A0 and A1. The timing requirements illustrated in Figure 2 must be observed. The minimum write pulse width is 300nsec while the data setup and hold times are 180nsec and 30nsec respectively. Although the logic inputs are TTL compatible, they are high impedance and the allowable logic high voltage extends to $+V_{CC}$.

Table I shows the gain select truth table. The gains for the PGA201 are shown in parenthesis.

TABLE I. Gain Select Truth Table.

A1	A0	$\overline{WR}$	GAIN PGA200 (PGA201)
X	X	⎍	Maintains previous gain
0	0	0	1 (1)
0	1	0	10 (8)
1	0	0	100 (64)
1	1	0	1000 (512)

Logic "1": $V_{AH} \geq 2.4V$
Logic "0": $V_{AL} \leq 0.8V$

INPUT AND OUTPUT OFFSETTING

Figure 3 illustrates the appropriate connections for offset adjustment. Since the instrumentation amplifier is a two-stage device, the total offset is composed of two parts, an input and an output component. Because both are actively laser trimmed, adjustment is not required in most applications. The input component is due to the mismatch in the offset voltage of the two input amplifiers and changes with gain. The output component is due to the offset of the second stage amplifier and is constant.

R_1 may be used to null the input offset. Its quality will affect the results; therefore, choose a potentiometer with good temperature and mechanical resistance stability. The wiper should be connected to $+V_{CC}$ at a point as close as possible to the $+V_{CC}$ terminal of the instrumentation amplifier. Null the offset as follows:

1. Set $E_1 = E_2 = 0$ (be sure a good ground return path exists to the inputs).
2. Set the gain to 1000 (or 512 for PGA201).
3. Adjust R_1 until the output reaches 0V ±1mV or desired value.

Input offset adjustment will affect the offset drift by approximately 3.1μV/°C/mV of offset that is trimmed. This effect can be greatly reduced by using the alternate offset adjust circuit shown inside the dashed line.

The output offset may be nulled or, alternately, the output can be level shifted with R_4. R_2 and R_3 divide the wiper voltage of R_4 down for increased sensitivity. Their ratio may be changed in order to increase the range of adjustment if desired. The buffer amplifier is required in order to keep the impedance at pin 8 low so that the gain and common-mode rejection will not be disturbed.

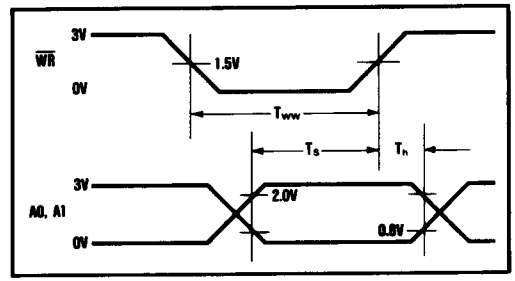


FIGURE 2. Timing Diagrams.

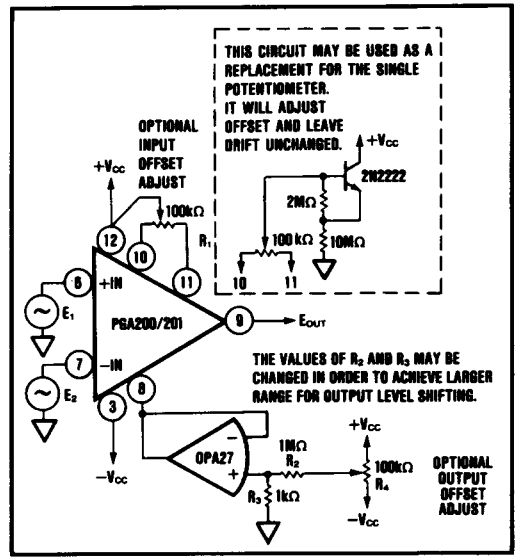


FIGURE 3. Optional Input/Output Offset Adjust.

GUARD DRIVE

Use of the guard drive connection in Figure 4 can improve system common-mode rejection when the

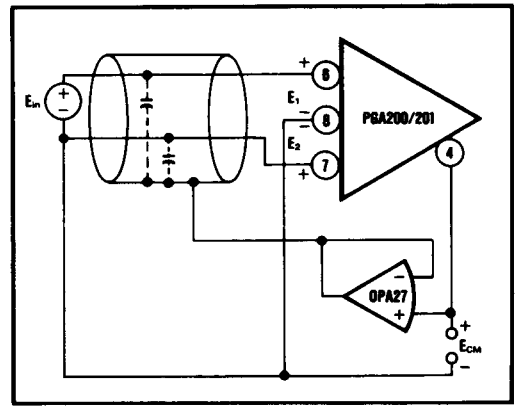


FIGURE 4. Guard Drive.

distributed capacitance of the input lines is significant. The common-mode voltage which appears on pin 4 is resistively derived from the output of the first stage amplifiers and has the value $(E_1 - E_2)/2$. This voltage is used to drive the shield which preferably should extend up to and around the input pins 6 and 7. This configuration improves common-mode rejection by reducing the common-mode current flow. The buffer amplifier is used in order to supply more current than the internal 20kΩ resistors can provide so that the guard can accurately track the actual common-mode voltage.

TYPICAL APPLICATIONS

The PGA200 and PGA201 are ideal for computer-controlled data acquisition systems as shown in Figure 5.

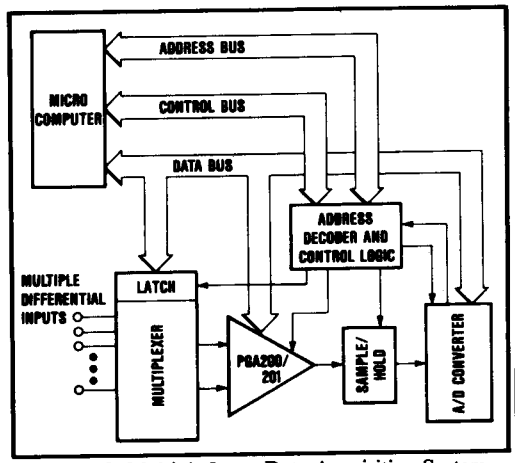


FIGURE 5. Multiple Input Data Acquisition System With Various Input Ranges.