PGA2311
Stereo Audio Volume Control

1 Features

- Digitally-Controlled Analog Volume Control:
  - Two Independent Audio Channels
  - Serial Control Interface
  - Zero Crossing Detection
  - Mute Function
- Wide Gain and Attenuation Range: +31.5 dB to −95.5 dB with 0.5-dB Steps
- Low Noise and Distortion:
  - 120-dB Dynamic Range
  - 0.0004% THD+N at 1 kHz (U-Grade)
  - 0.0002% THD+N at 1 kHz (A-Grade)
- Noise-Free Level Transitions
- Low Interchannel Crosstalk: −130 dBFS
- Power Supplies: ±5-V Analog, +5-V Digital
- Available in PDIP-16 and SOIC-16 Packages
- Pin- and Software-Compatible With the Crystal CS3310

2 Applications

- Audio Amplifiers
- Mixing Consoles
- Multi-Track Recorders
- Broadcast Studio Equipment
- Musical Instruments
- Effects Processors
- A/V Receivers
- Car Audio Systems

3 Description

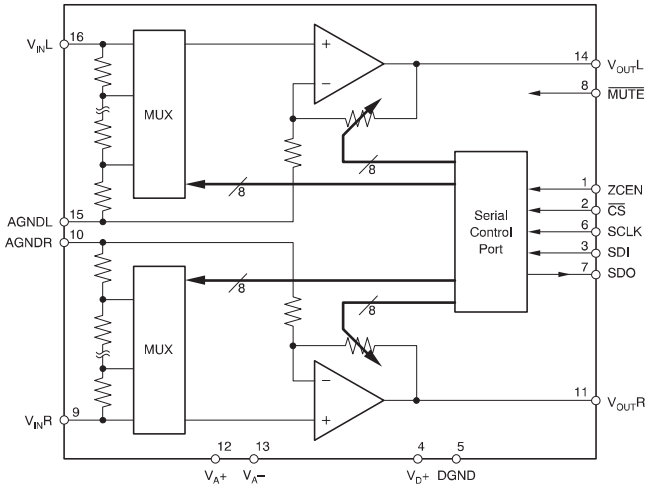
The PGA2311 device is a high-performance, stereo audio volume control designed for professional and high-end consumer audio systems. The PGA2311 uses an internal high-performance operational amplifier to yield low noise and distortion. The PGA2311 also provides the capability to drive 660-Ω loads directly without buffering. The 3-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining of multiple PGA2311 devices.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA2311	SOIC (16)	7.5 mm × 10.30 mm
	PDIP (16)	6.35 mm × 19.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Stereo Audio Volume Control



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2016) to Revision D — **Page**

- Changed the values of Voltage range, PGA2311PA, UA (A−grade) To: (V_A-) = + 1.25 V, and (V_A-) = –1.25 V in the *Electrical Characteristics* table ... 5
- Chnaged the Quiescent current Test Conditions To: V_A = +5 V, and V_A = –5 V in the *Electrical Characteristics* table ... 6

Changes from Revision B (January 2016) to Revision C — **Page**

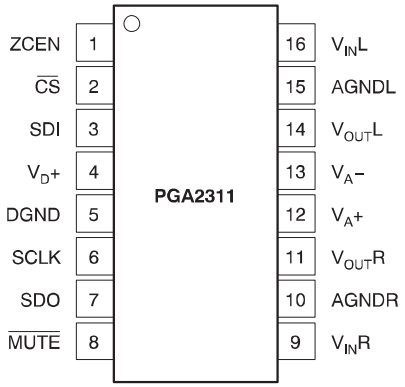
- Changed package family terms in second to last Features bullet ... 1
- Changed description of pin 7 in *Pin Functions* table ... 3
- Deleted lead temperature and package temperature rows from *Absolute Maximum Ratings* table ... 4

Changes from Revision A (June 2002) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Pin Configuration and Functions

N or DW Package
16-Pin PDIP or SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ZCEN	I	Zero-crossing enable input (active high)
2	$\overline{CS}$	I	Chip-select input (active low)
3	SDI	I	Serial data input
4	V_D+	I	Digital power supply, +5 V
5	DGND	—	Digital ground
6	SCLK	I	Serial clock input
7	SDO	O	Serial data output
8	$\overline{MUTE}$	I	Mute control input (active low)
9	V_{IN}R	I	Analog input, right channel
10	AGNDR	—	Analog ground, right channel
11	V_{OUT}R	O	Analog output, right channel
12	V_A+	I	Analog power supply, +5 V
13	V_A–	I	Analog power supply, –5 V
14	V_{OUT}L	O	Analog output, left channel
15	AGNDL	—	Analog ground, left channel
16	V_{IN}L	I	Analog input, left channel

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_A+		5.5	V
	V_A–		–5.5	
	V_D+		5.5	
	V_A+ to V_D+		< ±0.3	
Analog input voltage		0	V_A+, V_A–	V
Digital input voltage		–0.3	V_D+	V
Operating temperature		–40	85	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
PGA2311 in 16-Pin SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
PGA2311 in 16-Pin PDIP Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_A+	Positive analog power supply	4.75	5	5.25	V
V_A–	Negative analog power supply	–4.75	–5	–5.25	V
V_D+	Digital power supply	4.75	5	5.25	V
	Operating temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		PGA2311		UNIT
		N (PDIP)	DW (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.9	83	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	44	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	40.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.7	11.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	40.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

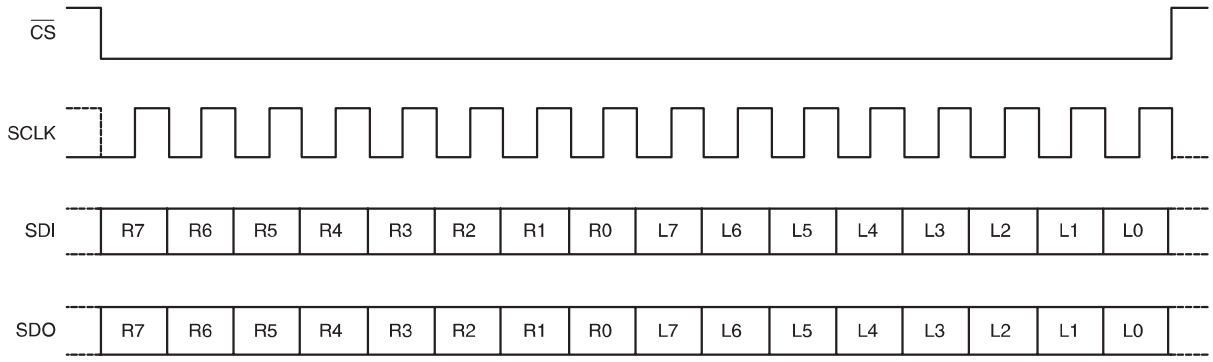
At T_A = +25°C, V_A+ = +5 V, V_A− = –5 V, V_D+ = +5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
	Step size				0.5		dB
	Gain error	Gain setting = 31.5 dB			±0.05		dB
	Gain matching				±0.05		dB
	Input resistance				10		kΩ
	Input capacitance	PGA2311P, U (U−grade)			3		pF
		PGA2311PA, UA (A−grade)				7	
AC CHARACTERISTICS							
	THD+N	V_{IN} = 2 Vrms, f = 1 kHz	PGA2311P, U (U−grade)		0.0004%	0.001%	
			PGA2311PA, UA (A−grade)		0.0002%	0.0004%	
	Dynamic range	V_{IN} = AGND, gain = 0 dB		116	120		dB
	Voltage range, output	PGA2311P, U (U−grade)		(V_A−) + 1.25		(V_A+) –1.25	V
		PGA2311PA, UA (A−grade)		(V_A−) + 1.25		(V_A−) − 1.25	
	Voltage range, input (without clipping)				2.5		Vrms
	Output noise	V_{IN} = AGND, gain = 0 dB			2.5	4	μV_{RMS}
	Interchannel crosstalk	f = 1 kHz			–130		dBFS
OUTPUT BUFFER							
	Offset voltage	V_{IN} = AGND, gain = 0 dB			0.25	0.5	mV
	Load capacitance stability				100		pF
	Short-circuit current				50		mA
	Unity-gain bandwidth, small signal				10		MHz
DIGITAL CHARACTERISTICS							
V_{IH}	High-level input voltage			2		V_D+	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level output voltage	I_O = 200 µA	PGA2311P, U (U−grade)	(V_A+) − 1			V
			PGA2311PA, UA (A−grade)	(V_D+) − 1			
V_{OL}	Low-level output voltage	I_O = –3.2 mA				0.4	V
	Input leakage current				1	10	µA
SWITCHING CHARACTERISTICS							
f_{SCLK}	Serial clock (SCLK) frequency			0		6.25	MHz
t_{PL}	SCLK pulse duration low			80			ns
t_{PH}	SCLK pulse duration high			80			ns
t_{MI}	$\overline{\text{MUTE}}$ pulse duration low			2			ms
INPUT TIMING							
t_{SDS}	SDI setup time			20			ns
t_{SDH}	SDI hold time			20			ns
t_{CSCR}	$\overline{\text{CS}}$ falling to SCLK rising			90			ns
t_{CFCS}	SCLK falling to $\overline{\text{CS}}$ rising			35			ns
OUTPUT TIMING							
t_{CSO}	$\overline{\text{CS}}$ low to SDO active					35	ns
t_{CFDO}	SCLK falling to SDO data valid					60	ns
t_{CSZ}	$\overline{\text{CS}}$ high to SDO high impedance					100	ns

Electrical Characteristics (continued)

At T_A = +25°C, V_A+ = +5 V, V_A– = –5 V, V_D+ = +5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Operating voltage	V_A+		4.75	5	5.25	V
	V_A–		–4.75	–5	–5.25	
	V_D+		4.75	5	5.25	
Quiescent current	I_A+	V_A+ = +5 V		8	10	mA
	I_A–	V_A– = –5 V		10	12	
	I_D+	V_D+ = +5 V		0.5	1	
PSRR Power-supply rejection ratio (250 Hz)				100		dB
TEMPERATURE RANGE						
Operating range			–40		85	°C



Gain Byte Format is MSB First, Straight Binary
R0 is the Least Significant Bit of the Right Channel Gain Byte
R7 is the Most Significant Bit of the Right Channel Gain Byte
L0 is the Least Significant Bit of the Left Channel Gain Byte
L7 is the Most Significant Bit of the Left Channel Gain Byte
SDI is latched on the rising edge of SCLK.
SDO transitions on the falling edge of SCLK.

Figure 1. Serial Interface Protocol

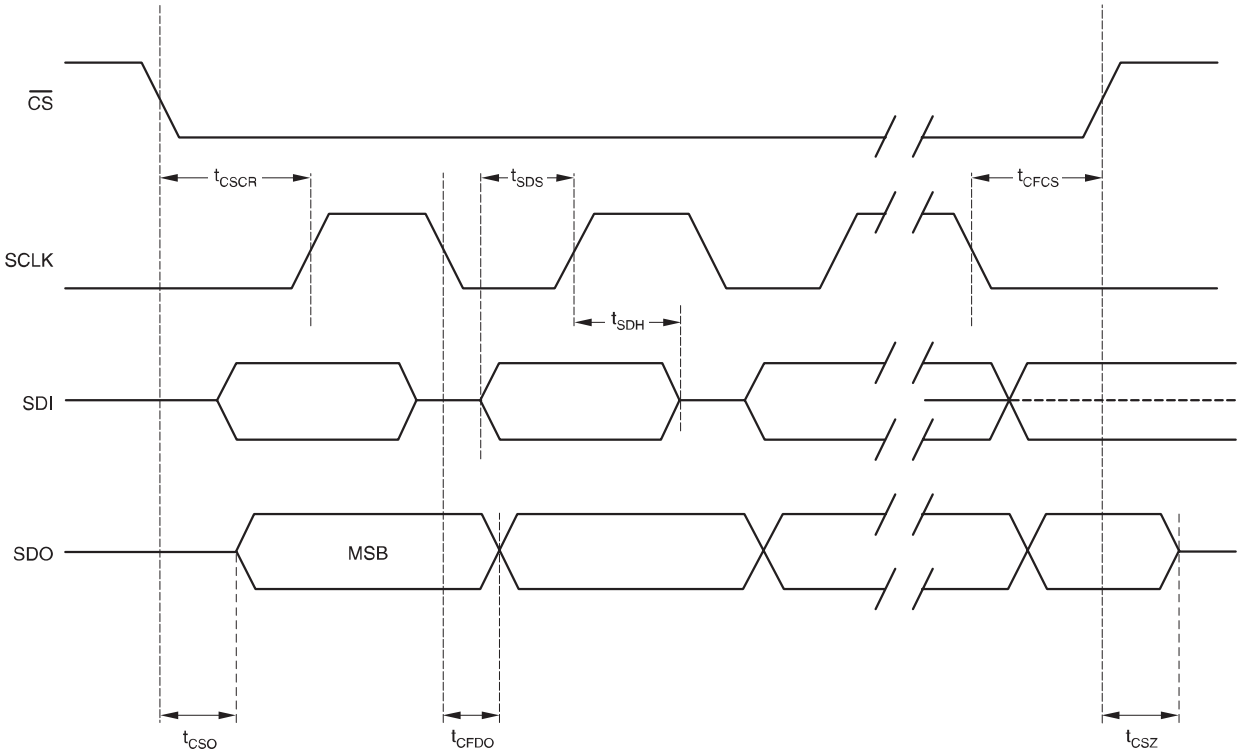
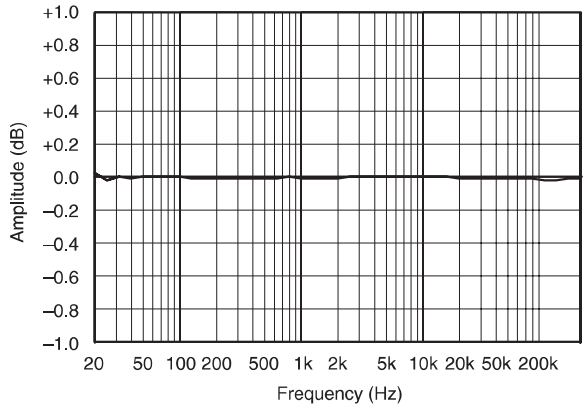


Figure 2. Serial Interface Timing Requirements

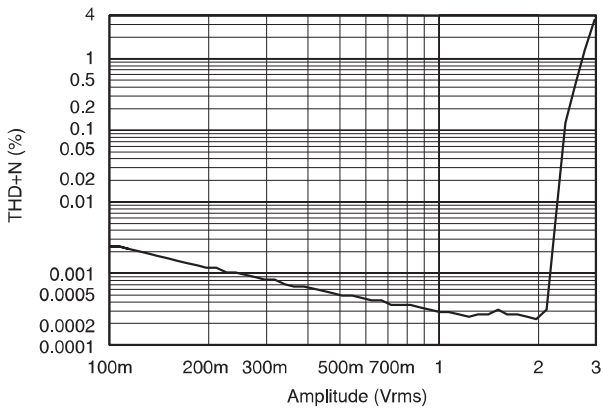
6.6 Typical Characteristics

At T_A = +25°C, V_A+ = +5 V, V_A− = −5 V, V_D+ = +5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted. All plots taken with PGA2311 A-grade.



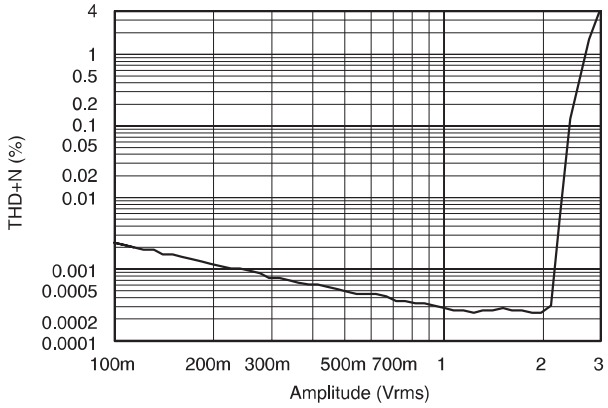
Gain = 0 dB, Load = 100 kΩ, V_{IN} = 2 Vrms

Figure 3. Amplitude vs Frequency



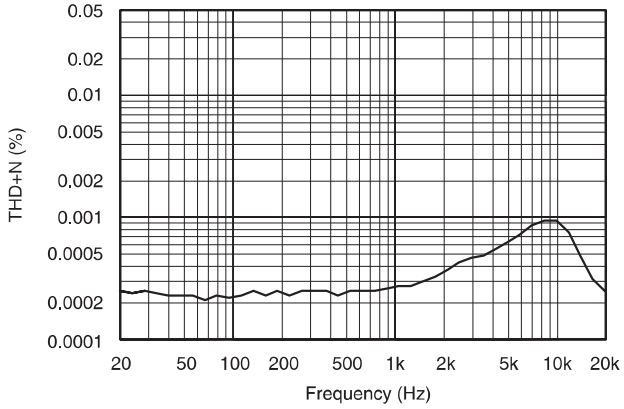
Gain = 0 dB, Freq = 1 kHz, Load = 100 kΩ

Figure 4. THD + N vs Amplitude



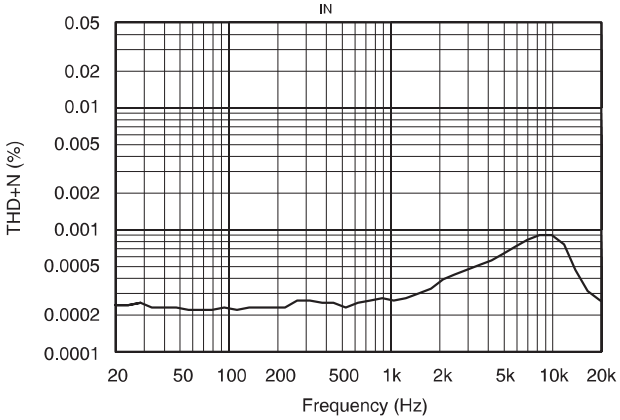
Gain = 0 dB, Freq = 1 kHz, Load = 600 Ω

Figure 5. THD + N vs Amplitude



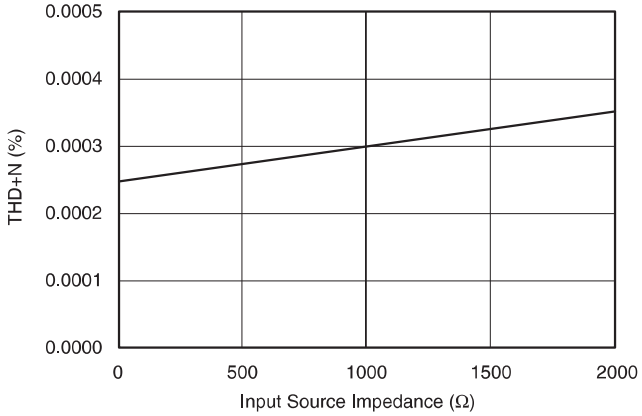
Gain = 0 dB, V_{IN} = 2 Vrms, Load = 100 kΩ

Figure 6. THD + N vs Frequency



Gain = 0 dB, V_{IN} = 2 Vrms, Load = 600 Ω

Figure 7. THD + N vs Frequency



Gain = 0 dB, V_{IN} = 2 Vrms, F_{IN} = 1 kHz

Figure 8. THD + N vs Input Source Impedance

Typical Characteristics (continued)

At T_A = +25°C, V_A+ = +5 V, V_A− = −5 V, V_D+ = +5 V, R_L = 100 kΩ, C_L = 20 pF, BW measure = 10 Hz to 20 kHz, unless otherwise noted. All plots taken with PGA2311 A-grade.

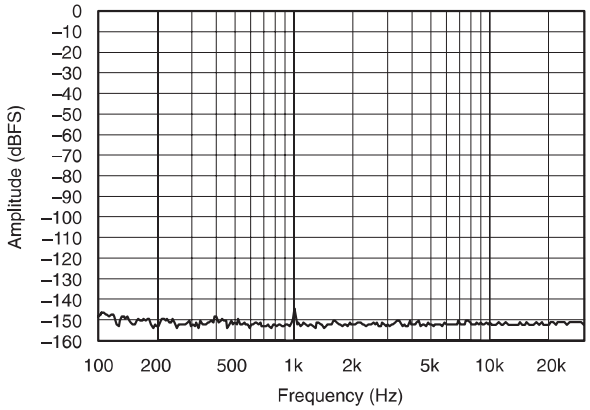


Figure 9. Crosstalk With F_{IN} = 1 kHz

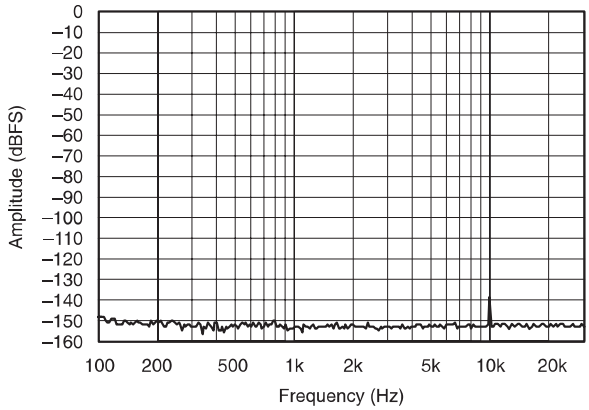


Figure 10. Crosstalk With F_{IN} = 10 kHz

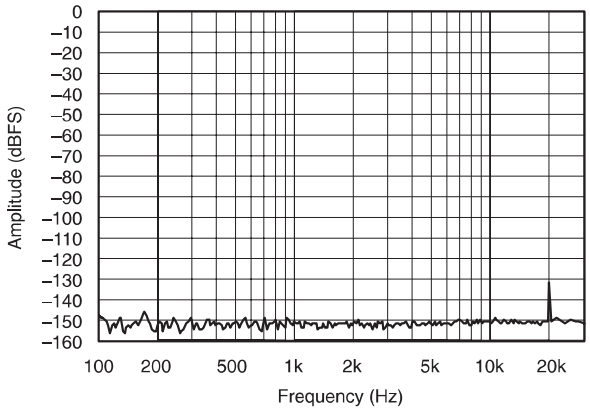


Figure 11. Crosstalk With F_{IN} = 20 kHz

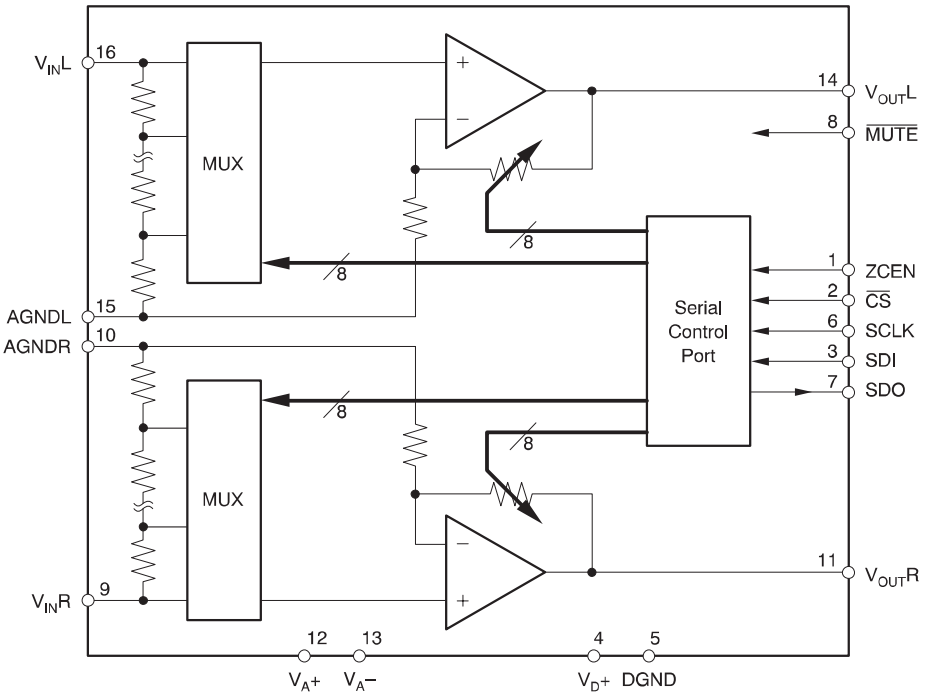
7 Detailed Description

7.1 Overview

The PGA2311 is a stereo audio volume control that can be used in a wide array of professional and consumer audio equipment. The PGA2311 is fabricated in a sub-micron CMOS process.

The heart of the PGA2311 is a resistor network, an analog switch array, and a high-performance operational amplifier stage. The switches select taps in the resistor network that determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. The *Functional Block Diagram* section shows a model diagram of the PGA2311.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs and Outputs

The PGA2311 includes two independent channels (referred to as the left and right channels). Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are $V_{IN}R$ (pin 9) and $V_{IN}L$ (pin 16), and the outputs are $V_{OUT}R$ (pin 11) and $V_{OUT}L$ (pin 14). The input and output pins can swing within 1.25 V of the analog power supplies, V_A+ (pin 12) and V_A- (pin 13). Given V_A+ = +5 V and V_A- = −5 V, the maximum input or output voltage range is 7.5 Vp-p.

For optimal performance, drive the PGA2311 with a low source impedance. A source impedance of 600 Ω or less is recommended. Source impedances up to 2 kΩ cause minimal degradation of THD+N; see Figure 8 for more details.

Feature Description (continued)

7.3.2 Gain Settings

The gain for each channel is set by its corresponding 8-bit code, either R[7:0] or L[7:0] (see Figure 1). The gain code data is straight binary format. If N equals the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

- For N = 0: Mute Condition. The input multiplexer is connected to analog ground (AGNDR or AGNDL).
- For N = 1 to 255: Gain (dB) = 31.5 − [0.5 w (255 − N)]

This results in a gain range of +31.5 dB (with N = 255) to −95.5 dB (with N = 1).

Changes in gain setting can be made with or without zero-crossing detection. The operation of the zero-crossing detector and timeout circuitry is discussed in the *Zero-Crossing Detection* section.

7.3.3 Daisy-Chaining Multiple PGA2311 Devices

To reduce the number of control signals required to support multiple PGA2311 devices on a printed circuit board (PCB), the serial control port supports daisy-chaining of multiple PGA2311 devices. Figure 12 shows the connection requirements for daisy-chain operation. This arrangement allows a 3-wire serial interface to control many PGA2311 devices.

As shown in Figure 12, the SDO pin from PGA2311 #1 is connected to the SDI input of PGA2311 #2, and is repeated for additional devices. This configuration in turn forms a large shift register, in which gain data can be written for all PGA2311s connected to the serial bus. The length of the shift register is 16 × N bits, where N is equal to the number of PGA2311 devices included in the chain. The $\overline{CS}$ input must remain LOW for 16 × N SCLK periods, where N is the number of devices connected in the chain, to allow enough SCLK cycles to load all devices.

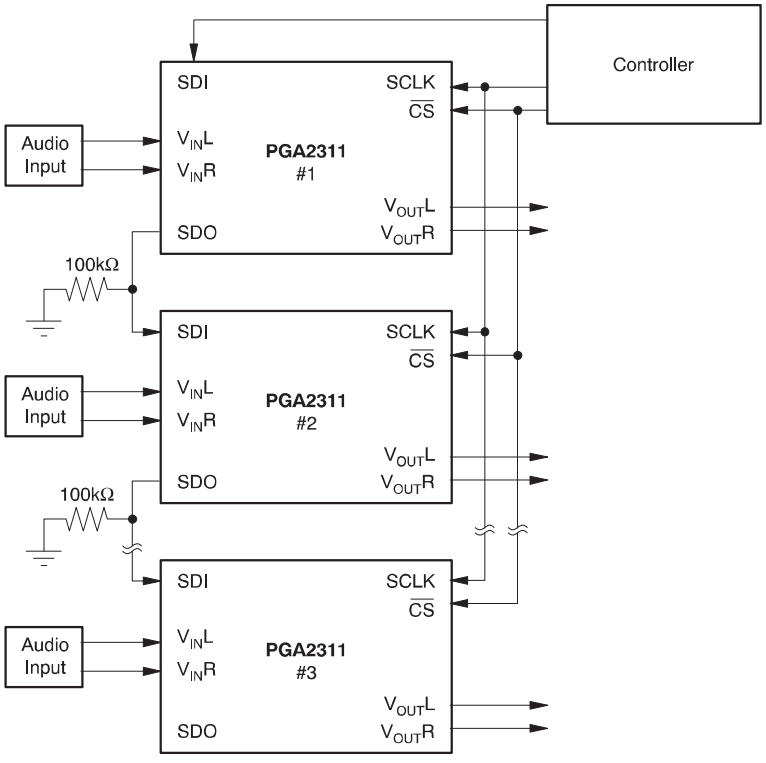


Figure 12. Daisy-Chaining Multiple PGA2311 Devices

Feature Description (continued)

7.3.4 Zero-Crossing Detection

The PGA2311 includes a zero-crossing detection function for noise-free level transitions. The concept is to change gain settings on a zero-crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is LOW, zero-crossing detection is disabled. When ZCEN is HIGH, zero-crossing detection is enabled.

The zero-crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting is not implemented until either a positive slope zero crossing is detected, or a time-out period of 16 ms has elapsed. In the case of a time-out, the new gain setting takes effect with no attempt to minimize audible artifacts.

7.3.5 $\overline{\text{MUTE}}$ Function

Muting can be achieved by either hardware or software control. Hardware muting is accomplished through the $\overline{\text{MUTE}}$ input, and software muting by loading all zeroes into the volume control register.

$\overline{\text{MUTE}}$ disconnects the internal buffer amplifiers from the output pins and terminates $A_{OUT}L$ and $A_{OUT}R$ with 10-kΩ resistors to ground. The mute is activated with a zero-crossing detection (independent of the zero-cross enable status), or an 16-ms time-out to eliminate any audible clicks or pops. $\overline{\text{MUTE}}$ also initiates an internal offset calibration.

A software mute is implemented by loading all zeroes into the volume control register. The internal amplifier is set to unity gain, with the amplifier input connected to AGND.

7.4 Device Functional Modes

7.4.1 Power-Up State

On power-up, power-up reset is activated for approximately 100 ms, during which the circuit is in hardware $\overline{\text{MUTE}}$ state and all internal flip-flops are reset. At the end of this period, the offset calibration is initiated without any external signals. When this step is complete, the gain byte value for both the left and right channels are set to 00_{HEX}, or the software $\overline{\text{MUTE}}$ condition. The gain remains at this setting until the host controller programs new settings for each channel via the serial control port.

If the power-supply voltage drops below ±3.2 V during normal operation, the circuit enters a hardware MUTE state. A power-up sequence initiates if the power-supply voltage returns to greater than ±3.2 V.

7.5 Programming

The serial control port is used to program the gain settings for the PGA2311. The serial control port includes three input pins and one output pin. The inputs include $\overline{\text{CS}}$ (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

The $\overline{\text{CS}}$ pin functions as the chip-select input. Data can be written to the PGA2311 only when $\overline{\text{CS}}$ is LOW. SDI is the serial data input pin. Control data are provided as a 16-bit word at the SDI pin, 8 bits each for the left and right channel gain settings.

Data are formatted as MSB first, in straight binary code. SCLK is the serial clock input. Data are clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and used when daisy-chaining multiple PGA2311 devices. Daisy-chain operation is described in the *Daisy-Chaining Multiple PGA2311 Devices* section. SDO is a tri-state output, and assumes a high-impedance state when $\overline{\text{CS}}$ is HIGH.

The protocol for the serial control port is illustrated in Figure 1; see Figure 2 for detailed timing specifications for the serial control port.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA2311 is commonly used as a digitally-controlled analog volume control. Analog volume is controlled through a serial interface in 0.5-dB steps, ranging from a gain of +31.5 dB down to an attenuation of −95.5 dB.

8.2 Typical Application

Figure 13 shows the recommended connections for the PGA2311. Place power-supply bypass capacitors as close to the PGA2311 package as physically possible.

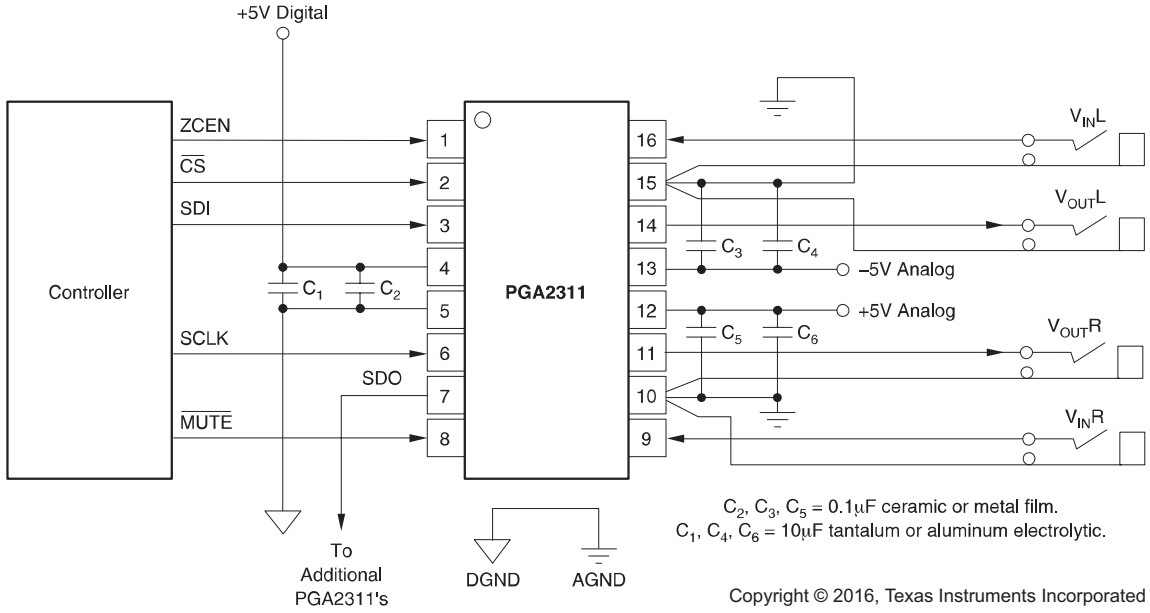


Figure 13. Recommended Connection Diagram

8.2.1 Design Requirements

- Wide dynamic range, +35.5 dB to –95.5 dB
- Operate from a 5-V digital supply and ±5-V analog supplies
- Digitally-controlled analog volume

8.2.2 Detailed Design Procedure

The PGA2311 is a complete digitally-controlled analog stereo volume controller system on a chip requiring only a controller to select the gain or attenuation through a serial interface. Figure 13 shows the basic connections to the PGA2311. Place power-supply bypass capacitors as close to the PGA2311 package as physically possible.

Typical Application (continued)

8.2.3 Application Curve

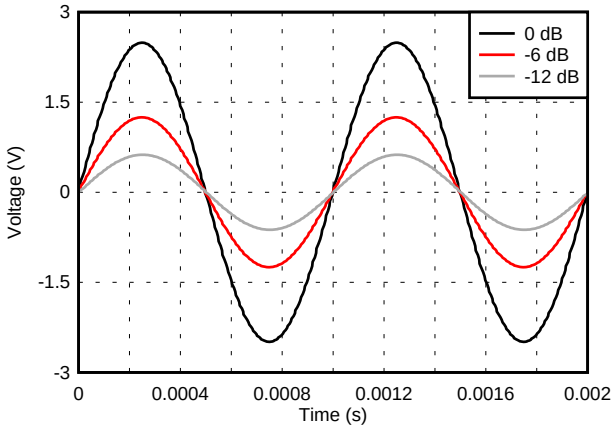


Figure 14. PGA2311 Operating at 0 dB, –6 dB and –12 dB

9 Power Supply Recommendations

The PGA2311 is specified for operation with its analog power supplies ranging from ±4.75 V to ±5.25 V and its digital power supply ranging from 4.75 V to 5.25 V. Place power-supply bypass capacitors as close to the PGA2311 package as physically possible.

10 Layout

10.1 Layout Guidelines

The ground planes for the digital and analog sections of the PCB must be separate from one another. The planes must be connected at a single point. Figure 15 shows the recommended PCB floor plan for the PGA2311.

The PGA2311 is mounted so that the device straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board and pins 9 through 16 are on the analog side of the board.

10.2 Layout Example

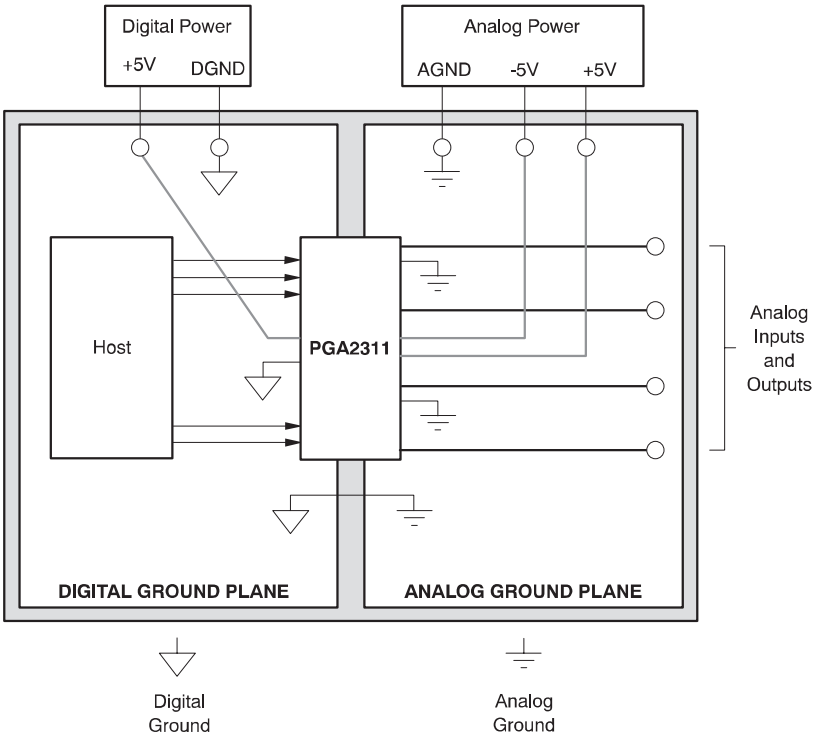


Figure 15. Typical PCB Layout Floor Plan

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Circuit Board Layout Techniques,* SLOA089
- *Shelf-Life Evaluation of Lead-Free Component Finishes,* SZZA046

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

E2E Audio Amplifier Forum ***TI's Engineer-to-Engineer (E2E) Community for Audio Amplifiers.*** Created to foster collaboration among engineers. Ask questions and receive answers in real-time.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA2311P	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA2311P	Samples
PGA2311PA	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA2311P A	Samples
PGA2311U	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2311U	Samples
PGA2311U/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2311U	Samples
PGA2311U/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2311U	Samples
PGA2311UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		PGA2311U A	Samples
PGA2311UA/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		PGA2311U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

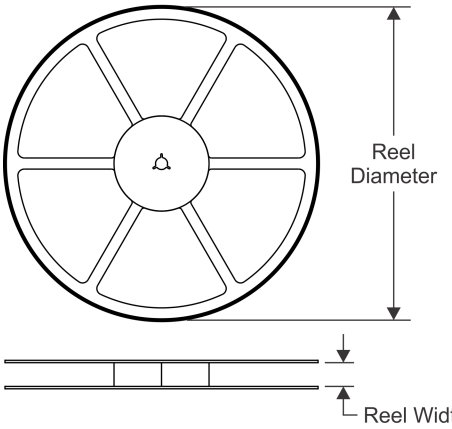
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

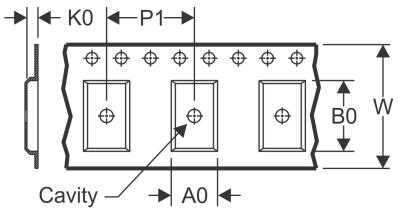
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

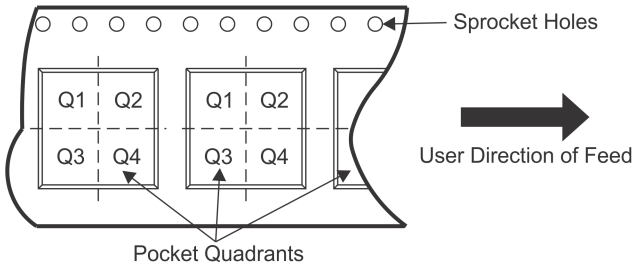


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

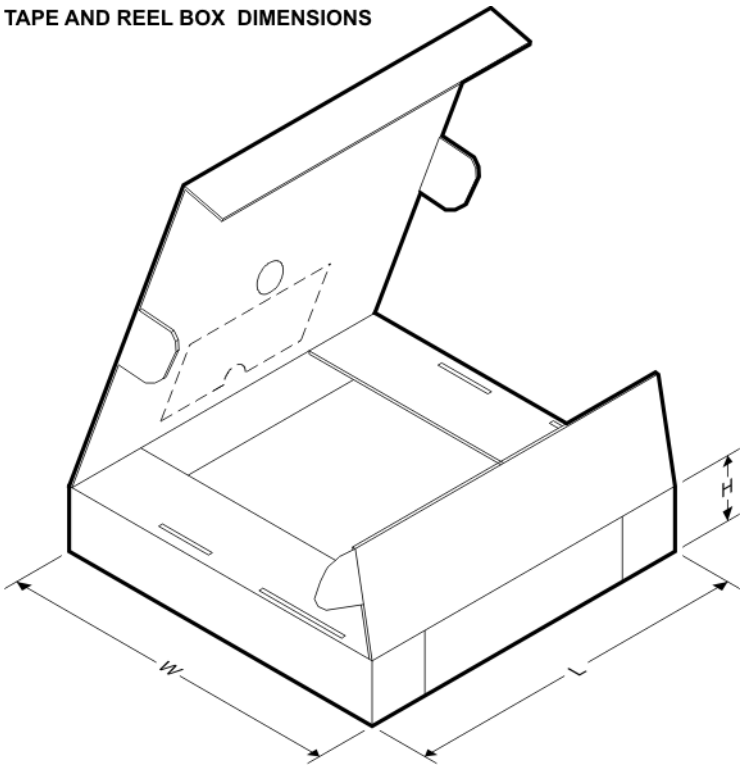
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA2311U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PGA2311UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



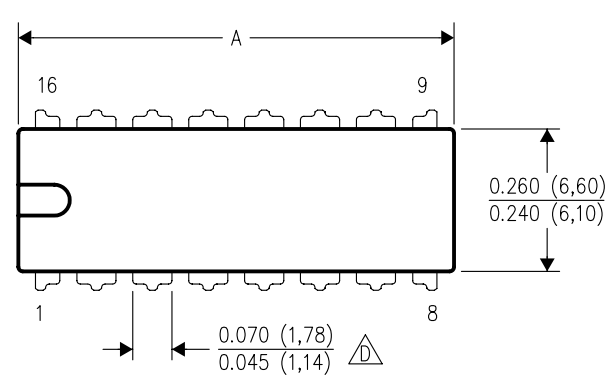
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA2311U/1K	SOIC	DW	16	1000	367.0	367.0	38.0
PGA2311UA/1K	SOIC	DW	16	1000	367.0	367.0	38.0

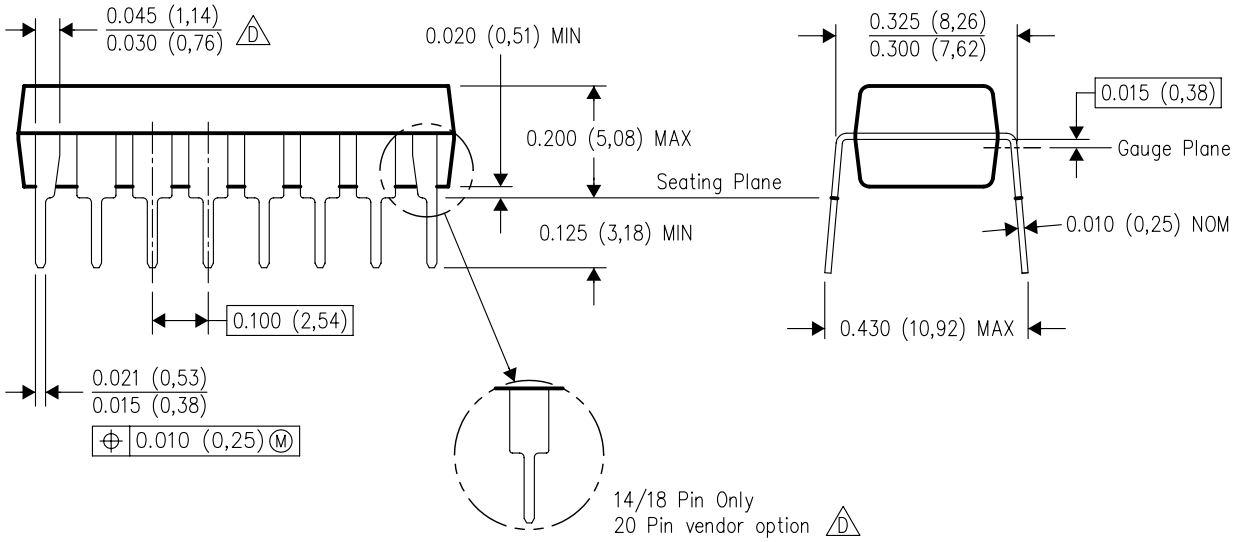
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

GENERIC PACKAGE VIEW

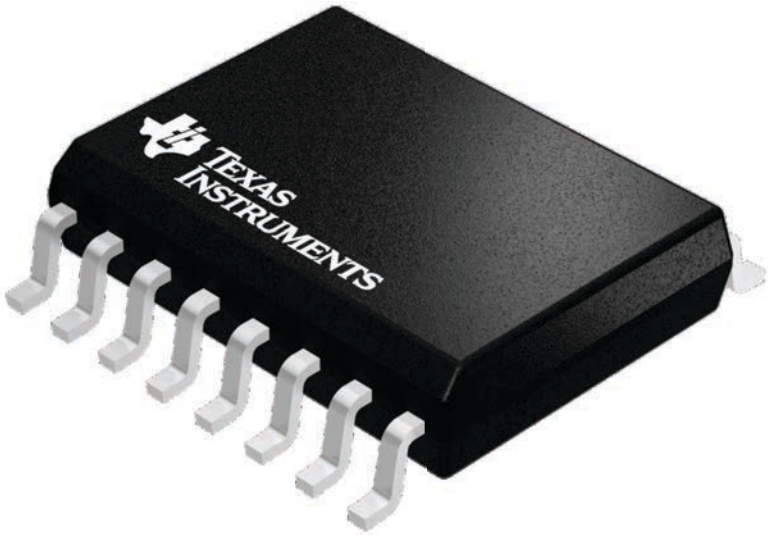
DW 16

SOIC - 2.65 mm max height

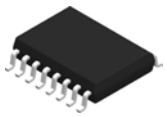
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

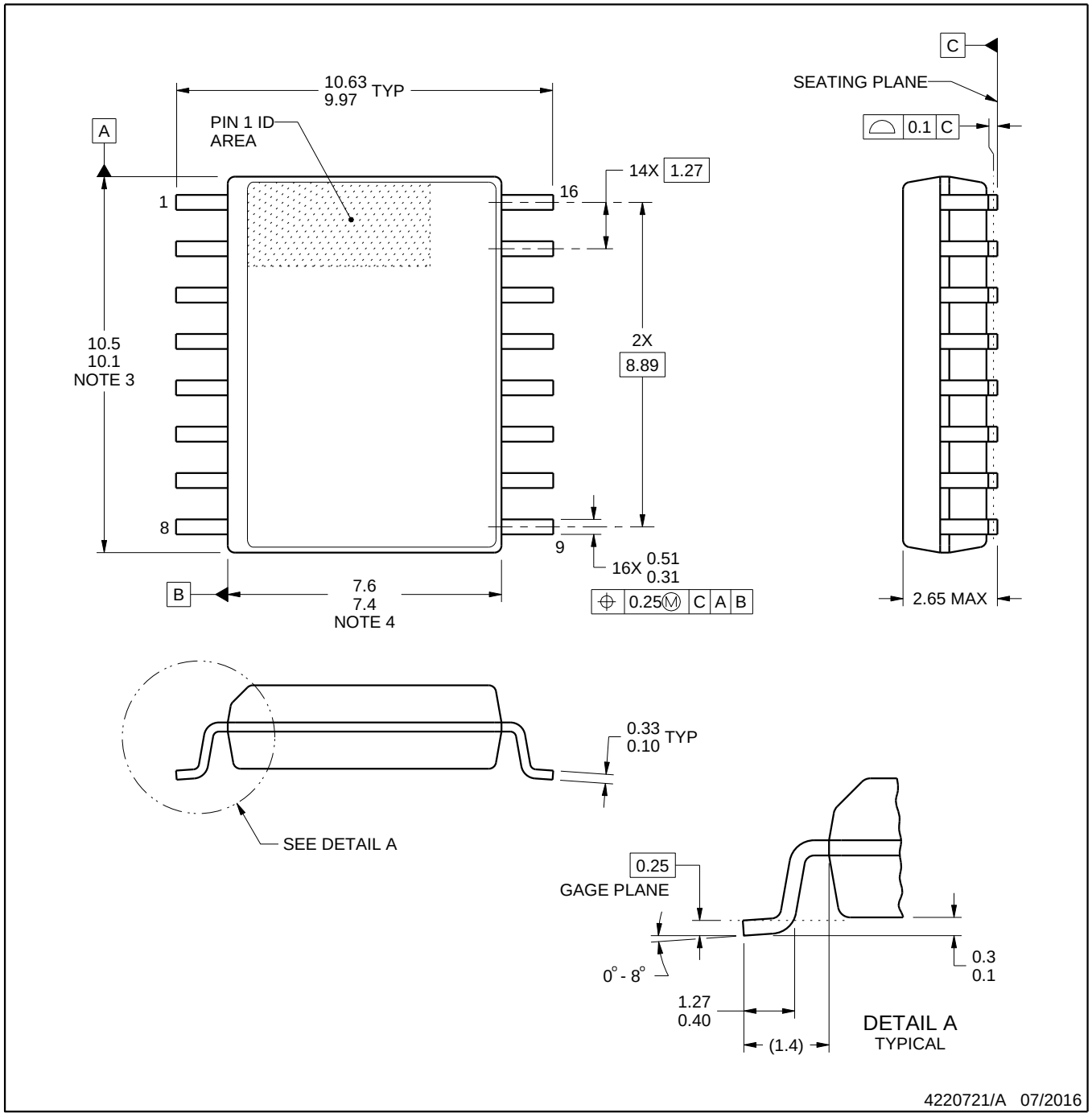


PACKAGE OUTLINE

DW0016A

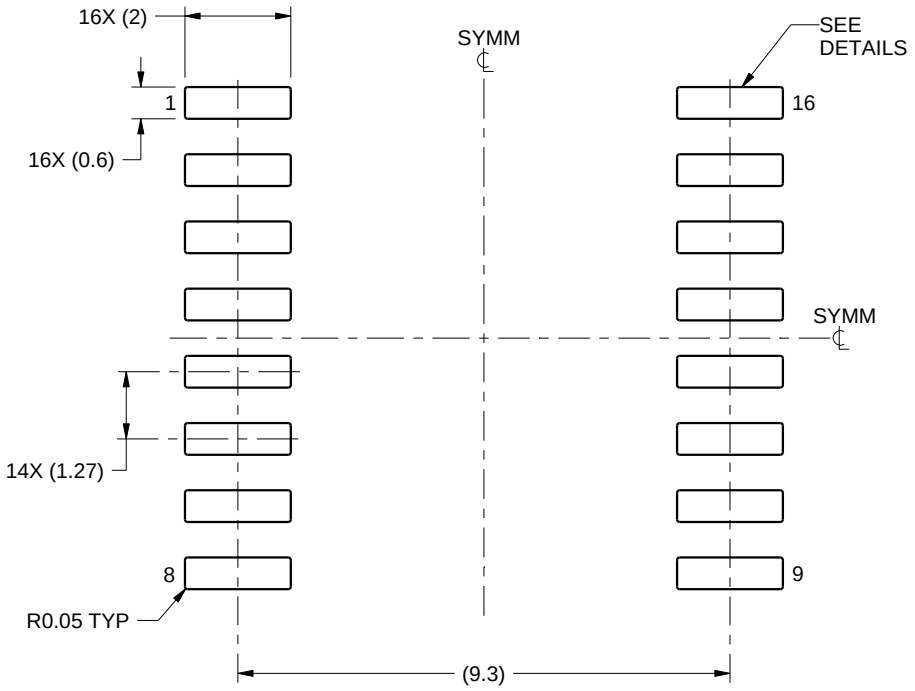
SOIC - 2.65 mm max height

SOIC

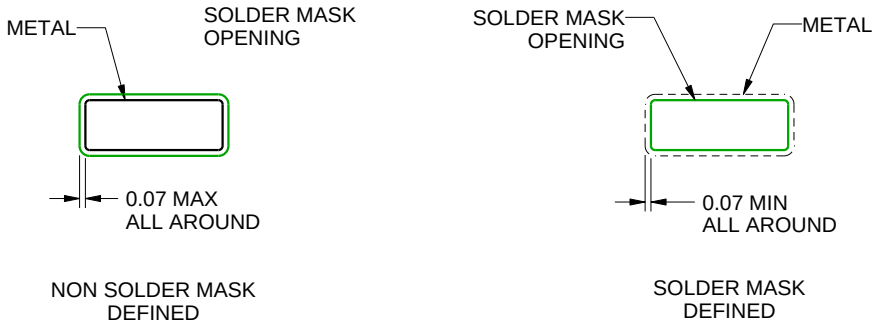


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

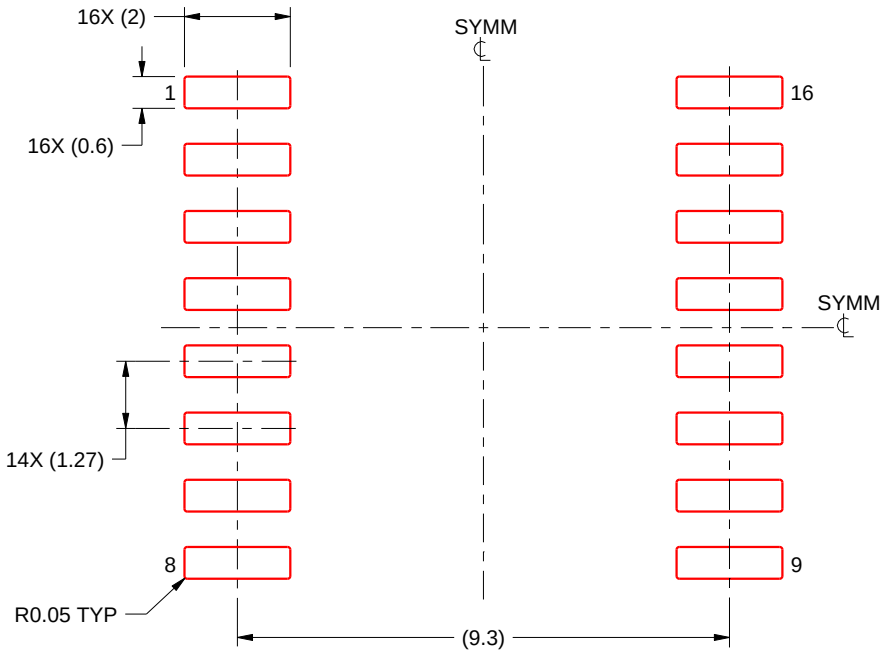


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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