POWERTIP TECH. CORP.

SPECIFICATIONS

CUSTOMER	:	PTC
SAMPLE CODE	:	SH320240T-022-I09Q
MASS PRODUCTION CODE	:	PH320240T-022-I09Q
SAMPLE VERSION	:	01
SPECIFICATIONS EDITION	:	004
DRAWING NO. (Ver.)	:	JLMD-PH320240T-022-I09Q_002
PACKAGING NO. (Ver.)	:	JPKG-PH320240T-022-I09Q_001

Customer Approved

Date:

POWERTIP
2016.01.29
JS RD APPROVED

Approved	Checked	Designer
閆偉	張久慧	劉進

□ Preliminary specification for design input

■ Specification for sample approval

POWERTIP TECH. CORP.

Headquarters:

No.8, 6th Road, Taichung Industrial Park,
Taichung, Taiwan
台中市 407 工業區六路 8 號

TEL: 886-4-2355-8168
FAX: 886-4-2355-8166

E-mail: sales@powertip.com.tw
Http://www.powertip.com.tw

History of Version

Date	Ver.	Edi.	Description	Page	Design by
03/28/2013	01	001	New sample	-	趙冬冬
04/08/2014	01	002	Updating LCM Drawing	-	譚超敏
08/18/2015	01	003	Show Backlight Life Time	9	劉進
01/28/2016	01	004	Update Timing Characteristics	18-23	劉進

Total: 33 Page

Contents

Note : For detailed information please refer to IC data sheet :

Primacy(TFT LCD): SSD2119

1. SPECIFICATIONS

1.1 Features

Main LCD Panel

Item	Standard Value
Display Type	320* (R、G、B) * 240 Dots
LCD Type	a-Si TFT , Normally White , TN mode , Transmissive type
Screen size (inch)	3.5 inch
Viewing Direction	6 O'clock
Color configuration	R.G.B. vertical stripe
Backlight	LED B/L
Driver IC	SSD2119 (262K Colors)
Interface	1. 8/ 9/ 16/ 18-bit 6800-series /8080-series Parallel Interface. 2. Serial Peripheral Interface (SPI). 3. 18-/6-bit RGB interface (DEN,DOTCLK, HSYNC, VSYNC, DB[17:0]). 4. VSYNC interface (system interface + VSYNC). 5. WSYNC interface (system interface + WSYNC).
ROHS	THIS PRODUCT CONFORMS THE ROHS OF PTC Detail information please refer web side： http://www.powertip.com.tw/news.php?area_id_view=1085560481/

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	76.9 (W) * 63.9(L) * 4.75(H)(MAX)	mm

LCD Panel

Item	Standard Value	Unit
Active Area	70.8 (W) * 53.2 (L)	mm

Touch Panel

Item	Standard Value	Unit
Outline Dimension (T/P)	76.4(W) * 61.0 (L)	mm
Active Area (T/P)	70.8 (W) * 53.2 (L)	mm

Note：For detailed information please refer to LCM drawing.

1.3 Absolute Maximum Ratings

Module

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDDIO	VSS	-0.3	+4.0	V
Input Voltage	VCI	-	-0.3	+5.0	V
Operating Temperature	T_{OP}	Excluded T/P	-20	+70	°C
Storage Temperature	T_{ST}	Excluded T/P	-30	+80	°C
Storage Humidity	H_D	Ta < 60 °C	20	90	%RH

1.4 DC Electrical Characteristics

Module VSS = 0V, Ta = 25°C

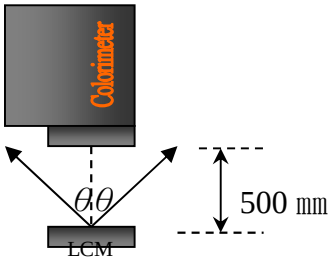
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDDIO	-	3.0	3.3	3.6	V
Input High Voltage	V_{IH1}	-	0.8*VDDIO	-	VDDIO	V
Input Low Voltage	V_{IL1}	-	0	-	0.2*VDDIO	V
Output High Voltage	V_{OH1}	I_{OH}=-0.1mA	0.9*VDDIO	-	VDDIO	V
Output Low Voltage	V_{OL1}	I_{OL}=0.1mA	0	-	0.1*VDDIO	V
Supply Current	I_{DDIO}	VDDIO = 3.3V	-	7.5	11.5	mA

1.5 Optical Characteristics

TFT LCD Panel VDDIO =3.3V, Ta=25°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	-
Response time		Tr + Tf	-	-	30	45	ms	Note2
Viewing angle	Top	θY+	CR ≥ 10	-	60	-	Deg.	Note4
	Bottom	θY-		-	60	-		
	Left	θX-		-	60	-		
	Right	θX+		-	60	-		
Contrast ratio		CR	-	500	600	-	-	Note3
Color of CIE Coordinate	White	X	-	0.26	0.31	0.36	-	Note1
		Y		0.28	0.33	0.38		
	Red	X		0.58	0.63	0.68		
		Y		0.29	0.34	0.39		
	Green	X		0.29	0.34	0.39		
		Y		0.55	0.60	0.70		
	Blue	X		0.10	0.15	0.20		
		Y		0.04	0.09	0.14		
Average Brightness Pattern=white display		IV	IF= 20 mA	162	187	-	cd/m^2	Note1
Uniformity		△B		70	-	-	%	Note1

Note1:
1：△B=B(min) / B(max) ×100%
2：Measurement Condition for Optical Characteristics:
a：Environment: 25℃±5℃ / 60±20%R.H，no wind，dark room below 10 Lux at typical lamp current and typical operating frequency.
b：Measurement Distance: 500 ± 50 ㎜ ，(θ= 0°)
c：Equipment: TOPCON BM-7 fast，(field 1°)，after 10 minutes operation.
d：The uncertainty of the C.I.E coordinate measurement ±0.01，Average Brightness ± 4%

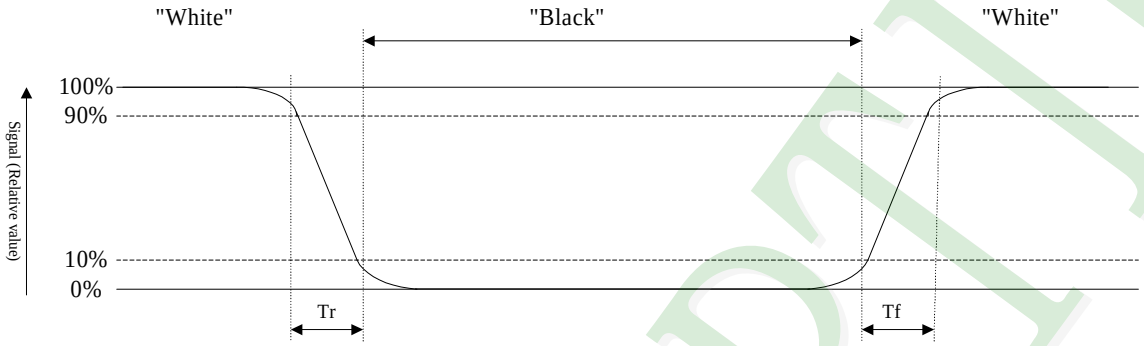


Colorimeter=BM-7 fast

Note2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:



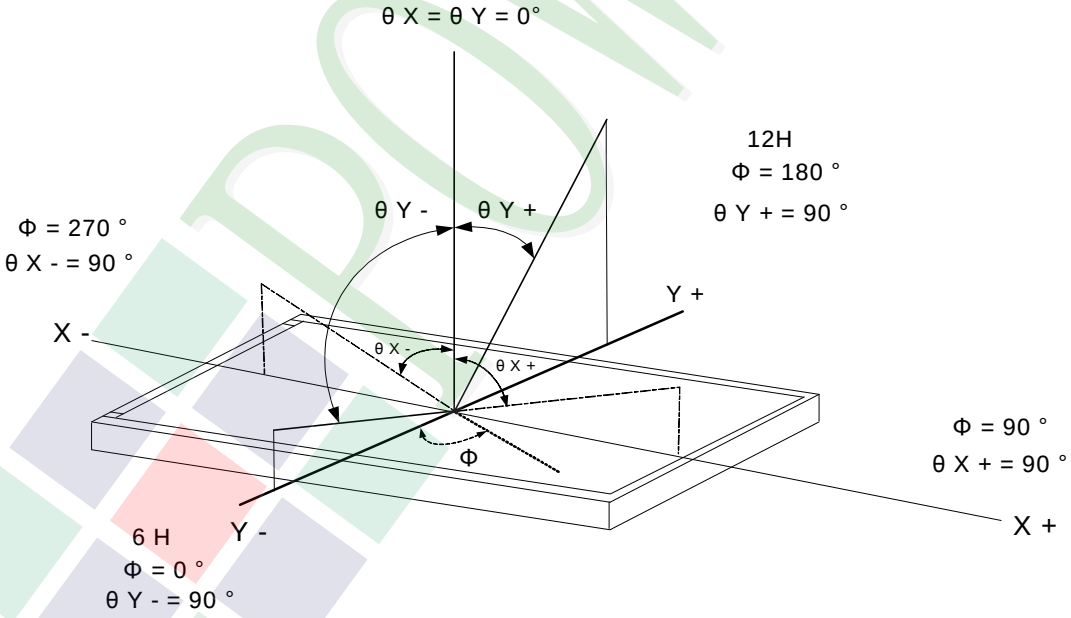
Note3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note4: Definition of viewing angle:

Refer to figure as below:



1.6 Backlight Characteristics

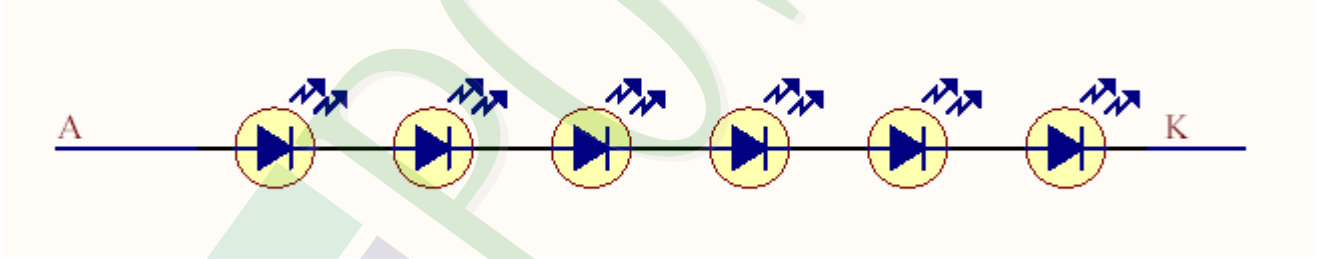
Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
LED Forward Current	IF	Ta =25℃	-	40	mA
LED Reverse Voltage	VR	Ta =25℃	-	21	V

Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	VF	If=20mA	17.4	19.2	21	V
Average Brightness (Without LCD &T/P)	IV		4500	5200	-	cd/m^2
CIE Color Coordinate (Without LCD &T/P)	X		0.28	0.30	0.32	-
	Y		0.28	0.30	0.32	
Color	White					

Internal Circuit Diagram



Other Description

Item	Conditions	Description
Life Time	Ta =25℃ IF= 20mA	20000 hrs

1.7 Touch Panel Characteristics

Touch Panel General Standard Specification

Item	Specification
Input Method	Finger or stylus pen
Operating Temperature Range	-20℃~70℃.
Storage Temperature Range	-30℃~80℃.
Operation Humidity	90%RH or less.
Storage temperature	90%RH or less
Surface Hardness	≧3H.
Pen Sliding Durability	≧1,000,000 times.
Light Transparency	80% min.
Linearity	Less than 1.5%
Resistance Between Terminals.	Direction X (Film side): 200Ω~900Ω. Direction Y (Glass side): 200Ω~900Ω.
Operating Voltage	10V DC max
Operating force	20g~80g

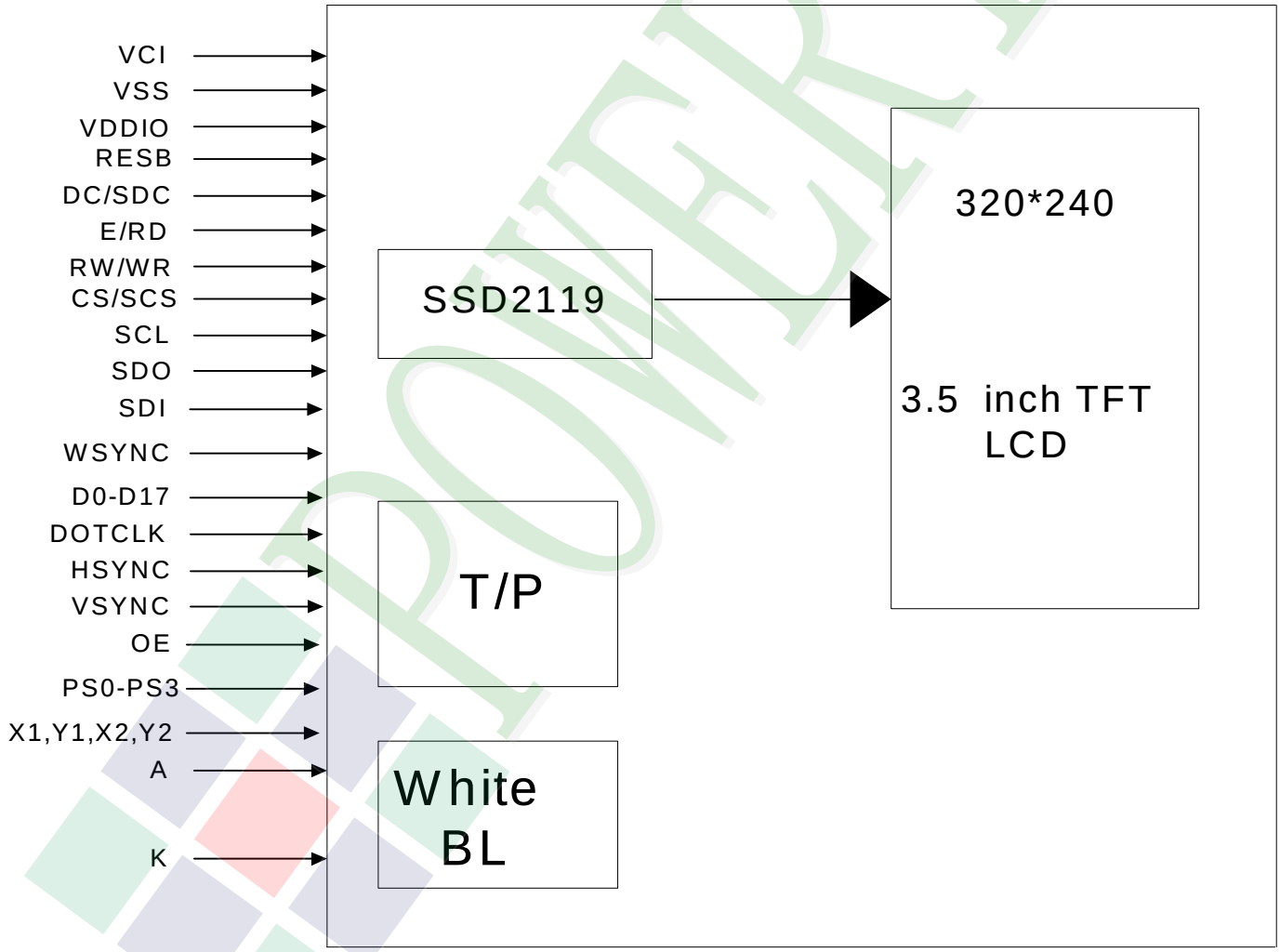
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram



2.2 Interface Pin Description

Pin No	Symbol	Function
1	VCI	Booster input voltage pin.
2	VCI	Booster input voltage pin.
3	VSS	System ground pin of the IC.
4.	VDDIO	Voltage input pin for logic I/O.
5	VSS	System ground pin of the IC.
6	RESB	System reset pin. - An active low pulse at this pin will reset the IC, Connect to VDDIO in normal operation.
7	DC/SDC	Data or command. DC: Parallel Interface. SDC: Serial Interface.
8	E/RD	6800-system:E(enable signal). 8080-system:RD(read strobe signal). Serial mode: Not used and should be connected to VDDIO or VSS.
9	RW/WR	6800-system: RW(indicates read cycle when High, write cycle when Low). 8080-system: WR(write strobe signal).
10	CS/SCS	CS: Chip Select pin for 6800/8080 Parallel Interface. SCS: Chip select pin for Serial Mode Interface.
11	SCL	Serial clock input.
12	SDO	Data output pin in serial interface.
13	SDI	Data input pin in serial interface.
14	WSYNC	Ram Write Synchronization output. -Leave it OPEN when not used.
15	D17	For parallel mode,8/9/16/18 bit interface. Unused pins should connect to VSS.
16	D16	
17	D15	
18	D14	
19	D13	

Pin No	Symbol	Function
20	D12	For parallel mode,8/9/16/18 bit interface. Unused pins should connect to VSS. Please refer to Table 1.
21	D11	
22	D10	
23	D9	
24	D8	
25	D7	
26	D6	
27	D5	
28	D4	
29	D3	
30	D2	
31	D1	
32	D0	
33	VSS	System ground pin of the IC.
34	DOTCLK	Dot-clock signal and oscillator source.
35	HSYNC	Line Synchronization input.
36	VSYNC	Frame/Ram Write Synchronization input.
37	OE	Display enable pin from controller.
38	VSS	System ground pin of the IC.
39	PS0	Please refer to Table 1.
40	PS1	
41	PS2	
42	PS3	
43	VSS	System ground pin for the IC.
44	X1	Touch screen.
45	Y1	Touch screen.

Pin No	Symbol	Function
46	X2	Touch screen.
47	Y2	Touch screen.
48	VSS	System ground pin for the IC.
49	K	Backlight LED's cathode.
50	A	Backlight LED's anode.

Table 1

PS3	PS2	PS1	PS0	Interface Mode	Data bus input
0	0	0	0	16-bit 6800 parallel interface.	D[17:10],D[8:1]
0	0	0	1	8-bit 6800 parallel interface.	D[17:10]
0	0	1	0	16-bit 8080 parallel interface.	D[17:10],D[8:1]
0	0	1	1	8-bit 8080 parallel interface.	D[17:10]
0	1	0	0	9-bit generic D[17:9] (262k color) + 3-wire SPI If 65K color, D12 shorts to D17 internally.	-
0	1	0	1	16-bit generic (262k color)+ 3-wire SPI.	-
0	1	1	0	18-bit generic (262k color)+ 3-wire SPI.	-
0	1	1	1	6-bit generic D[17:12] (262k color) + 3-wire SPI.	-
1	0	0	0	18-bits 6800 parallel interface.	D[17:0]
1	0	0	1	9-bits 6800 parallel interface.	D[17:9]
1	0	1	0	18-bit 8080 parallel interface.	D[17:0]
1	0	1	1	9-bit 8080 parallel interface.	D[17:9]
1	1	1	0	3-wire SPI.	-
1	1	1	1	4-wire SPI.	-

2.2.1 Refer Initial code

```
void Initial_Main(void) // For    SSD2119
{
        WriteCOM_Main(0x00,0x28); //VCOM    OTP
        WriteDAT_Main(0x00,0x06);
        WriteCOM_Main(0x00,0x00); //OSCEN=1
        WriteDAT_Main(0x00,0x01);
        WriteCOM_Main(0x00,0x01);    //Driver Output Control
        WriteDAT_Main(0x32,0xef); //0X32,0XEF
        WriteCOM_Main(0x00,0x02);
        WriteDAT_Main(0x04,0x00); //00    00
        WriteCOM_Main(0x00,0x03);
        WriteDAT_Main(0x60,0x64); //60
        WriteCOM_Main(0x00,0x10);     //Sleep=0
        WriteDAT_Main(0x00,0x00);
        WriteCOM_Main(0x00,0x11);
        WriteDAT_Main(0x64,0x30);//0X68,0X70       //64,30 07/15
                                          //64       30
        WriteCOM_Main(0x00,0x07);
        WriteDAT_Main(0x00,0x33);
        WriteCOM_Main(0x00,0x25);       //Frame frequency=70HZ
        WriteDAT_Main(0xd0,0x00);
        WriteCOM_Main(0x00,0x0B);       //Frequency
        WriteDAT_Main(0x53,0x08);
 //---------- Adjust the Gamma Curve ----------
        WriteCOM_Main(0x00,0x30);
        WriteDAT_Main(0x00,0x00);
        WriteCOM_Main(0x00,0x31);
        WriteDAT_Main(0x01,0x01);
```

```
        WriteCOM_Main(0x00,0x32);
        WriteDAT_Main(0x01,0x00);
        WriteCOM_Main(0x00,0x33);
        WriteDAT_Main(0x07,0x07);
        WriteCOM_Main(0x00,0x34);
        WriteDAT_Main(0x07,0x07);
        WriteCOM_Main(0x00,0x35);
        WriteDAT_Main(0x03,0x05);
        WriteCOM_Main(0x00,0x36);
        WriteDAT_Main(0x07,0x07);
        WriteCOM_Main(0x00,0x37);
        WriteDAT_Main(0x02,0x01);
        WriteCOM_Main(0x00,0x3a);
        WriteDAT_Main(0x12,0x00);
        WriteCOM_Main(0x00,0x3b);
        WriteDAT_Main(0x09,0x00);
//-------------------------power on sequence----------------------------
        WriteCOM_Main(0x00,0x0c);
        WriteDAT_Main(0x00,0x04);     //0X03
        Delay(5000);
        WriteCOM_Main(0x00,0x0d);
        WriteDAT_Main(0x00,0x09);     //0X09
        Delay(5000);
        WriteCOM_Main(0x00,0x1e);
        WriteDAT_Main(0x00,0x68);
        Delay(5000);
        WriteCOM_Main(0x00,0x0e);
        WriteDAT_Main(0x27,0x00);     //27
        Delay(5000);
```

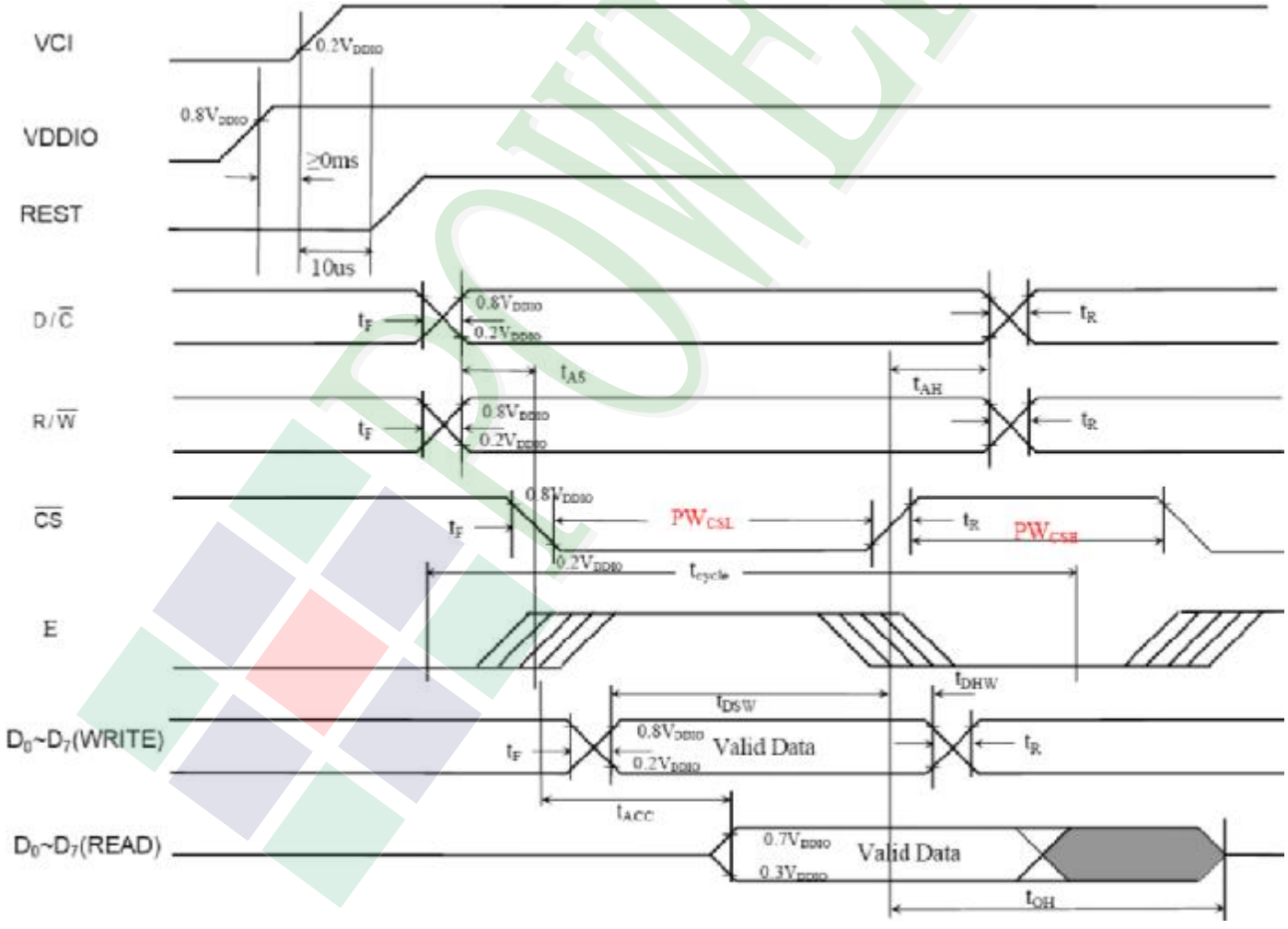
```
  WriteCOM_Main(0x00,0x26);
  WriteDAT_Main(0x7c,0x00);
  WriteCOM_Main(0x00,0x27);
  WriteDAT_Main(0x00,0x6d);
}
```

2.3 Timing Characteristics

2.3.1 6800 Interface Timing

Ta= -20 to 70 °C，VDDIO = 3.0 to 3.6V

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address Setup Time (R/$\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time (R/$\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	200	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	225	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	225	-	-	ns
t_R	Rise time	-	-	15	ns
t_F	Fall time	-	-	15	ns

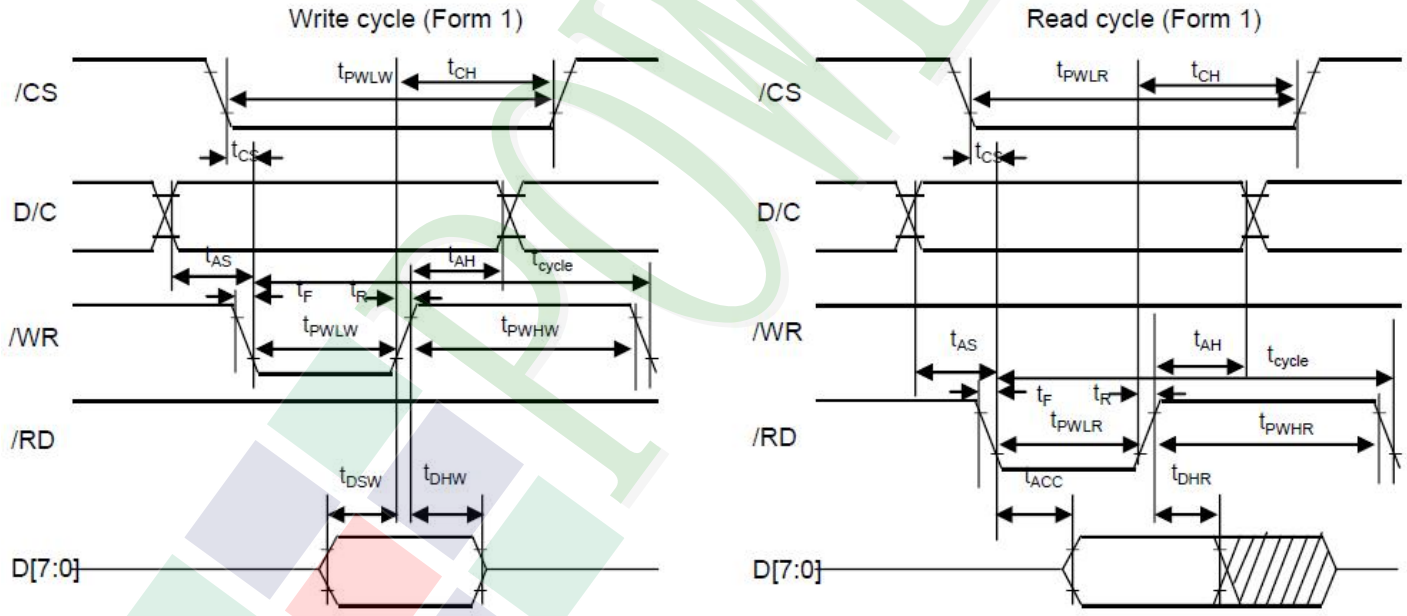


2.3.2 8080 Interface Timing

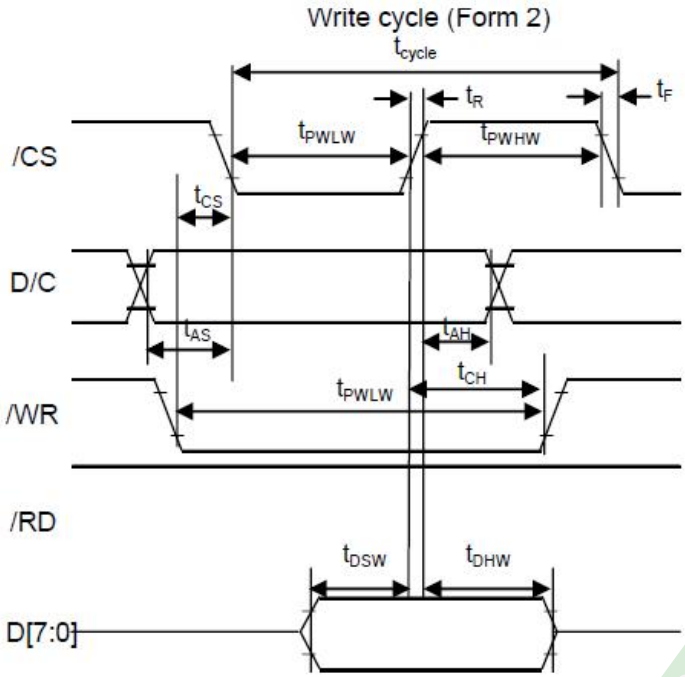
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	100	-	-	ns
t_{ACC}	Access Time (RAM) Access Time (command)	250 250	- -	- -	ns ns
t_{PWLR} t_{PWLR} t_{PWLW}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 50	- - -	- - -	ns ns ns
t_{PWHR} t_{PWHW}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	500 50	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

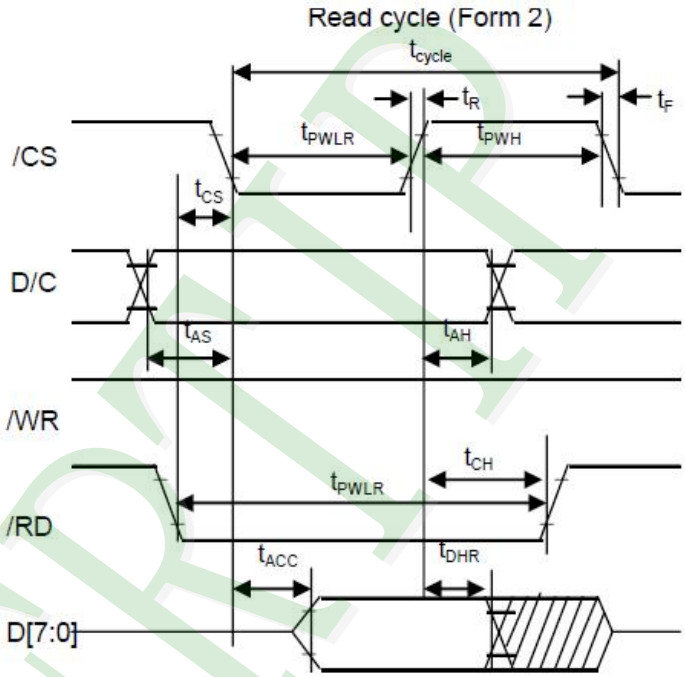
Note: All timings are based on 20% to 80% of VDDIO-VSS

Form 1: /CS low pulse width > /WR low pulse width



Form 2: /CS low pulse width < /WR low pulse width

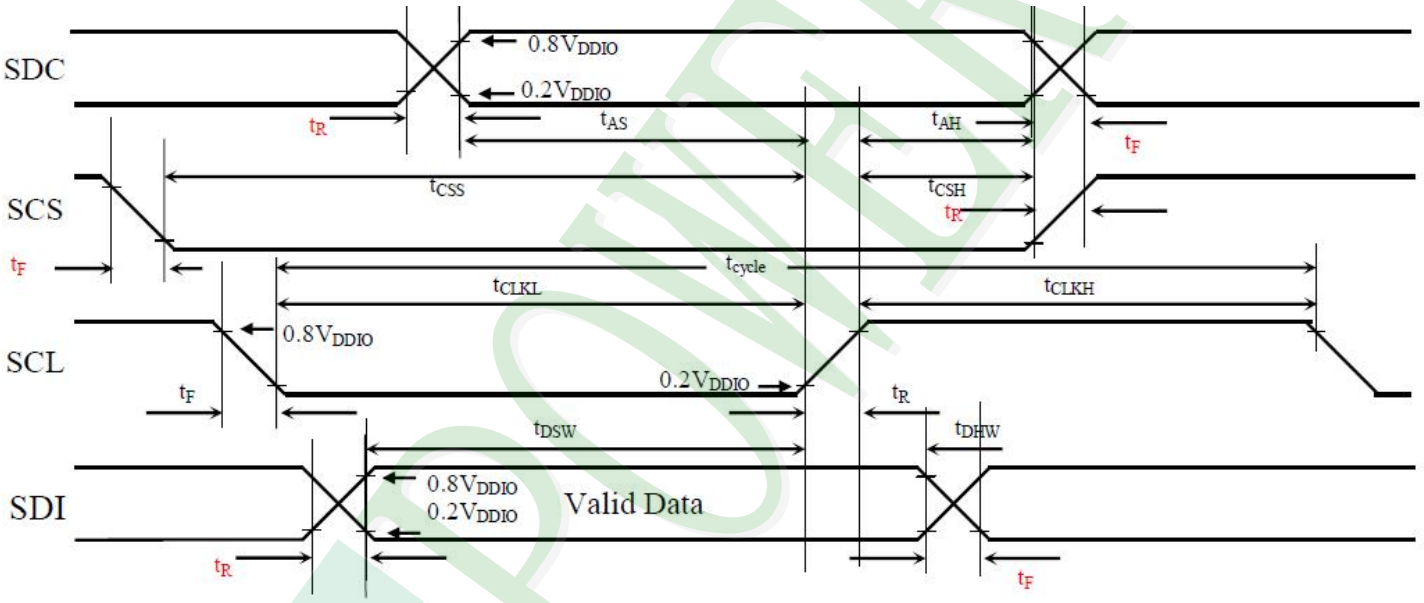




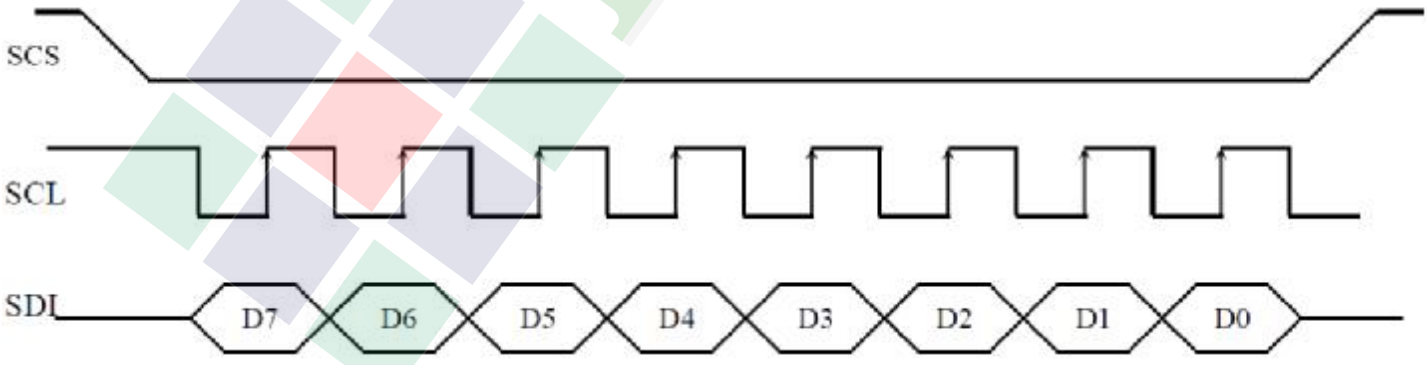
2.3.3 Serial Interface Timing

Ta= -20 to 70 °C，VDDIO = 3.0 to 3.6V

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	15	ns
t_F	Fall time	-	-	15	ns



Data format



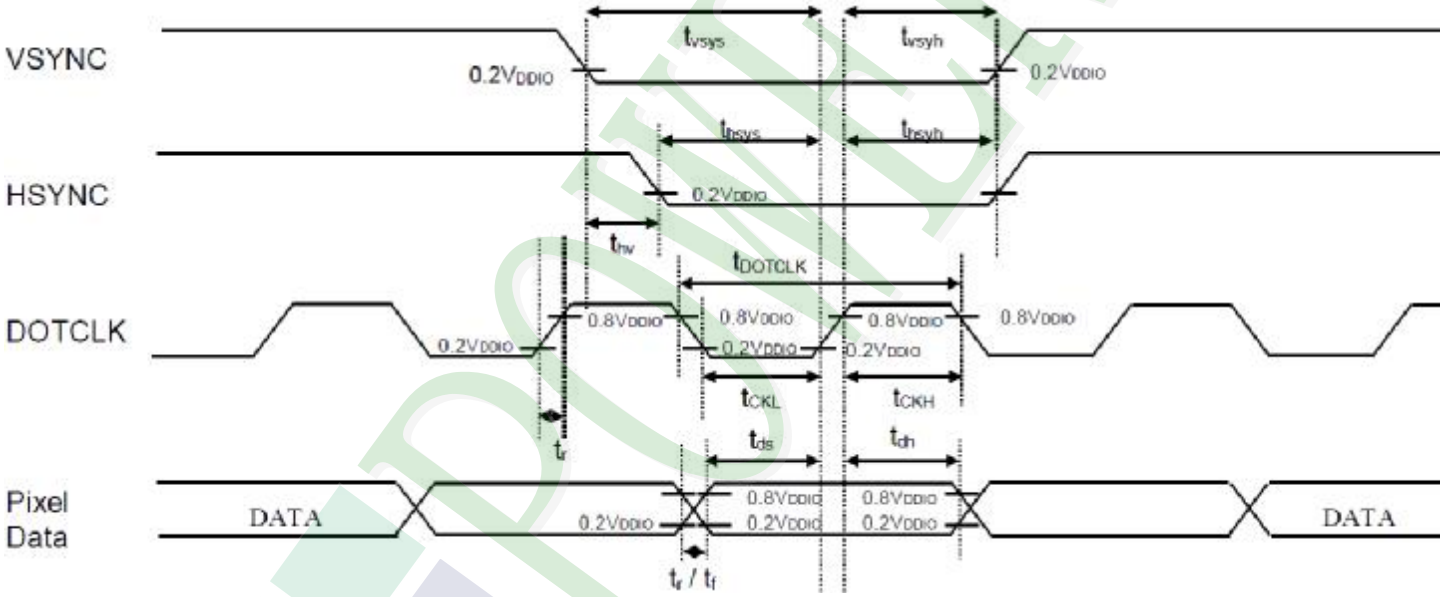
2.3.4 RGB Interface Timing

Ta= -20 to 70 °C，VDDIO = 3.0 to 3.6V

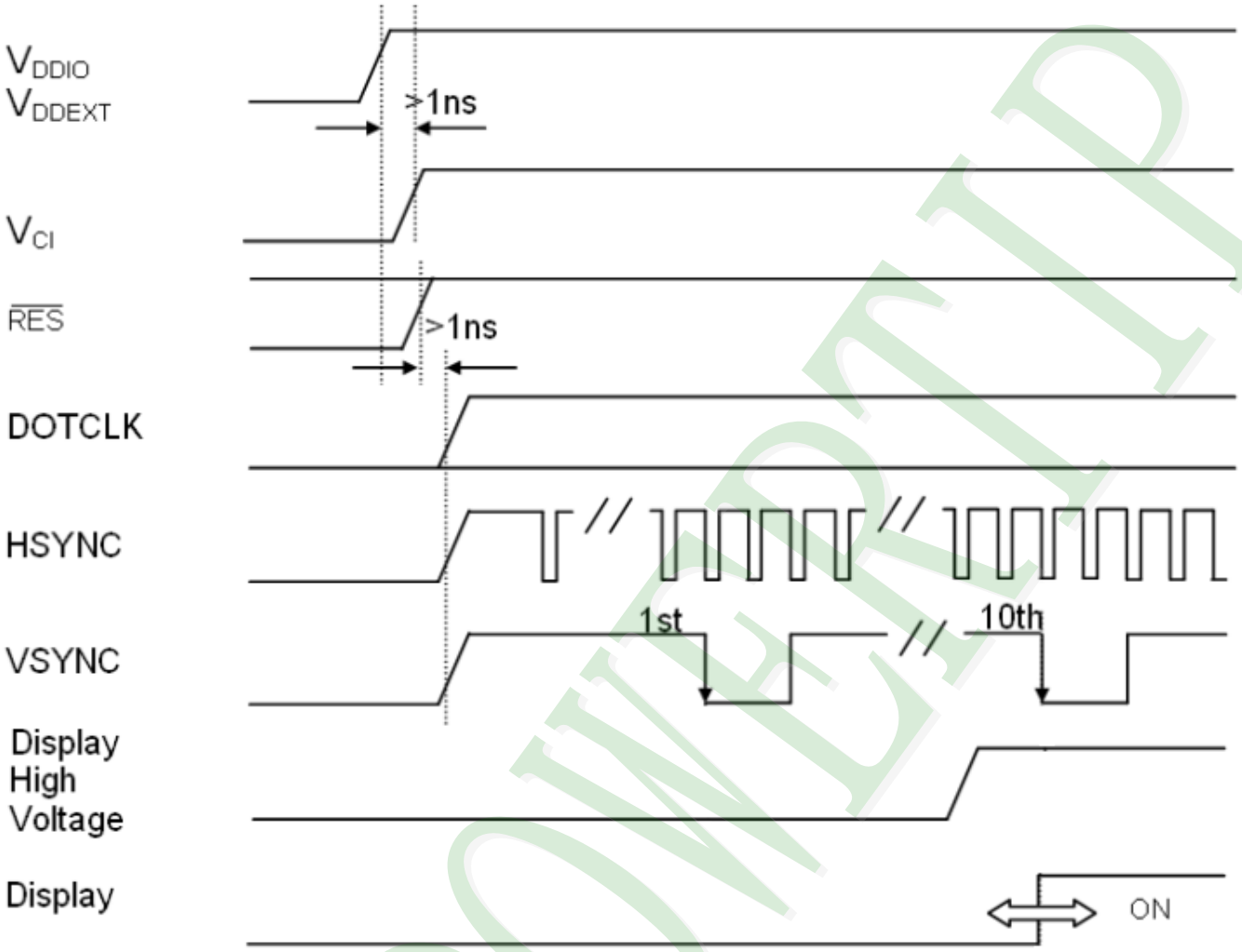
Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	HFP-1	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns

Note: External clock source must be provided to DOTCLK pin of SSD2119AM1. The driver will not operate in absence of the clocking signal.

*HFP: Horizontal Front Porch setting in customers' setup



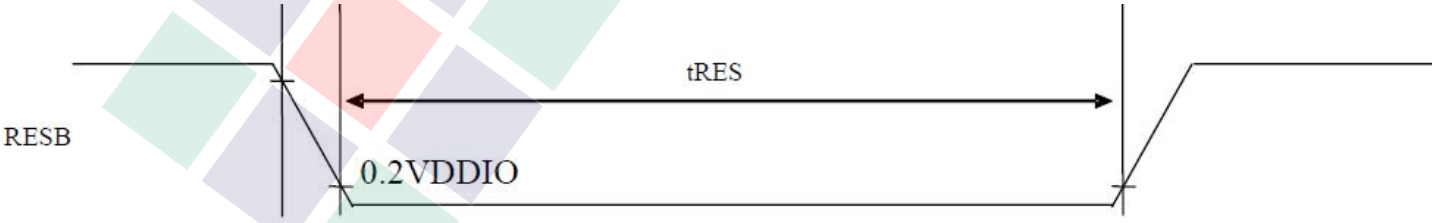
Power Up Sequence for RGB mode



2.3.5 Reset Timing

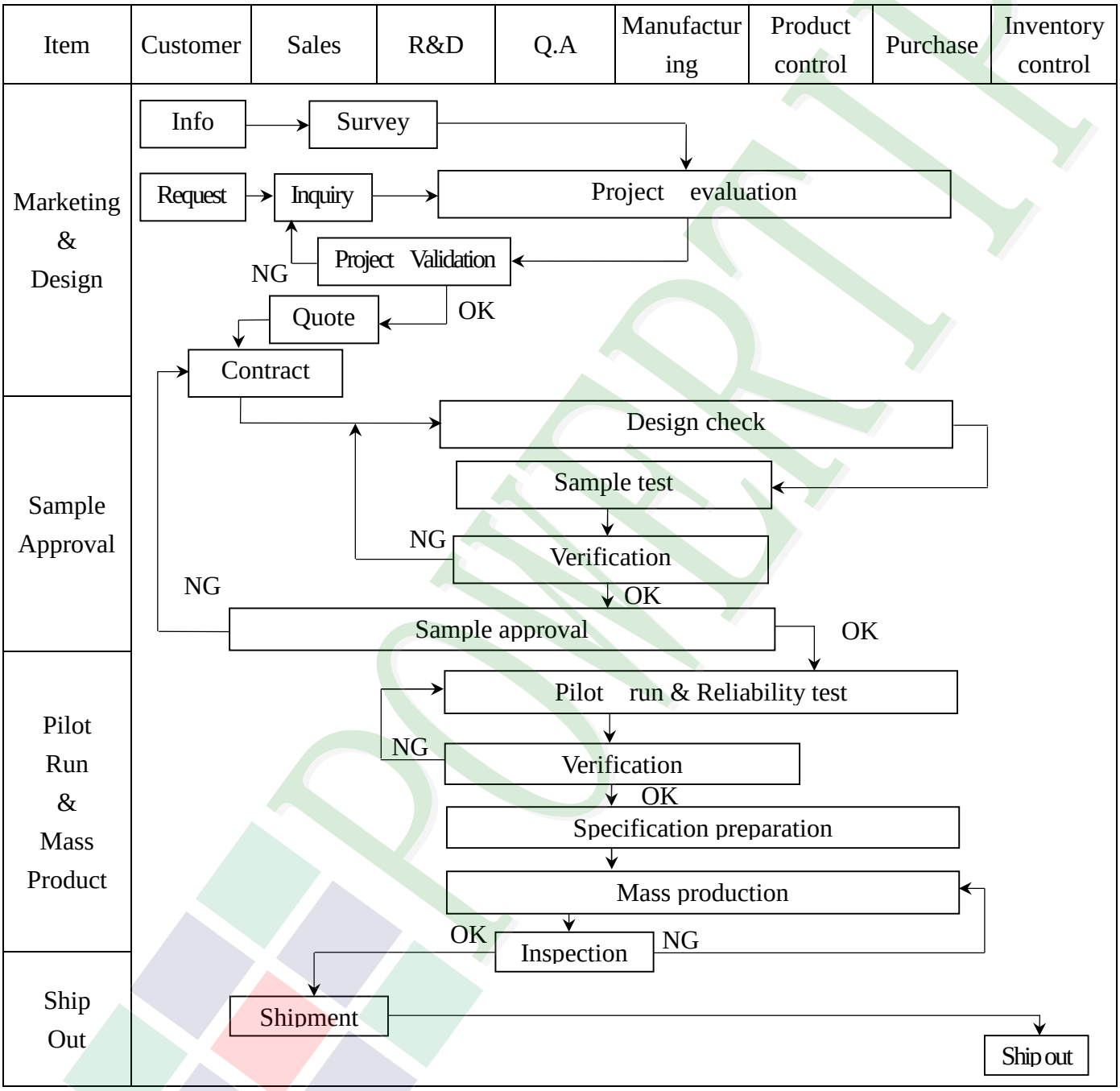
Ta= -20 to 70 °C，VDDIO = 3.0 to 3.6V

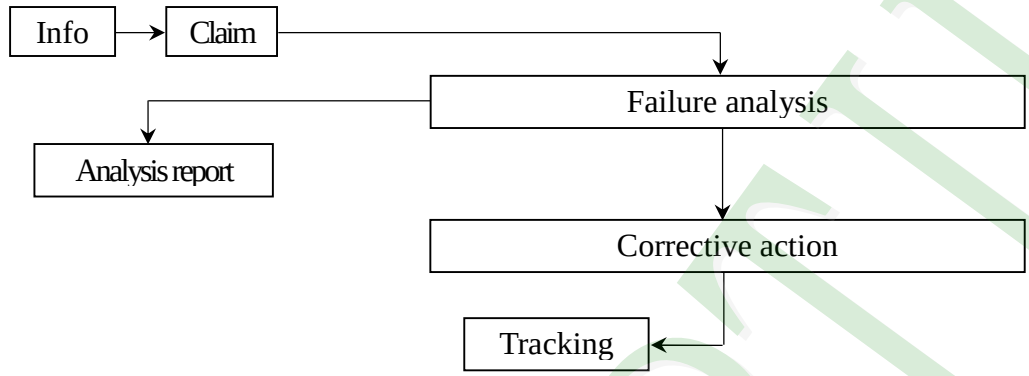
Symbol	Parameter	Min	Typ	Max	Unit
t_{RES}	Reset pulse duration	15	-	-	us



3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufacturing	Product control	Purchase	Inventory control
Sales Service								
Q.A Activity	1. ISO 9001 Maintenance Activities 2. Process improvement proposal 3. Equipment calibration 4. Education And Training Activities 5. Standardization Management							

3.2. Inspection Specification

◆Scope：The document shall be applied to TFT-LCD Module for 3.5″ ~10″ (Ver.B01).

◆Inspection Standard：MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

◆Equipment：Gauge、MIL-STD、Powertip Tester、Sample

◆Defect Level：Major Defect AQL： 0.4 ； Minor Defect AQL： 1.5

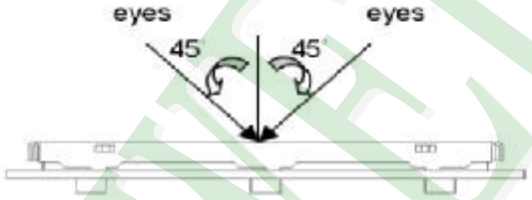
◆OUT Going Defect Level：Sampling.

◆Standard of the product appearance test：

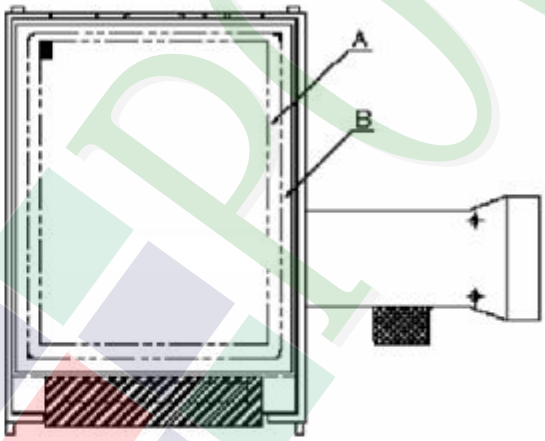
a. Manner of appearance test：

(1). The test best be under 20W×2 fluorescent light、and distance of view must be at 30 cm.

(2). The test direction is base on about around 45° of vertical line.



(3). Definition of area.



A area : viewing area

B area : Outside of viewing area

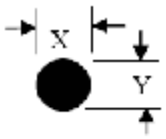
(4). Standard of inspection： (Unit：mm)

◆Specification For TFT-LCD Module 3.5″ ~10″ : (Ver.B01)

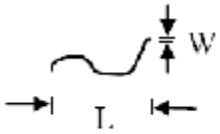
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="3">01</td><td rowspan="3">Product condition</td><td>1.1 The part number is inconsistent with work order of production.</td><td>Major</td></tr>
<tr><td>1.2 Mixed product types.</td><td>Major</td></tr>
<tr><td>1.3 Assembled in inverse direction.</td><td>Major</td></tr>
<tr><td>02</td><td>Quantity</td><td>2.1 The quantity is inconsistent with work order of production.</td><td>Major</td></tr>
<tr><td>03</td><td>Outline dimension</td><td>3.1 Product dimension and structure must conform to structure diagram.</td><td>Major</td></tr>
<tr><td rowspan="5">04</td><td rowspan="5">Electrical Testing</td><td>4.1 Missing line character and icon.</td><td>Major</td></tr>
<tr><td>4.2 No function or no display.</td><td>Major</td></tr>
<tr><td>4.3 Display malfunction.</td><td>Major</td></tr>
<tr><td>4.4 LCD viewing angle defect.</td><td>Major</td></tr>
<tr><td>4.5 Current consumption exceeds product specifications.</td><td>Major</td></tr>
<tr><td>05</td><td>Dot defect
(Bright dot、Dark dot)
On -display</td><td>
<table>
<tr><th colspan="2">Item</th><th>Acceptance (Q'ty)</th></tr>
<tr><td rowspan="4">Dot Defect</td><td>Bright Dot</td><td>≦ 4</td></tr>
<tr><td>Dark Dot</td><td>≦ 5</td></tr>
<tr><td>Joint Dot</td><td>≦ 3</td></tr>
<tr><td>Total</td><td>≦ 7</td></tr>
</table>
5.1 Inspection pattern : full white , full black , Red , Green and blue screens.
5.2 It is defined as dot defect if defect area >1/2 dot.
5.3 The distance between two dot defect ≥5 mm.
</td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module 3.5″ ~10″ : (Ver:B01)

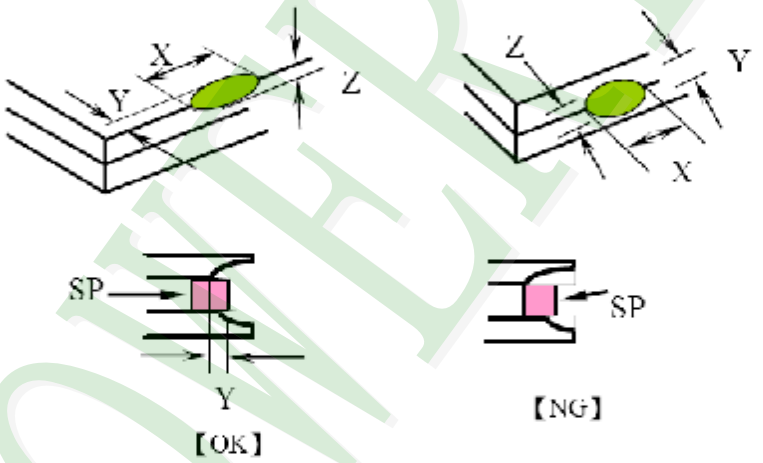
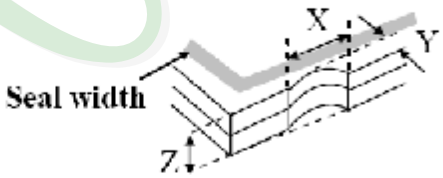
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>06</td><td>Black or white dot、scratch、contamination

Round type
 

Φ=(x+y) / 2

Line type
 
</td><td>6.1 Round type (Non-display or display) :
<table><tr><th rowspan="2">Dimension (diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>A area</th><th>B area</th></tr><tr><td>Φ ≦ 0.25</td><td>Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.25 < Φ ≦ 0.50</td><td>5</td></tr><tr><td>Φ > 0.50</td><td>0</td></tr><tr><td>Total</td><td>5</td></tr></table>
6.2 Line type(Non-display or display) :
<table><tr><th rowspan="2">Length (L)</th><th rowspan="2">Width (W)</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>A area</th><th>B area</th></tr><tr><td>---</td><td>W ≦ 0.03</td><td>Ignore</td><td rowspan="5">Ignore</td></tr><tr><td>L ≦10.0</td><td>0.03 < W ≦ 0.05</td><td>4</td></tr><tr><td>L ≦5.0</td><td>0.05 < W ≦ 0.10</td><td>2</td></tr><tr><td>---</td><td>W >0.10</td><td>As round type</td></tr><tr><td colspan="2">Total</td><td>5</td></tr></table></td><td>Minor</td></tr>
<tr><td>07</td><td>Polarizer Bubble</td><td><table><tr><th rowspan="2">Dimension (diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>A area</th><th>B area</th></tr><tr><td>Φ ≦ 0.25</td><td>Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.25 < Φ ≦ 0.50</td><td>4</td></tr><tr><td>0.50 < Φ ≦ 0.80</td><td>1</td></tr><tr><td>Φ > 0.80</td><td>0</td></tr><tr><td>Total</td><td>5</td></tr></table></td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module 3.5″ ~10″ : (Ver:B01)

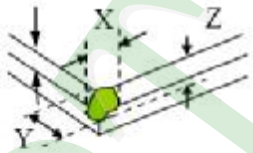
NO	Item	Criterion	Level
08	The crack of glass	Symbols : X : The length of crack Z : The thickness of crack t : The thickness of glass Y : The width of crack. W : terminal length a : LCD side length 8.1 General glass chip : 8.1.1 Chip on panel surface and crack between panels:   	Minor

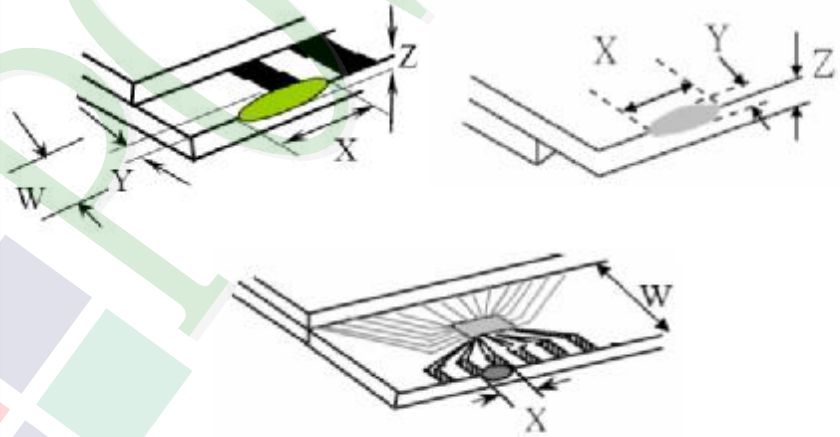
X	Y	Z
≦ a	Crack can't enter viewing area	≤1/2 t
≦ a	Crack can't exceed the half of SP width.	1/2 t < Z ≦2 t

◆Specification For TFT-LCD Module 3.5″ ~10″ : (Ver.B01)

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="2">08</td><td rowspan="2">The crack of glass</td><td>Symbols :

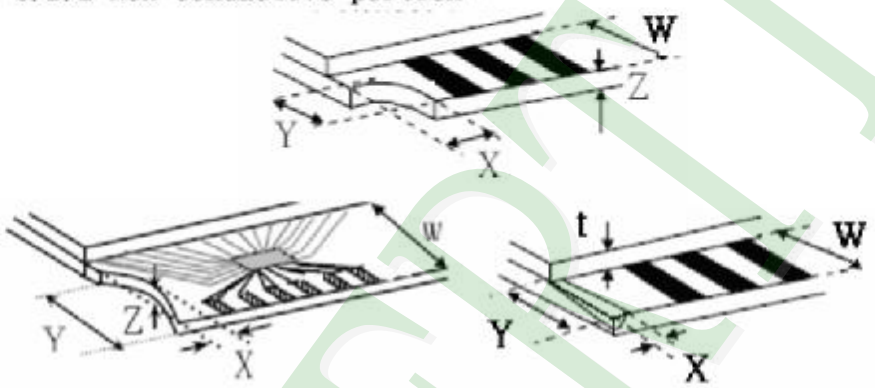
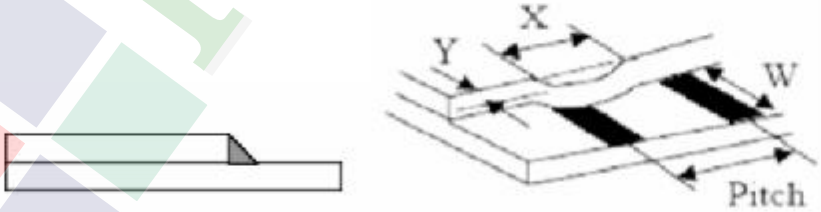
X : The length of crack
Z : The thickness of crack
t : The thickness of glass
Y : The width of crack.
W : terminal length
a : LCD side length

8.1.2 Corner crack :
 

<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≦1/5 a</td><td>Crack can't enter viewing area</td><td>Z ≦1/2 t</td></tr><tr><td>≦1/5 a</td><td>Crack can't exceed the half of SP width.</td><td>1/2 t < Z ≦2 t</td></tr></table></td><td></td></tr>
<tr><td>8.2 Protrusion over terminal :
8.2.1 Chip on electrode pad :
 

<table><tr><th></th><th>X</th><th>Y</th><th>Z</th></tr><tr><td>Front</td><td>≦ a</td><td>≦ 1/2 W</td><td>≦ t</td></tr><tr><td>Back</td><td>≦ a</td><td>≦ W</td><td>≦ 1/2 t</td></tr></table></td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module 3.5″ ~10″ : (Ver.B01)

NO	Item	Criterion	Level
08	The crack of glass	Symbols : X : The length of crack Y : The width of crack. Z : The thickness of crack W : terminal length t : The thickness of glass a : LCD side length 8.2.2 Non-conductive portion :  X: ≦ 1/3 a; Y: ≦ W; Z: ≦t ⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. 8.2.3 Glass remain :  X: ≦ a; Y: ≦ 1/3 W; Z: ≦t	Minor

4. RELIABILITY TEST

4.1 Reliability Test Condition (VER.B01)

<table>
<tr><th>NO.</th><th>TEST ITEM</th><th>TEST CONDITION</th></tr>
<tr><td>1</td><td>High Temperature Storage Test</td><td>Keep in 80℃ ±2℃ 96 hrs
Surrounding temperature, then storage at normal condition 4hrs.</td></tr>
<tr><td>2</td><td>Low Temperature Storage Test</td><td>Keep in -30℃ ±2℃ 96 hrs
Surrounding temperature, then storage at normal condition 4hrs.</td></tr>
<tr><td>3</td><td>High Temperature / High Humidity Storage Test</td><td>Keep in +60 ℃ / 90% R.H duration for 96 hrs
Surrounding temperature, then storage at normal condition 4hrs.
(Excluding the polarizer)</td></tr>
<tr><td>4</td><td>Temperature Cycling Storage Test</td><td>-30℃ → +25℃ → +80℃ → +25℃
(30mins) (5mins) (30mins) (5mins)
10 Cycle
Surrounding temperature, then storage at normal condition 4hrs.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">ESD Test</td><td>Air Discharge:
Apply 2 KV with 5 times
Discharge for each polarity +/-
Contact Discharge:
Apply 250 V with 5 times
discharge for each polarity +/-</td></tr>
<tr><td>1. Temperature ambiance : 15℃～35℃
2. Humidity relative : 30%～60%
3. Energy Storage Capacitance(Cs+Cd) : 150pF±10%
4. Discharge Resistance(Rd) : 330Ω±10%
5. Discharge, mode of operation :
Single Discharge (time between successive discharges at least 1 sec)
(Tolerance if the output voltage indication : ±5%)</td></tr>
<tr><td>6</td><td>Vibration Test (Packaged)</td><td>1. Sine wave 10～55 Hz frequency (1 min/sweep)
2. The amplitude of vibration :1.5 mm
3. Each direction (X、Y、Z) duration for 2 Hrs</td></tr>
<tr><td>7</td><td>Drop Test (Packaged)</td><td><table><tr><th>Packing Weight (Kg)</th><th>Drop Height (cm)</th></tr><tr><td>0 ~ 45.4</td><td>122</td></tr><tr><td>45.4 ~ 90.8</td><td>76</td></tr><tr><td>90.8 ~ 454</td><td>61</td></tr><tr><td>Over 454</td><td>46</td></tr></table>Drop Direction :※1 corner / 3 edges / 6 sides each 1time.</td></tr>
</table>

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.

5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

5.2.1 Avoid any strong mechanical shock which can break the glass.

5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.

5.2.3 Do not remove the panel or frame from the module.

5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully, do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)

5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.

5.2.6 Do not touch the display area with bare hands , this will stain the display area.

5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

5.2.8 To control temperature and time of soldering is 320 ± 10°C and 3-5 sec.

5.2.9 To avoid liquid (include organic solvent) stained on LCM.

5.3 STORAGE

5.3.1 Store the panel or module in a dark place where the temperature is 25°C ± 5°C and the humidity is below 65% RH.

5.3.2 Do not place the module near organics solvents or corrosive gases.

5.3.3 Do not crush , shake , or jolt the module.

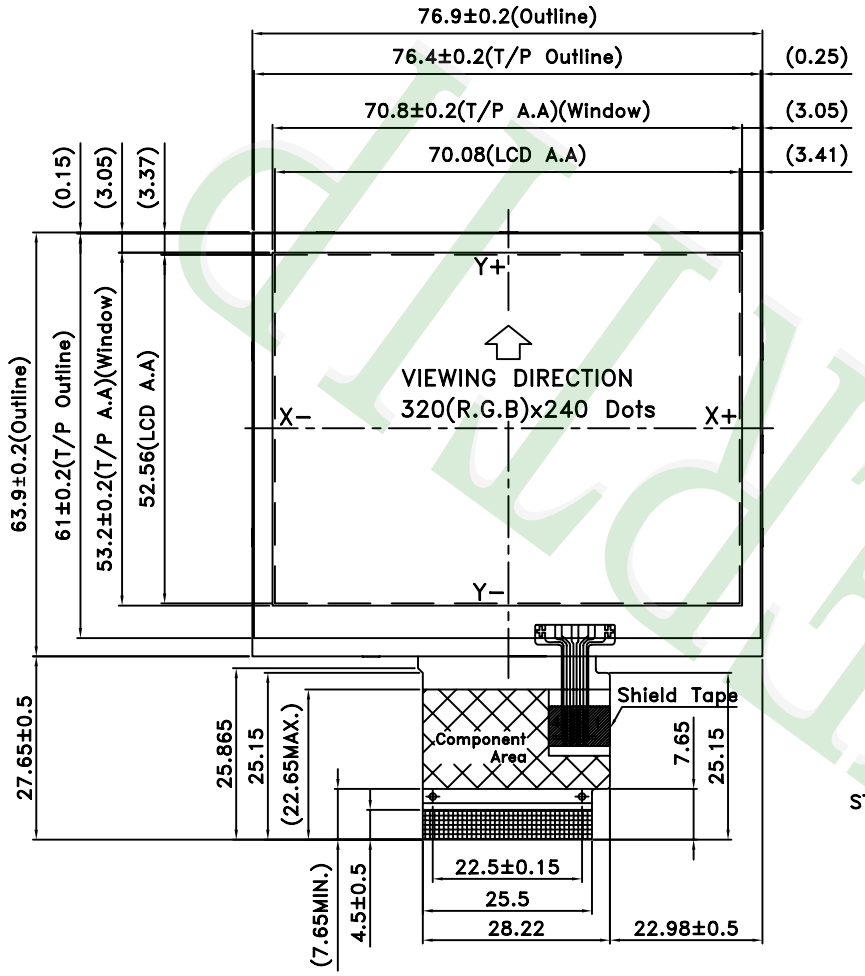
5.4 TERMS OF WARRANTY

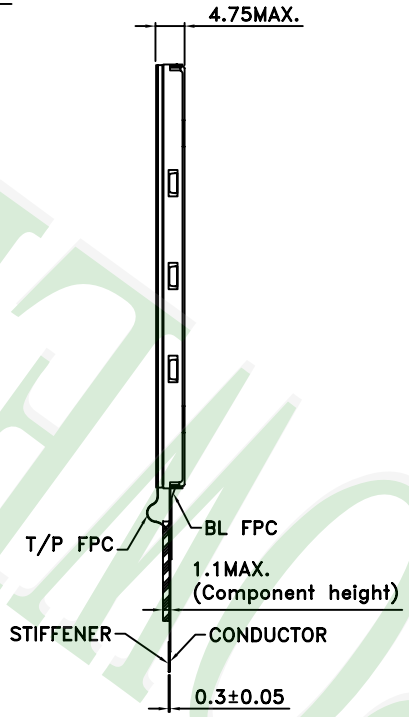
5.4.1 Applicable warrant period

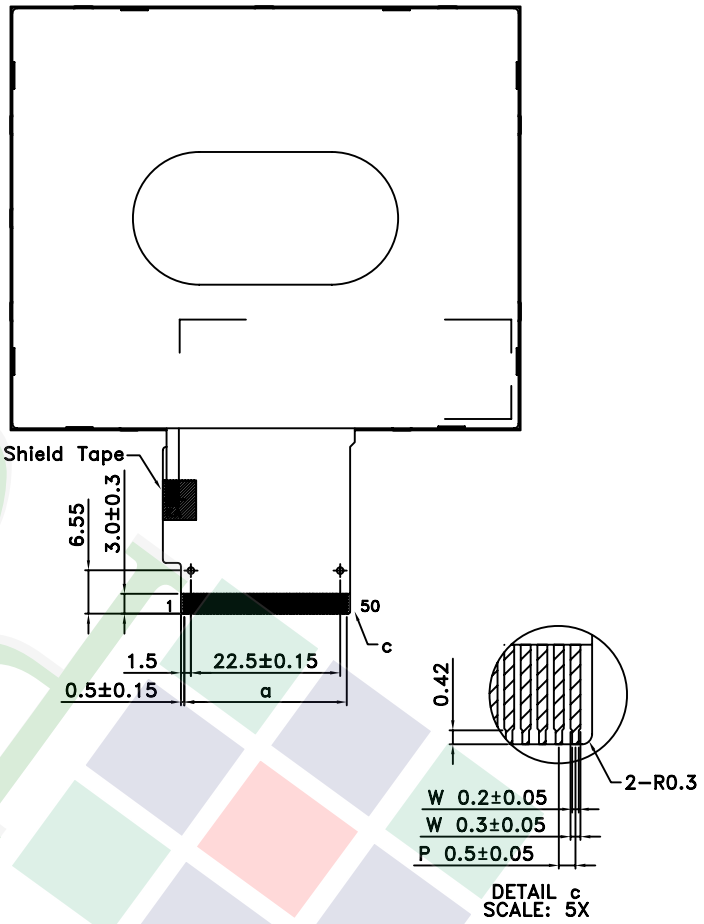
The period is within thirteen months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.







NOTES:
1. LCD TYPE: a-SI TFT
2. LCD DISPLAY: POSITIVE/TRANSMISSIVE
3. VIEW DIRECTION: 6 O'CLOCK
4. The tolerance unless classified ±0.2mm
5. IC No.: ILI9322 OR COMPARABLE DRIVER IC
6. a: PITCH 0.5X49=24.5±0.1
7. FPC suggested connector : (ENTERY)6701K-E50N-00L or compatible

REV	REV BY	REVISER	DATE
007			
006			
005			
004			
003			
002	Add CN	Sally	2014/04/08
001	NEW DRAWING	Sally	2013/03/26

PART NO: PH320240T-022-I09Q

DRAWING NAME : JLMD-PH320240T-022-I09Q

TITLE: LCD MODULE DRAWING

久正光電股份有限公司
POWERTIP TECHNOLOGY CORPORATION

Design	Sally	(3)	Surface		
Check	Terry	Unit	MM	Material	
Approve	Ryan	Scale	1:1	Thickness	
		Page	1/1	Quantity	

Precision Level (Length(Min) (mm) / Tolerance / Precision)	Precision Level
1 ~ 4	-
4 ~ 16	-
16 ~ 63	-
63 ~ 250	-
250 ~ 1000	-

Ver.001	
Documents NO.	JPKG-PH320240T-022-I09Q

LCM包裝規格書
LCM Packaging Specifications (For Tray)

Approve	Check	Contact
Ryan	Terry	Sally

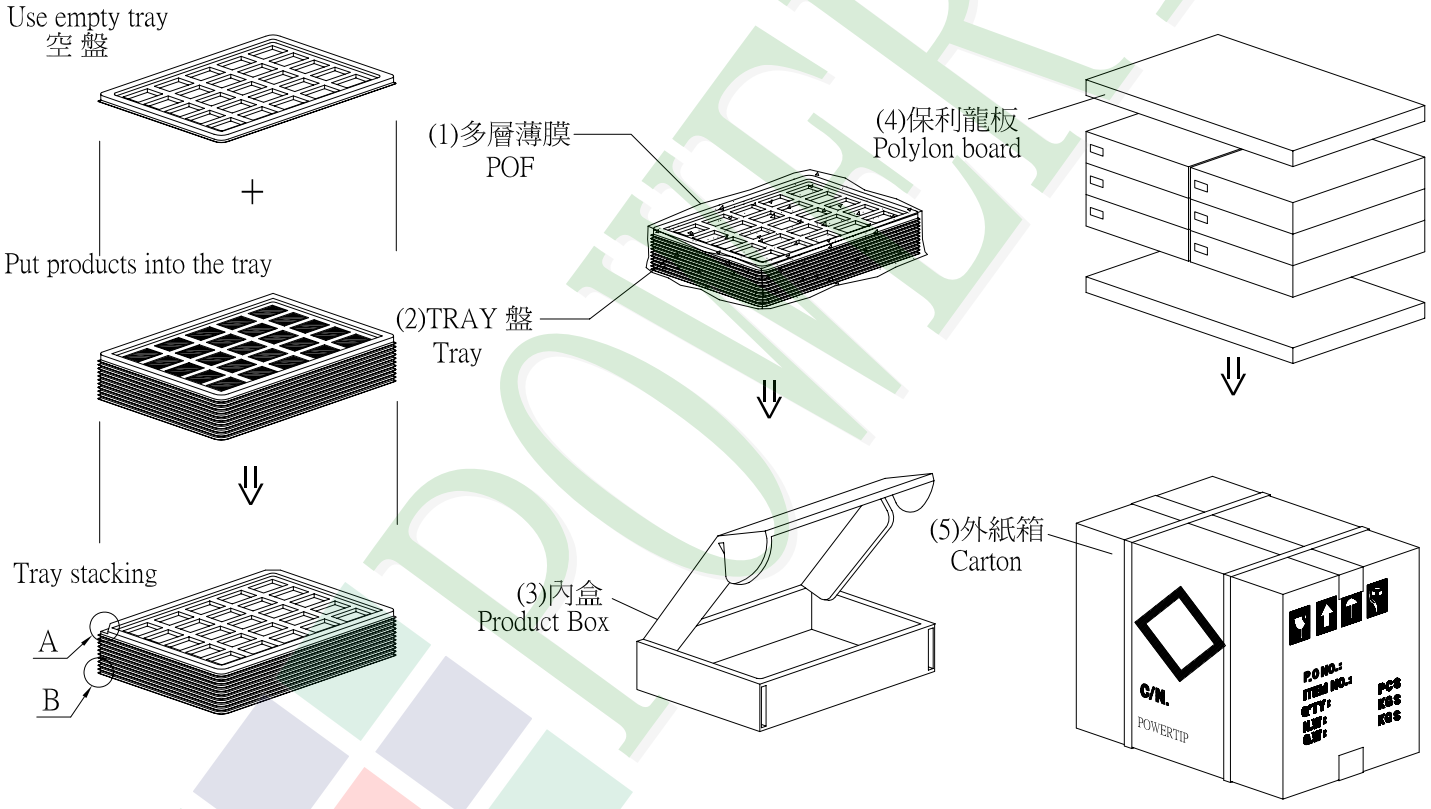
1.包裝材料規格表 (Packaging Material) : (per carton)

No.	Item	Model	Dimensions (mm)	1Pcs Weight	Quantity	Total Weight
1	成品 (LCM)	PH320240T-022-I09Q	76.9 X 63.9 X 4.75(MAX)	0.038	252	9.576
2	多層薄膜(1)POF	OTFILM0BA03ABA	19"X350X0.015	——	6	——
3	TRAY 盤 (2)Tray	TYPH32024004BA	352 X 260 X 12.8	0.0999	48	4.7952
4	內盒(3)Product Box	BX36627063ABBA	393 X 274 X 68	0.2692	6	1.6152
5	保利龍板(4)Polylon board	OTPLB00PL08ABA	550 X 393 X 20	0.0284	2	0.0568
6	外紙箱(5)Carton	BX57041027CCBA	570 X 410 X 265	1.4208	1	1.4208
7						
8						
9						

2.一 整箱總重量 (Total LCD Weight in carton) : 17.46 Kg±10%

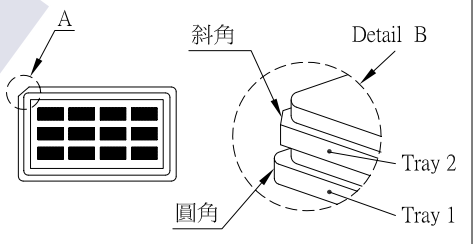
3.單箱數量規格表 (Packaging Specifications and Quantity) :

(1)LCM quantity per box : no per tray	6	x no of tray	7	=	42
(2)Total LCM quantity in carton : quantity per box	42	x no of boxes	6	=	252



特 記 事 項 (REMARK)

1. Label Specifications :
參照作業標準書內容



2.TRAY盤相疊時,需旋轉180度,請詳見B視圖
Rotate tray 180 degrees and place on top of stack.
Check the tray stack using Fig. B.

3.可適用於單品包裝
It's also suitable to Panel

4.Tray料號:
Tray Number:PT-PH320240T-004-1