

SPECIFICATIONS

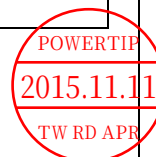
CUSTOMER	:	HCN070
SAMPLE CODE	:	SH320480T009-LAA01
MASS PRODUCTION CODE	:	PH320480T009-LAA01
SAMPLE VERSION	:	01
SPECIFICATIONS EDITION	:	002
DRAWING NO. (Ver.)	:	LMD-PH320480T009-LAA01 (Ver.001)
PACKAGING NO. (Ver.)	:	PKG-PH320480T009-LAA01 (Ver.001)

Customer Approved

Date:

Approved	Checked	Designer
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- ☐ Preliminary specification for design input
☒ Specification for sample approval



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History of Version

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Note : For detailed information please refer to IC data sheet : ST7796S-G5

1. SPECIFICATIONS

1.1 Features

Main LCD panel

Item	Standard Value
Display Type	320 * 3 (RGB) * 480 Dots
LCD Type	a-Si TFT , Normally white, Transmissive type
Screen size(inch)	3.5 inch
Viewing Direction	12 O'clock
Color configuration	RGB-Strip
Backlight	LED Backlight
Interface	Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit, and 18-bit) 16/18 RGB Interface Serial Peripheral Interface (SPI Interface) MIPI Interface
Other(controller/driver IC)	ST7796S-G5
ROHS	THIS PRODUCT CONFORMS THE ROHS OF PTC Detail information please refer website : http://www.powertip.com.tw/news.php?area_id_view=1085560481/

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	55.26(W) x 84.69 (L) x 2.7(H)	mm
Viewing Area	49.96(W) x 74.44(L)	mm
Active Area	48.96 (W) * 73.44 (L)	mm

Note : For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Module

Item	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	VDD	-	-0.3	+4.6	V
Supply Voltage(I/O)	VDDI	-	-0.3	+4.6	V
Operating Temperature	T _{OP}	-	-20	+70	°C
Storage Temperature	T _{ST}	-	-30	+80	°C

1.4 DC Electrical Characteristics

Module

GND = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	-	2.5	2.8	3.3	V
Supply Voltage(I/O)	VDDI	-	1.65	1.8	3.3	V
Input High Voltage	V _{IH}	-	0.7 VDDI	-	VDDI	V
Input Low Voltage	V _{IL}	-	GND	-	0.3 VDDI	V
Output High Voltage	V _{OH}	I _{OH} =-0.1mA	0.8*VDDI	-	VDDI	V
Output Low Voltage	V _{OL}	I _{OL} =+0.1mA	GND	-	0.2*VDDI	V
Supply Current	IDD	Pattern= Full display	-	15	20	mA

Note1:Maximum current display

1.5 Optical Characteristics

TFT LCD Module

VDD=VDDI = 3.3V, Ta=25°C

Item		Symbol	Condition	Min.	Typ.	Max.	unit	-
Response time		Tr+ Tf	Ta = 25°C θX, θY = 0°	-	25	38	ms	Note2
Viewing angle	Top	θY+	-	-	60	-	Deg.	Note4
	Bottom	θY-		-	60	-		
	Left	θX-		-	60	-		
	Right	θX+		-	60	-		
Contrast ratio		CR	Ta = 25°C θX , θY = 0°	500	600	-	-	Note3
Color of CIE Coordinate (With B/L & T/P)	White	X	-	0.24	0.29	0.34	-	Note1
		Y		0.27	0.32	0.37		
	Red	X		0.55	0.60	0.65		
		Y		0.30	0.35	0.40		
	Green	X		0.28	0.33	0.38		
		Y		0.57	0.62	0.67		
	Blue	X		0.09	0.14	0.19		
		Y		0.02	0.07	0.12		
Average Brightness Pattern=white (With LCD) *1		IV	IF=120 mA	350	430	-	cd/m ²	
Uniformity (With LCD) *2		△B	IF=120 mA	70	-	-	%	

Note 1:

*1 : $\Delta B = B(\min) / B(\max) * 100\%$

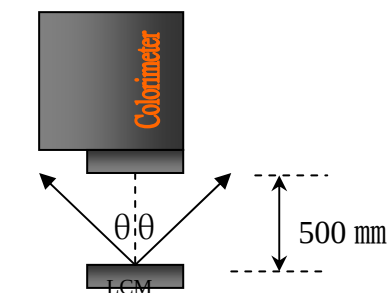
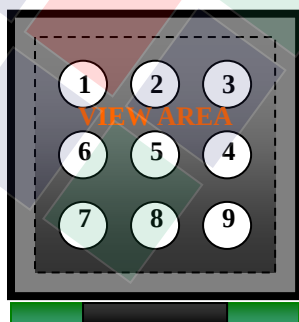
*2 : Measurement Condition for Optical Characteristics:

a : Environment: 25°C±5°C / 60±20%R.H, no wind, dark room below 10 Lux at typical lamp current and typical operating frequency.

b : Measurement Distance: 500 ± 50 mm , (θ= 0°)

c : Equipment: TOPCON BM-7 fast, (field 1°), after 10 minutes operation.

d : The uncertainty of the C.I.E coordinate measurement ±0.01, Average Brightness ± 4%



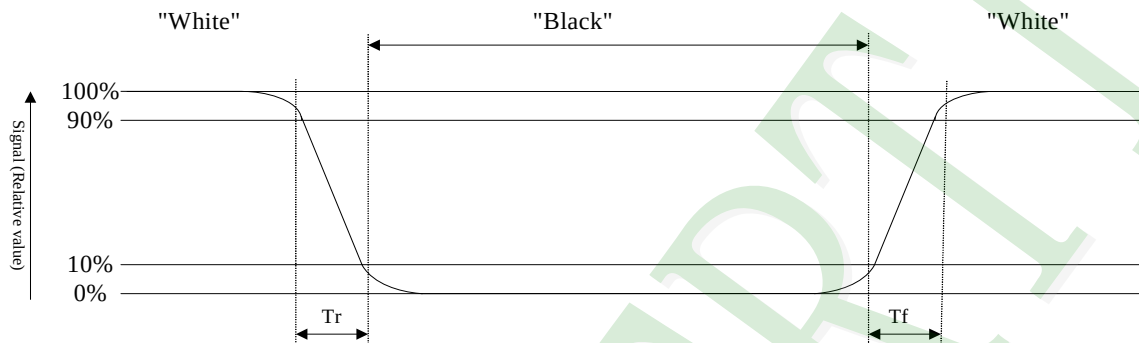
Colorimeter=BM-7 fast

To be measured at the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 10 minutes operation (module)

Note2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:



Note3: Definition of contrast ratio:

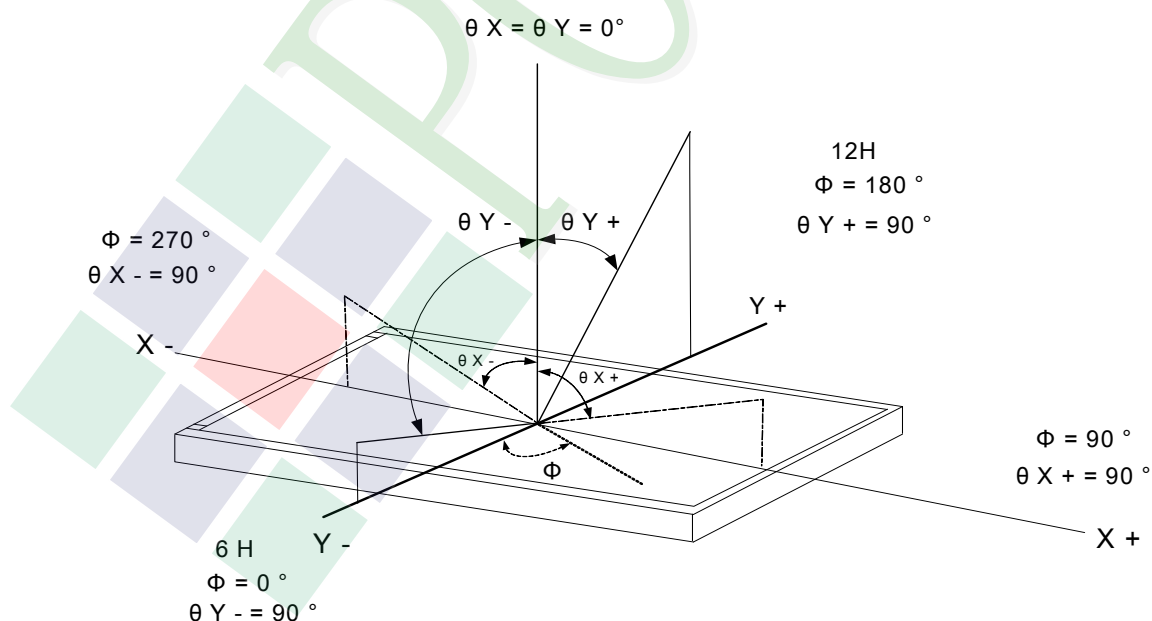
Contrast ratio is calculated with the following formula

Photo detector output when LCD is at “White” state

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note4: Definition of viewing angle:

Refer to figure as below:



1.6 Backlight Characteristics

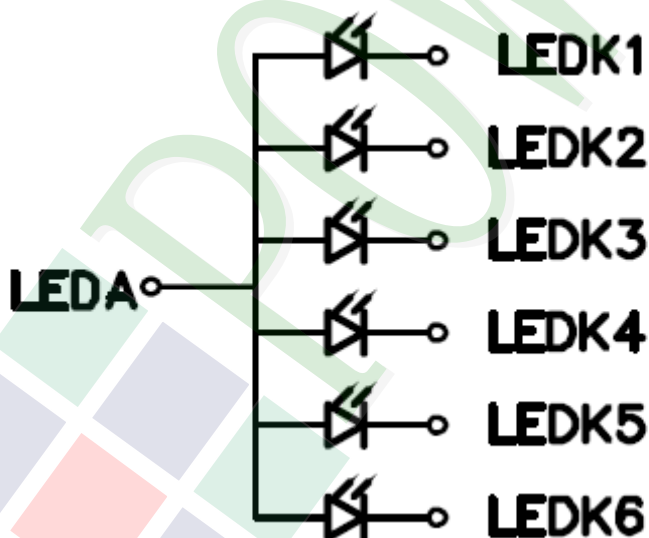
Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25°C	-	150	mA
Reverse Voltage	VR	Ta =25°C	-	4	V
Power Dissipation	PD	Ta =25°C	-	540	mW

Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	VF	IF= 120 mA	2.8	3.2	3.6	V
Average Brightness (Without LCD)	IV		6000	7200	-	cd/m ²
CIE Color Coordinate (Without LCD)	X		0.26	0.28	0.32	-
	Y		0.26	0.28	0.32	
Color	White					

Circuit diagram :



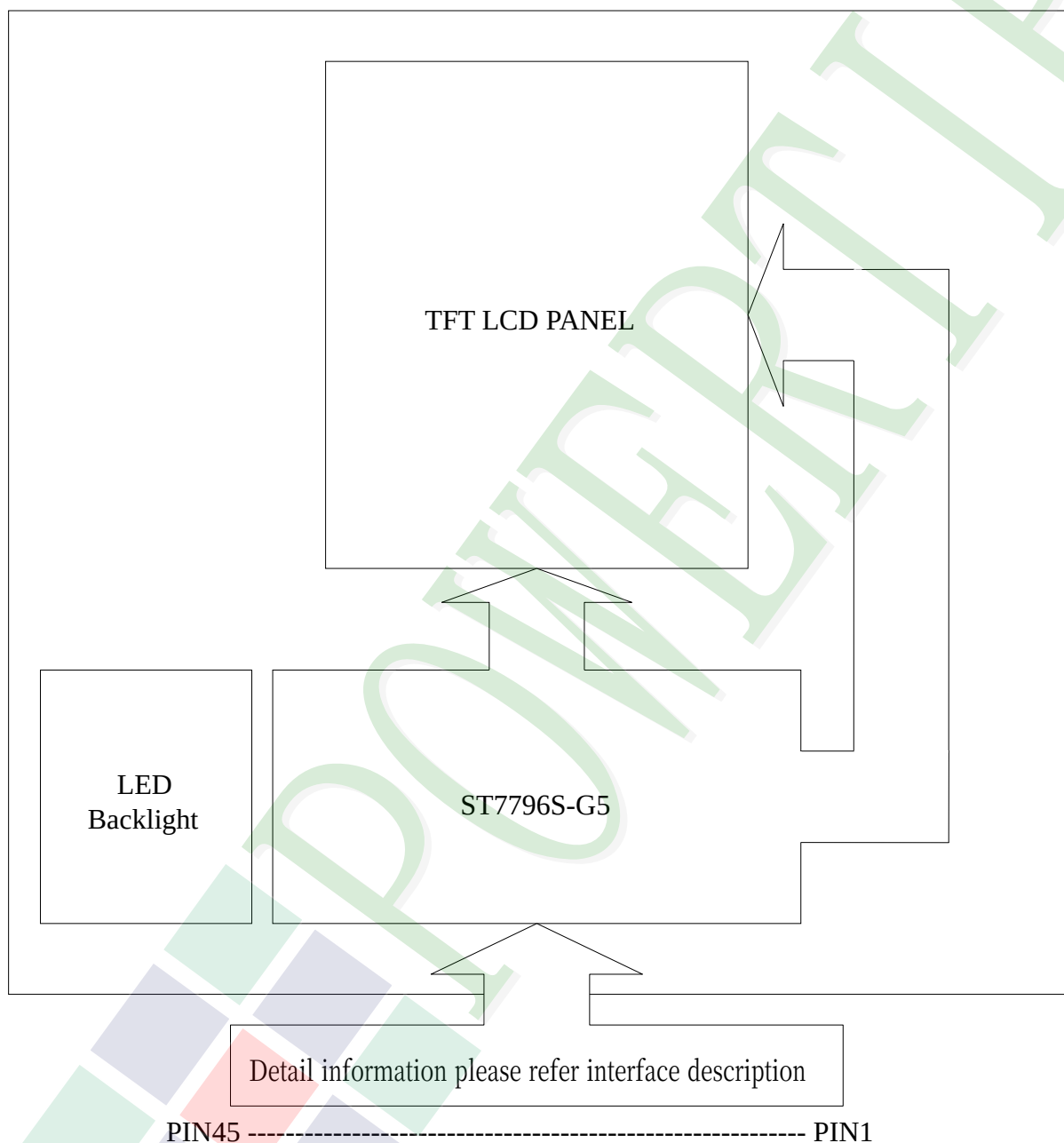
Item	Conditions	Description
Life Time	Ta =25°C	20000 hrs
	IF= 120 mA	

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram



2.2 Interface Pin Description

Pin No.	Symbol	Function
1	LEDK6-	Power supply for LED Backlight cathode input
2	LEDK5-	
3	LEDK4-	
4	LEDK3-	
5	LEDK2-	
6	LEDK1-	
7	LED A	Power supply for LED Backlight anode input
8	GND	Ground
9	VDD	Power supply for analog and booster circuits
10	VDDI	Power supply for I/O system. VDDI must be lower than or equal to VDD.
11	TE	Tearing Effect output signal. Leave the pin open when not in use.
12	CSX	Chip selection pin. Low-active. If not used, please fix this pin at VDDI or DGND level.
13	DCX	Display data/command selection (RS) pin in MCU interface. DCX='1': display data or parameter. DCX='0': register index / command. If not used, please fix this pin at VDDI or DGND level.
14	WRX/SCL	Write enable in MCU parallel interface. In SPI mode, this pin is used as SCL. If not used, please fix this pin at VDDI or DGND level.
15	RDX	Read enable in 8080 MCU parallel interface. Low-active. If not used, please fix this pin at VDDI or DGND level.
16	SDA	SPI interface input/output pin. The data is latched on the rising edge of the SCL signal. If not used, please fix this pin at VDDI or DGND level.
17	SDO	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. If not used, please fix this pin at floating.
18	DB0	Data bus Fix to GND level when not in use.
19	DB1	
20	DB2	
21	DB3	

22	DB4	Data bus Fix to GND level when not in use.																																													
23	DB5																																														
24	DB6																																														
25	DB7																																														
26	DB8																																														
27	DB9																																														
28	DB10																																														
29	DB11																																														
30	DB12																																														
31	DB13																																														
32	DB14																																														
33	DB15																																														
34	DB16	<table><tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr><tr><td>0</td><td>0</td><td>0</td><td>8080 18-bit Interface</td><td>DB[17:0]</td></tr><tr><td>0</td><td>0</td><td>1</td><td>8080 9-bit Interface</td><td>DB[8:0]</td></tr><tr><td>0</td><td>1</td><td>0</td><td>8080 16-bit Interface</td><td>DB[15:0]</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8080 8-bit Interface</td><td>DB[7:0],</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Reserve</td><td>--</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3SPI</td><td>SDA, SDO</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MIPI</td><td>MIPI_DATA MIPI_CLOCK</td></tr><tr><td>1</td><td>1</td><td>1</td><td>4Line SPI</td><td>SDA, SDO</td></tr></table>	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	8080 18-bit Interface	DB[17:0]	0	0	1	8080 9-bit Interface	DB[8:0]	0	1	0	8080 16-bit Interface	DB[15:0]	0	1	1	8080 8-bit Interface	DB[7:0],	1	0	0	Reserve	--	1	0	1	3SPI	SDA, SDO	1	1	0	MIPI	MIPI_DATA MIPI_CLOCK	1	1	1	4Line SPI	SDA, SDO
IM2	IM1	IM0	MPU Interface Mode	Data pin																																											
0	0	0	8080 18-bit Interface	DB[17:0]																																											
0	0	1	8080 9-bit Interface	DB[8:0]																																											
0	1	0	8080 16-bit Interface	DB[15:0]																																											
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1	0	0	Reserve	--																																											
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1	1	0	MIPI	MIPI_DATA MIPI_CLOCK																																											
1	1	1	4Line SPI	SDA, SDO																																											
35	DB17																																														
36	ENABLE	Data enable signal for RGB interface operation. If not used, please fix this pin at VDDI or DGND.																																													
37	DOTLCK	Dot clock signal for RGB interface operation. If not used, please fix this pin at VDDI or DGND.																																													
38	HSYNC	Horizontal synchronizing input signal for RGB interface operation. If not used, please fix to VDDI or DGND.																																													
39	GND	Ground																																													
40	VSYNC	Vertical synchronizing input signal for RGB interface operation. If not used, please fix to the VDDI or DGND.																																													
41	RESET	This signal will reset the device and it must be applied to properly initialize the chip. Signal is active low.																																													
42	IM2	The MCU interface mode select.																																													
43	IM1																																														
44	IM0																																														
45	GND	Ground																																													

2.2.1 Refer Initial Code : (RGB interface)

```
CALL    DELAY
CALL    DELAY
MOV     DPL,#11H
CALL    SPI_COM

CALL    DELAY
CALL    DELAY
CALL    DELAY
CALL    DELAY

MOV     DPL,#F0H
CALL    SPI_COM
MOV     DPL,#C3H
CALL    SPI_DAT

MOV     DPL,#F0H
CALL    SPI_COM
MOV     DPL,#96H
CALL    SPI_DAT

MOV     DPL,#36H
CALL    SPI_COM
MOV     DPL,#48H
CALL    SPI_DAT

MOV     DPL,#B4H
CALL    SPI_COM
MOV     DPL,#01H
CALL    SPI_DAT

MOV     DPL,#B6H
CALL    SPI_COM
MOV     DPL,#20H
CALL    SPI_DAT
MOV     DPL,#02H
CALL    SPI_DAT
MOV     DPL,#3BH
CALL    SPI_DAT

MOV     DPL,#E8H
CALL    SPI_COM
MOV     DPL,#40H
CALL    SPI_DAT
MOV     DPL,#8AH
CALL    SPI_DAT
MOV     DPL,#00H
CALL    SPI_DAT
MOV     DPL,#00H
CALL    SPI_DAT
MOV     DPL,#29H
CALL    SPI_DAT
MOV     DPL,#19H
CALL    SPI_DAT
```



```
MOV    DPL,#A5H
CALL   SPI_DAT
MOV    DPL,#33H
CALL   SPI_DAT
```

```
MOV    DPL,#C1H
CALL   SPI_COM
MOV    DPL,#06H
CALL   SPI_DAT
```

```
MOV    DPL,#C2H
CALL   SPI_COM
MOV    DPL,#A7H
CALL   SPI_DAT
```

```
MOV    DPL,#C5H
CALL   SPI_COM
MOV    DPL,#18H
CALL   SPI_DAT
```

```
MOV    DPL,#E0H
CALL   SPI_COM
MOV    DPL,#F0H
CALL   SPI_DAT
MOV    DPL,#09H
CALL   SPI_DAT
MOV    DPL,#0BH
CALL   SPI_DAT
MOV    DPL,#06H
CALL   SPI_DAT
MOV    DPL,#04H
CALL   SPI_DAT
MOV    DPL,#15H
CALL   SPI_DAT
MOV    DPL,#2FH
CALL   SPI_DAT
MOV    DPL,#54H
CALL   SPI_DAT
MOV    DPL,#42H
CALL   SPI_DAT
MOV    DPL,#3CH
CALL   SPI_DAT
MOV    DPL,#17H
CALL   SPI_DAT
MOV    DPL,#14H
CALL   SPI_DAT
MOV    DPL,#18H
CALL   SPI_DAT
MOV    DPL,#1BH
CALL   SPI_DAT
```

```
MOV    DPL,#E1H
CALL   SPI_COM
MOV    DPL,#F0H
CALL   SPI_DAT
```



```
MOV    DPL,#09H
CALL   SPI_DAT
MOV    DPL,#0BH
CALL   SPI_DAT
MOV    DPL,#06H
CALL   SPI_DAT
MOV    DPL,#04H
CALL   SPI_DAT
MOV    DPL,#03H
CALL   SPI_DAT
MOV    DPL,#2DH
CALL   SPI_DAT
MOV    DPL,#43H
CALL   SPI_DAT
MOV    DPL,#42H
CALL   SPI_DAT
MOV    DPL,#3BH
CALL   SPI_DAT
MOV    DPL,#16H
CALL   SPI_DAT
MOV    DPL,#14H
CALL   SPI_DAT
MOV    DPL,#17H
CALL   SPI_DAT
MOV    DPL,#1BH
CALL   SPI_DAT
```

```
MOV    DPL,#F0H
CALL   SPI_COM
MOV    DPL,#3CH
CALL   SPI_DAT
```

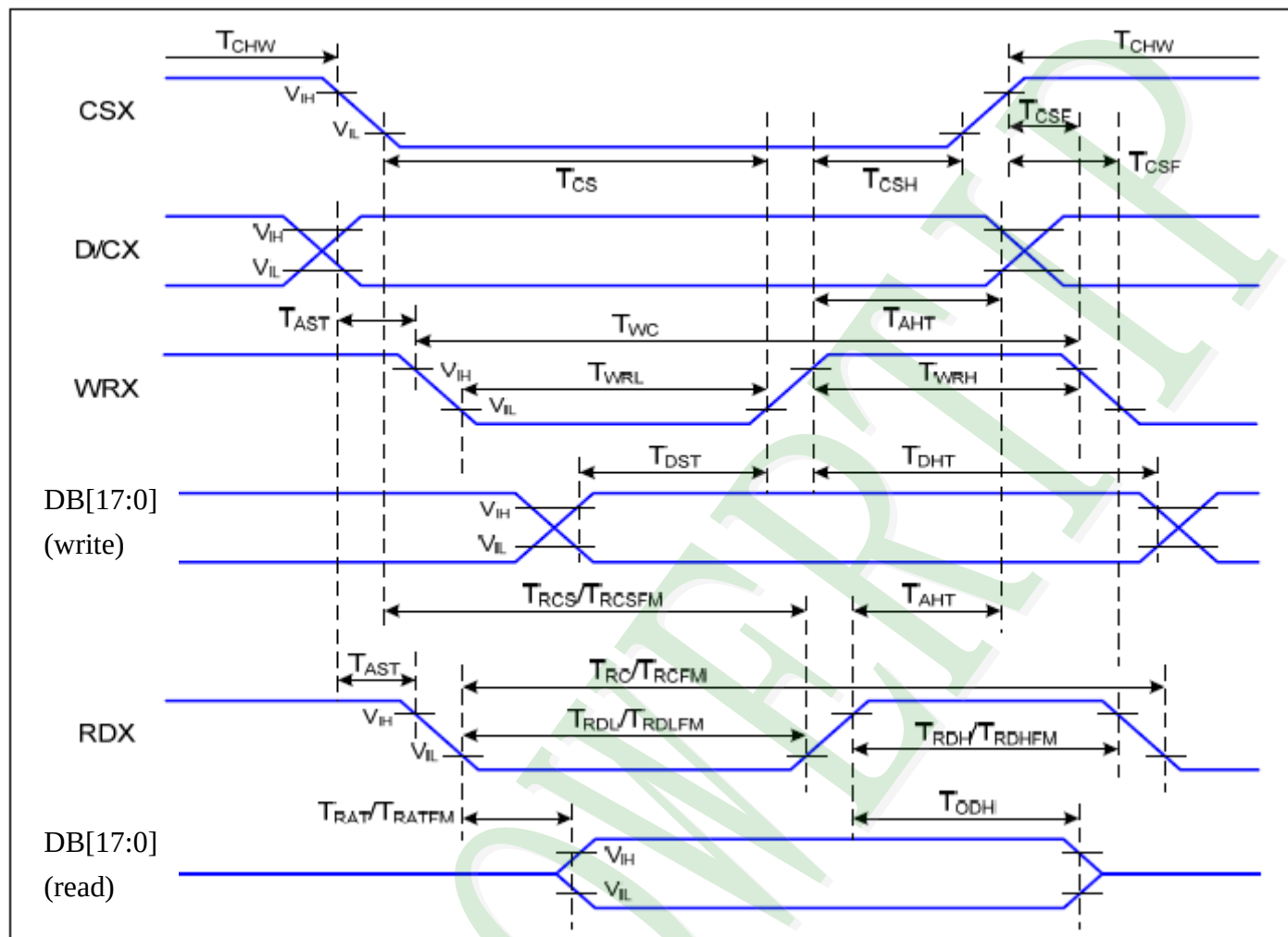
```
MOV    DPL,#F0H
CALL   SPI_COM
MOV    DPL,#69H
CALL   SPI_DAT
```

```
CALL   DELAY
CALL   DELAY
CALL   DELAY
CALL   DELAY
```

```
MOV    DPL,#29H
CALL   SPI_COM
```

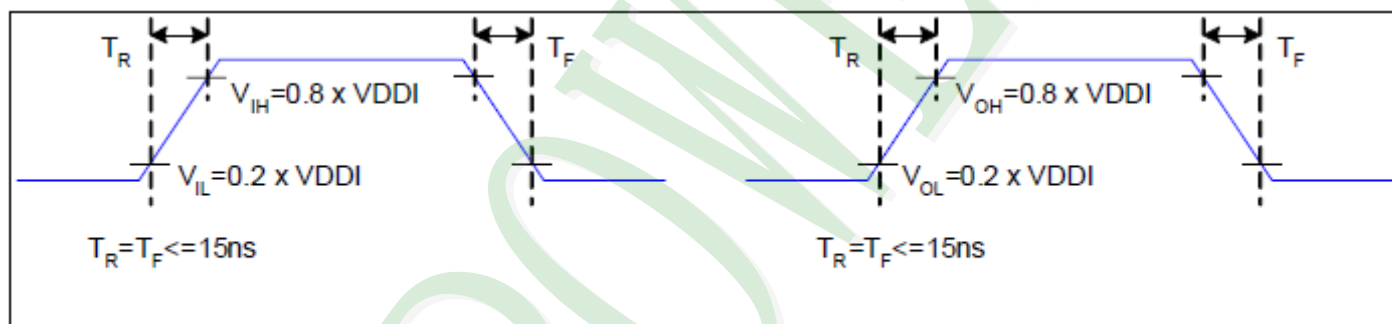
2.3 Timing Characteristics

8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

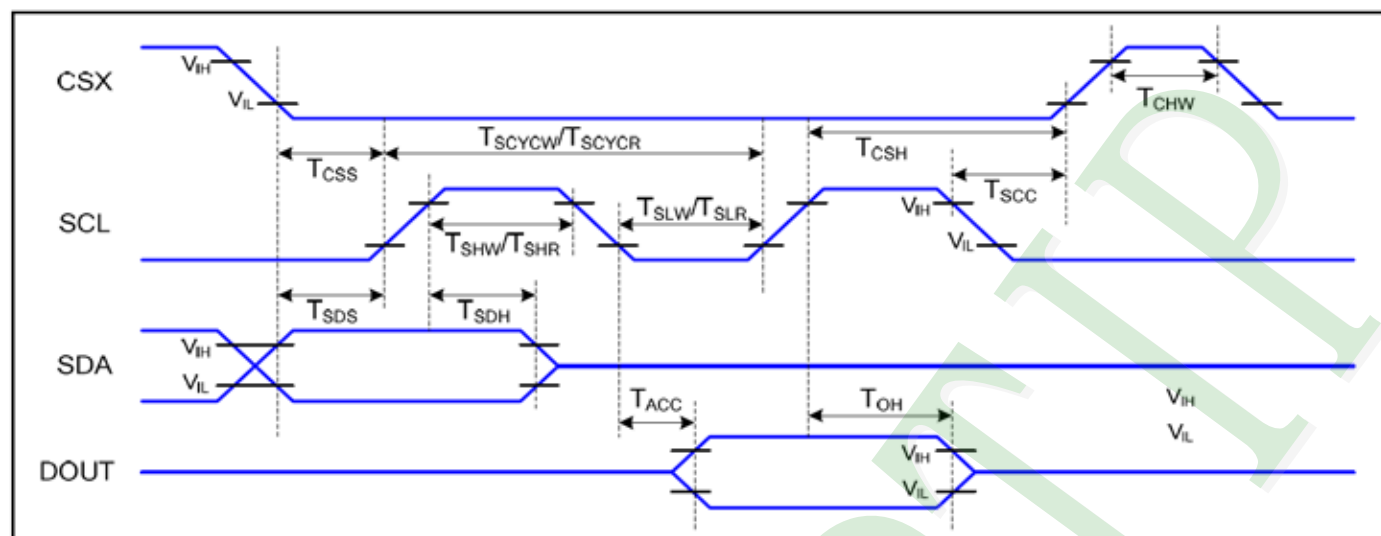
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
DB[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (T_R , T_F) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of V_{DDI} for Input signals.

3-SPI Serial Data Transfer Interface Characteristics:



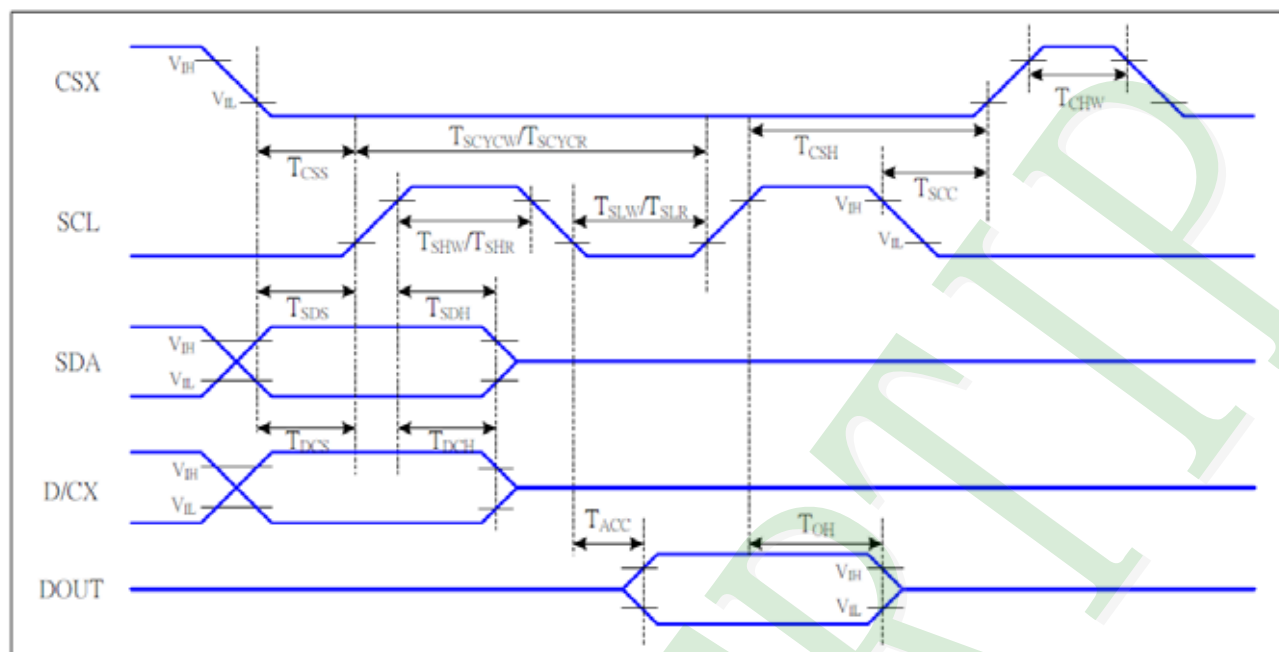
3-SPI Interface Timing Characteristics

$V_{DDI}=1.8V, V_{DDA}=2.8V, AGND=DGND=0V, T_a=25^{\circ}C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

4-SPI Serial Data Transfer Interface Characteristics:

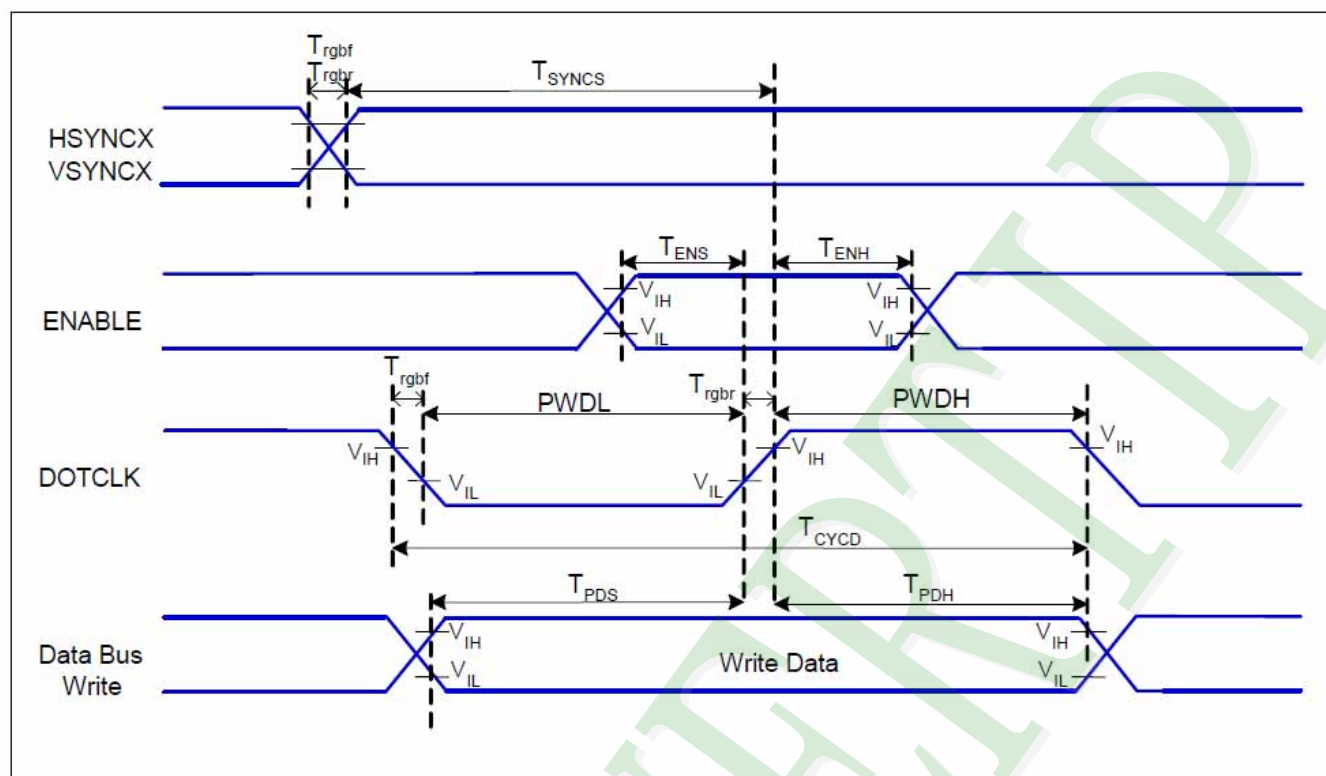


4-SPI Interface Timing Characteristics

$V_{DDI}=1.8V, V_{DDA}=2.8V, AGND=DGND=0V, T_a=25^{\circ}C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

RGB Interface Characteristics:



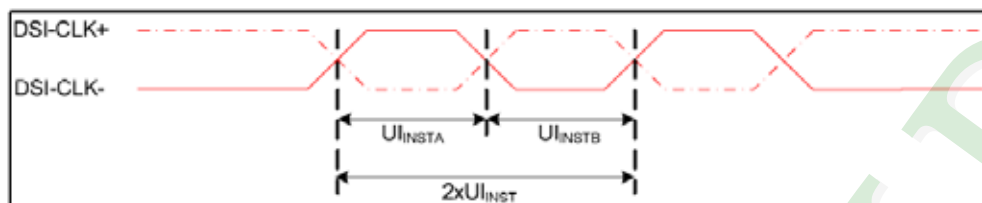
$V_{\text{DDI}}=1.8\text{V}$, $V_{\text{DDA}}=2.8\text{V}$, $\text{AGND}=\text{DGND}=0\text{V}$, $T_a=25^\circ\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCX}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

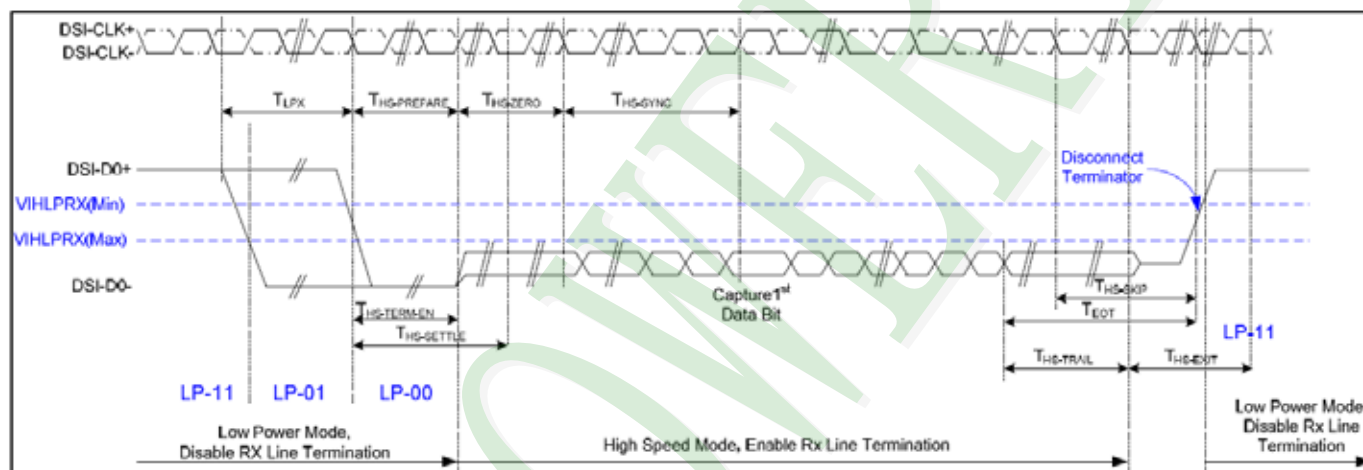
MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing



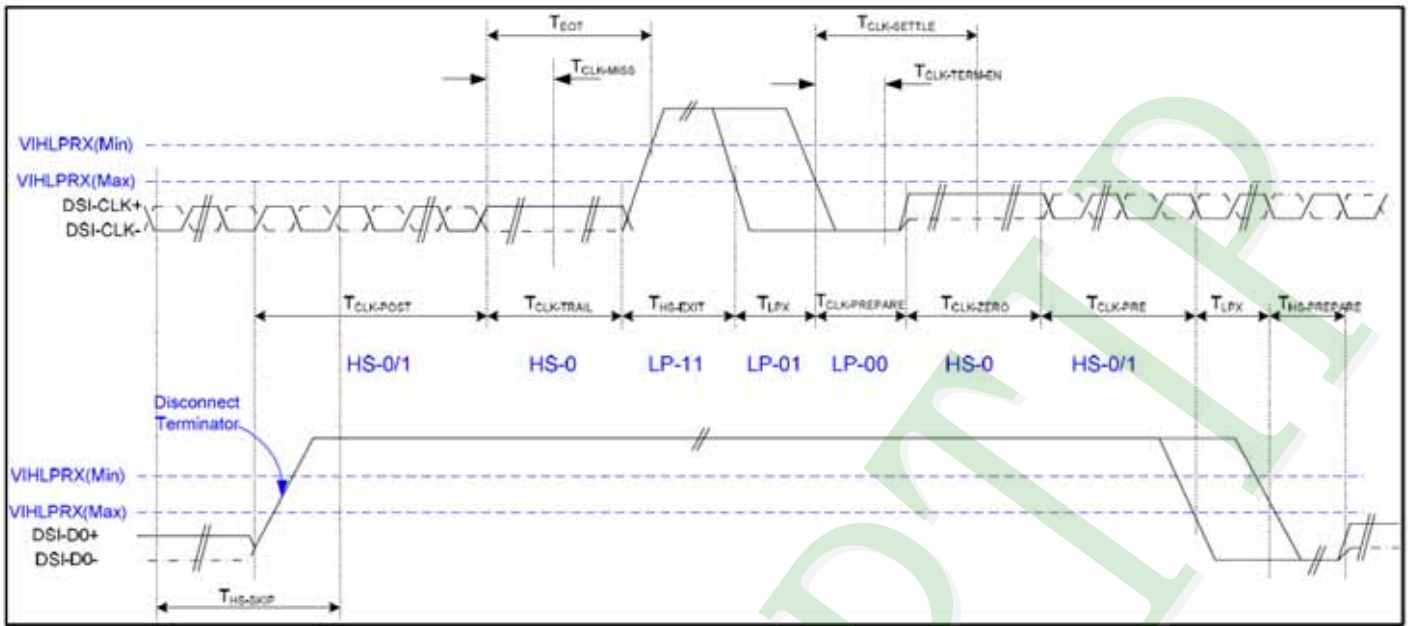
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI Instantaneous	4	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	2	12.5	ns	

High-Speed Data Transmission



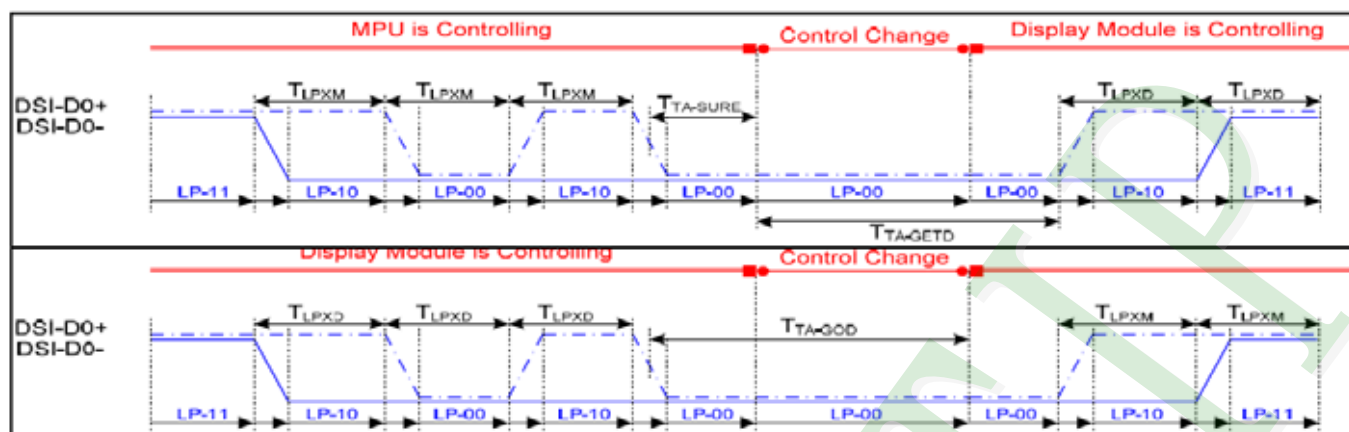
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated data lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

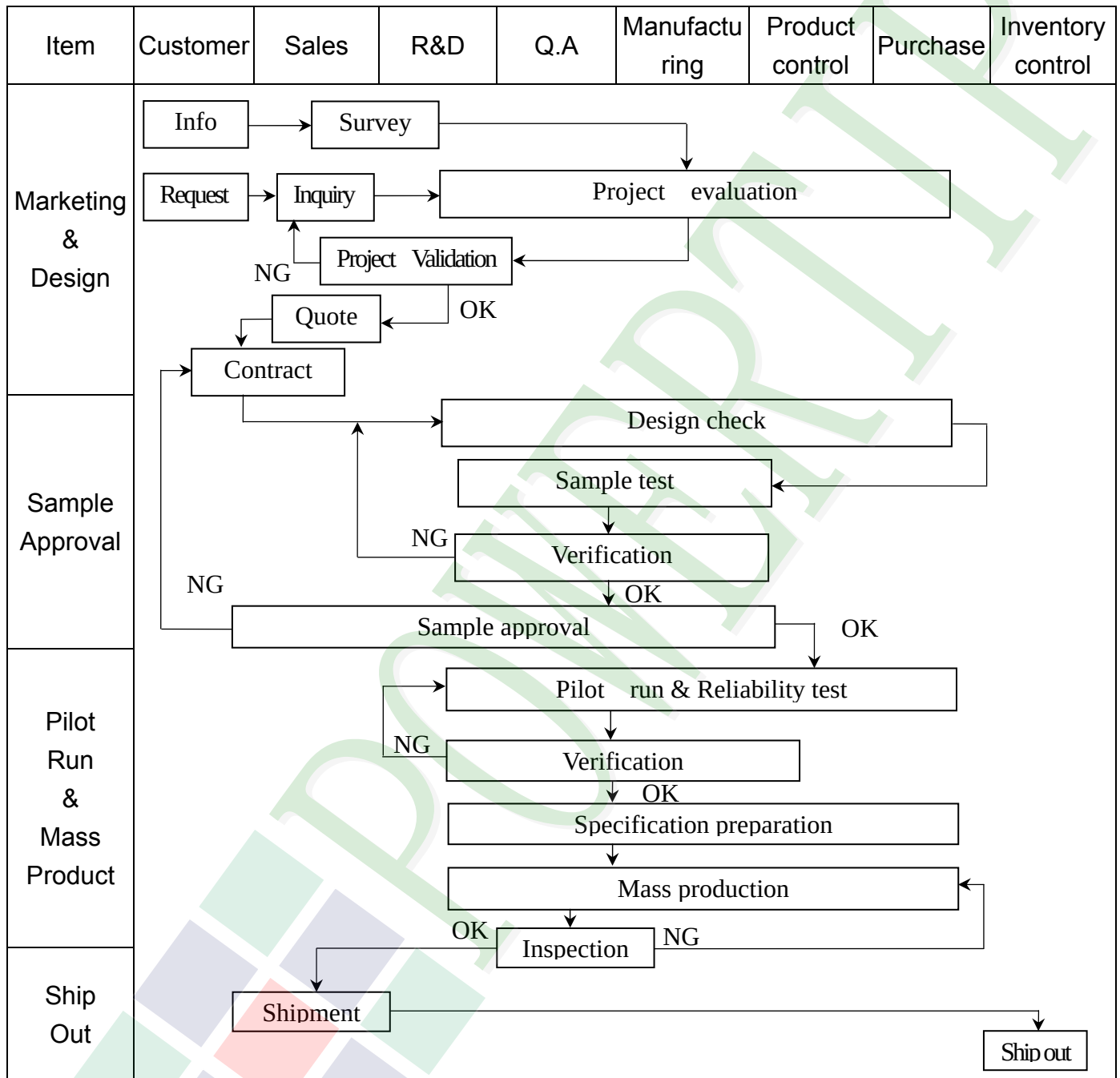
Bus Turnaround Procedure

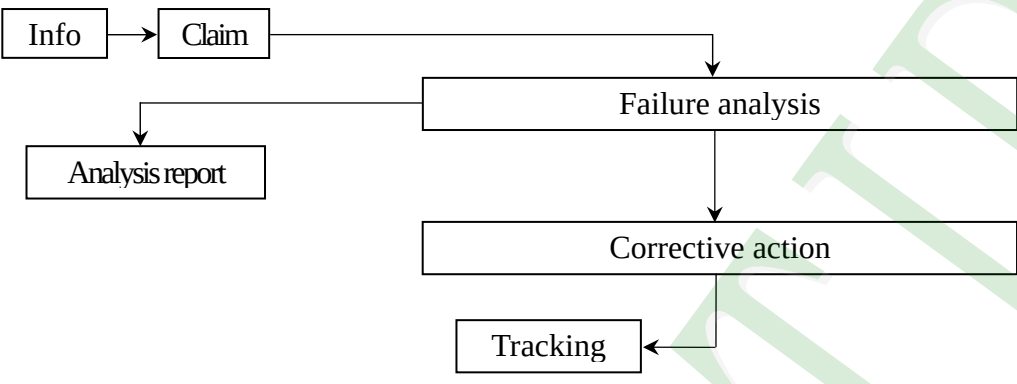


Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2 T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5 T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4 T_{LPX}$		ns

3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



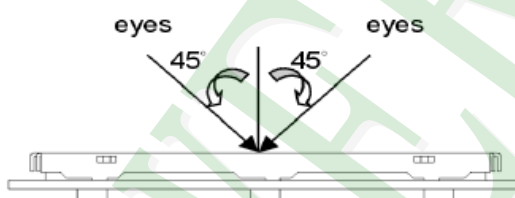
Item	Customer	Sales	R&D	Q.A	Manufacturing	Product control	Purchase	Inventory control
Sales Service	 <pre> graph TD Info[Info] --> Claim[Claim] Claim --> FA[Failure analysis] Claim --> AR[Analysis report] FA --> CA[Corrective action] CA --> Tracking[Tracking] </pre>							
Q.A Activity	1. ISO 9001 Maintenance Activities 3. Equipment calibration 5. Standardization Management				2. Process improvement proposal 4. Education And Training Activities			

3.2 Inspection Specification

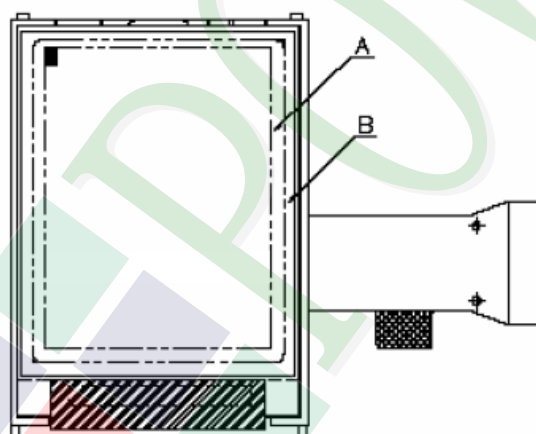
- ◆ **Scope** : The document shall be applied to TFT-LCD Module for less than 3.5" (Ver.B01).
- ◆ **Inspection Standard** : MIL-STD-105E Table Normal Inspection Single Sampling Level II.
- ◆ **Equipment** : Gauge 、 MIL-STD 、 Powertip Tester 、 Sample
- ◆ **Defect Level** : Major Defect AQL : 0.4 ; Minor Defect AQL : 1.5
- ◆ **OUT Going Defect Level** : Sampling.
- ◆ **Standard of the product appearance test** :

a. Manner of appearance test :

- (1). The test best be under 20W×2 fluorescent light , and distance of view must be at 30 cm.
- (2). The test direction is base on about around 45° of vertical line.



(3). Definition of area.



A area : viewing area

B area : Outside of viewing area

(4). Standard of inspection : (Unit : mm)

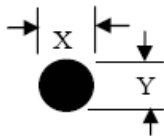
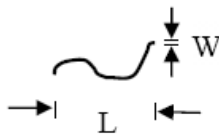
◆ Specification For TFT-LCD Module Less Than 3.5" :

(Ver.B01)

NO	Item	Criterion	Level												
01	Product condition	1. 1The part number is inconsistent with work order of production.	Major												
		1. 2 Mixed product types.	Major												
		1. 3 Assembled in inverse direction.	Major												
02	Quantity	2. 1The quantity is inconsistent with work order of production.	Major												
03	Outline dimension	3. 1 Product dimension and structure must conform to structure diagram.	Major												
04	Electrical Testing	4. 1 Missing line character and icon.	Major												
		4. 2 No function or no display.	Major												
		4. 3 Display malfunction.	Major												
		4. 4 LCD viewing angle defect.	Major												
		4. 5 Current consumption exceeds product specifications.	Major												
05	Dot defect (Bright dot 、Dark dot) On -display	<table><thead><tr><th colspan="2">Item</th><th>Acceptance (Q'ty)</th></tr></thead><tbody><tr><td rowspan="4">Dot Defect</td><td>Bright Dot</td><td>≤ 2</td></tr><tr><td>Dark Dot</td><td>≤ 3</td></tr><tr><td>Joint Dot</td><td>≤ 2</td></tr><tr><td>Total</td><td>≤ 3</td></tr></tbody></table> 5. 1 Inspection pattern : full white , full black , Red , Green and blue screens. 5. 2 It is defined as dot defect if defect area >1/2 dot. 5. 3 The distance between two dot defect ≥5 mm.	Item		Acceptance (Q'ty)	Dot Defect	Bright Dot	≤ 2	Dark Dot	≤ 3	Joint Dot	≤ 2	Total	≤ 3	Minor
Item		Acceptance (Q'ty)													
Dot Defect	Bright Dot	≤ 2													
	Dark Dot	≤ 3													
	Joint Dot	≤ 2													
	Total	≤ 3													

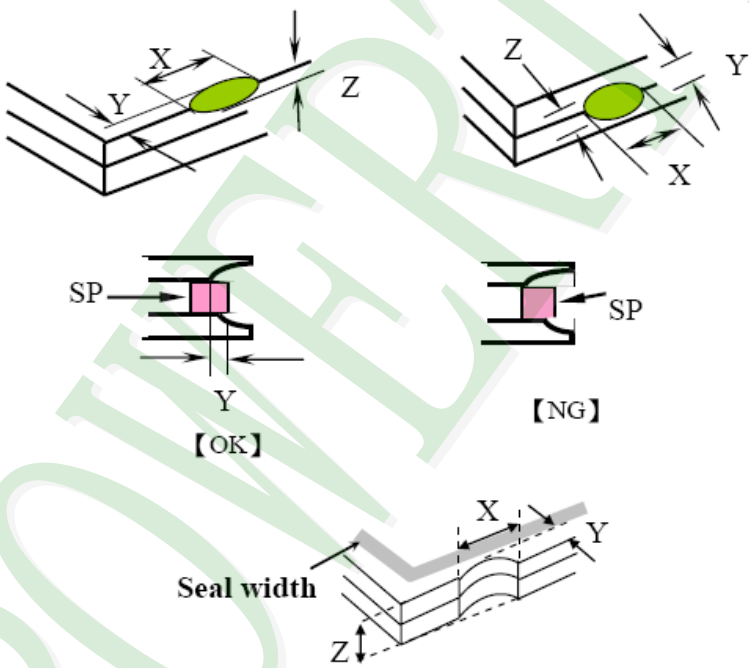
◆ Specification For TFT-LCD Module Less Than 3.5" :

(Ver.B01)

NO	Item	Criterion	Level																																							
06	Black or white dot、scratch、contamination Round type  $\Phi=(x+y) / 2$ Line type 	6. 1 Round type (Non-display or display) : <table> <tr> <th rowspan="2">Dimension (diameter : Φ)</th> <th colspan="2">Acceptance (Q'ty)</th> </tr> <tr> <th>A area</th> <th>B area</th> </tr> <tr> <td>$\Phi \leq 0.15$</td> <td>Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.30$</td> <td>2</td> </tr> <tr> <td>$\Phi > 0.30$</td> <td>0</td> </tr> <tr> <td>Total</td> <td>3</td> <td></td> </tr> </table> 6. 2 Line type(Non-display or display) : <table> <tr> <th colspan="2">Dimension</th> <th colspan="2">Acceptance (Q'ty)</th> </tr> <tr> <th>Length (L)</th> <th>Width (W)</th> <th>A area</th> <th>B area</th> </tr> <tr> <td>---</td> <td>$W \leq 0.03$</td> <td>Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td>$L \leq 5.0$</td> <td>$0.03 < W \leq 0.05$</td> <td>3</td> </tr> <tr> <td>---</td> <td>$W > 0.05$</td> <td>As round type</td> </tr> <tr> <td colspan="2">Total</td> <td>3</td> <td></td> </tr> </table>	Dimension (diameter : Φ)	Acceptance (Q'ty)		A area	B area	$\Phi \leq 0.15$	Ignore	Ignore	$0.15 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.30$	2	$\Phi > 0.30$	0	Total	3		Dimension		Acceptance (Q'ty)		Length (L)	Width (W)	A area	B area	---	$W \leq 0.03$	Ignore	Ignore	$L \leq 5.0$	$0.03 < W \leq 0.05$	3	---	$W > 0.05$	As round type	Total		3		Minor
Dimension (diameter : Φ)	Acceptance (Q'ty)																																									
	A area	B area																																								
$\Phi \leq 0.15$	Ignore	Ignore																																								
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Total	3																																									
Dimension		Acceptance (Q'ty)																																								
Length (L)	Width (W)	A area	B area																																							
---	$W \leq 0.03$	Ignore	Ignore																																							
$L \leq 5.0$	$0.03 < W \leq 0.05$	3																																								
---	$W > 0.05$	As round type																																								
Total		3																																								
07	Polarizer Bubble	<table> <tr> <th rowspan="2">Dimension (diameter : Φ)</th> <th colspan="2">Acceptance (Q'ty)</th> </tr> <tr> <th>A area</th> <th>B area</th> </tr> <tr> <td>$\Phi \leq 0.20$</td> <td>Ignore</td> <td rowspan="4">Ignore</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.50$</td> <td>3</td> </tr> <tr> <td>$\Phi > 0.50$</td> <td>0</td> </tr> <tr> <td>Total</td> <td>3</td> </tr> </table>	Dimension (diameter : Φ)	Acceptance (Q'ty)		A area	B area	$\Phi \leq 0.20$	Ignore	Ignore	$0.20 < \Phi \leq 0.50$	3	$\Phi > 0.50$	0	Total	3	Minor																									
Dimension (diameter : Φ)	Acceptance (Q'ty)																																									
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$\Phi > 0.50$	0																																									
Total	3																																									

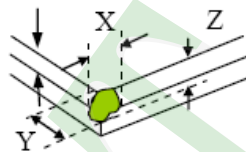
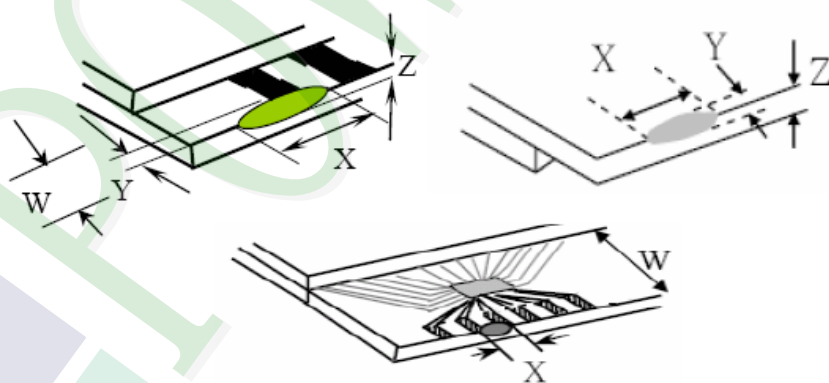
◆ Specification For TFT-LCD Module Less Than 3.5" :

(Ver.B01)

NO	Item	Criterion	Level									
08	The crack of glass	Symbols : X : The length of crack Z : The thickness of crack t : The thickness of glass Y : The width of crack. W : terminal length a : LCD side length 8.1 General glass chip : 8.1.1 Chip on panel surface and crack between panels:  <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$\leq a$</td><td>Crack can't enter viewing area</td><td>$\leq 1/2 t$</td></tr><tr><td>$\leq a$</td><td>Crack can't exceed the half of SP width.</td><td>$1/2 t < Z \leq 2 t$</td></tr></table>	X	Y	Z	$\leq a$	Crack can't enter viewing area	$\leq 1/2 t$	$\leq a$	Crack can't exceed the half of SP width.	$1/2 t < Z \leq 2 t$	Minor
		X	Y	Z								
$\leq a$	Crack can't enter viewing area	$\leq 1/2 t$										
$\leq a$	Crack can't exceed the half of SP width.	$1/2 t < Z \leq 2 t$										

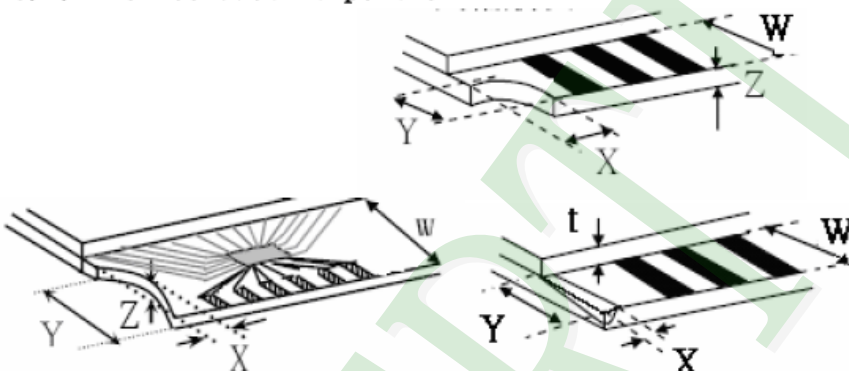
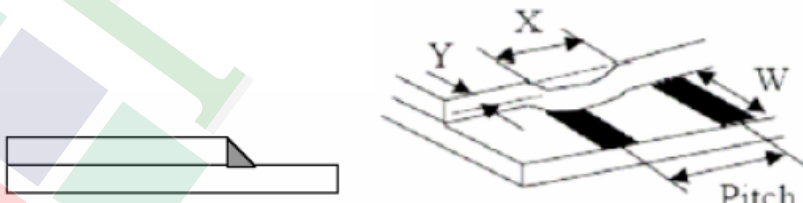
◆ Specification For TFT-LCD Module Less Than 3.5" :

(Ver.B01)

NO	Item	Criterion	Level												
08	The crack of glass	Symbols : X : The length of crack Z : The thickness of crack t : The thickness of glass Y : The width of crack. W : terminal length a : LCD side length	Minor												
		8.1.2 Corner crack :  <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$\leq 1/5 a$</td><td>Crack can't enter viewing area</td><td>$Z \leq 1/2 t$</td></tr><tr><td>$\leq 1/5 a$</td><td>Crack can't exceed the half of SP width.</td><td>$1/2 t < Z \leq 2 t$</td></tr></table>		X	Y	Z	$\leq 1/5 a$	Crack can't enter viewing area	$Z \leq 1/2 t$	$\leq 1/5 a$	Crack can't exceed the half of SP width.	$1/2 t < Z \leq 2 t$			
X	Y	Z													
$\leq 1/5 a$	Crack can't enter viewing area	$Z \leq 1/2 t$													
$\leq 1/5 a$	Crack can't exceed the half of SP width.	$1/2 t < Z \leq 2 t$													
		8.2 Protrusion over terminal : 8.2.1 Chip on electrode pad :  <table><tr><th></th><th>X</th><th>Y</th><th>Z</th></tr><tr><td>Front</td><td>$\leq a$</td><td>$\leq 1/2 W$</td><td>$\leq t$</td></tr><tr><td>Back</td><td>$\leq a$</td><td>$\leq W$</td><td>$\leq 1/2 t$</td></tr></table>		X	Y	Z	Front	$\leq a$	$\leq 1/2 W$	$\leq t$	Back	$\leq a$	$\leq W$	$\leq 1/2 t$	
	X	Y	Z												
Front	$\leq a$	$\leq 1/2 W$	$\leq t$												
Back	$\leq a$	$\leq W$	$\leq 1/2 t$												

◆ Specification For TFT-LCD Module Less Than 3.5" :

(Ver.B01)

NO	Item	Criterion	Level												
08	The crack of glass	Symbols : X : The length of crack Y : The width of crack. Z : The thickness of crack W : terminal length t : The thickness of glass a : LCD side length 8.2.2 Non-conductive portion :  <table> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td>$\leq 1/3 a$</td> <td>$\leq W$</td> <td>$\leq t$</td> </tr> </table> ☉ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. 8.2.3 Glass remain :  <table> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td>$\leq a$</td> <td>$\leq 1/3 W$</td> <td>$\leq t$</td> </tr> </table>	X	Y	Z	$\leq 1/3 a$	$\leq W$	$\leq t$	X	Y	Z	$\leq a$	$\leq 1/3 W$	$\leq t$	Minor
X	Y	Z													
$\leq 1/3 a$	$\leq W$	$\leq t$													
X	Y	Z													
$\leq a$	$\leq 1/3 W$	$\leq t$													

◆Specification For TFT-LCD Module Less Than 3.5" :
(Ver.B01)

NO	Item	Criterion	Level
09	Backlight elements	9. 1 Backlight can't work normally.	Major
		9. 2 Backlight doesn't light or color is wrong.	Major
		9. 3 Illumination source flickers when lit.	Major
10	General appearance	10. 1 Pin type 、 quantity 、 dimension must match type in structure diagram.	Major
		10. 2 No short circuits in components on PCB or FPC .	Major
		10. 3 Parts on PCB or FPC must be the same as on the production characteristic chart .There should be no wrong parts , missing parts or excess parts.	Major
		10. 4 Product packaging must the same as specified on packaging specification sheet.	Minor
		10. 5 The folding and peeled off in polarizer are not acceptable.	Minor
		10. 6 The PCB or FPC between B/L assembled distance(PCB or FPC) is ≤ 1.5 mm.	Minor

4. RELIABILITY TEST

4.1 Reliability Test Condition

(Ver.B01)

NO.	TEST ITEM	TEST CONDITION	
1	High Temperature Storage Test	Keep in +80 ±2℃ 96 hrs Surrounding temperature, then storage at normal condition 4hrs.	
2	Low Temperature Storage Test	Keep in -30 ±2℃ 96 hrs Surrounding temperature, then storage at normal condition 4hrs.	
3	High Temperature / High Humidity Storage Test	Keep in +60 ℃ / 90% R.H duration for 96 hrs Surrounding temperature, then storage at normal condition 4hrs. (Excluding the polarizer)	
4	Temperature Cycling Storage Test	-30℃ → +25℃ → +80℃ → +25℃ (30mins) (5mins) (30mins) (5mins) ←-----→ 10 Cycle Surrounding temperature, then storage at normal condition 4hrs.	
5	ESD Test	Air Discharge: Apply 2 KV with 5 times Discharge for each polarity +/-	Contact Discharge: Apply 250 V with 5 times discharge for each polarity +/-
		1. Temperature ambience : 15℃ 35℃ 2. Humidity relative : 30% 60% 3. Energy Storage Capacitance(Cs+Cd) : 150pF±10% 4. Discharge Resistance(Rd) : 330Ω±10% 5. Discharge, mode of operation : Single Discharge (time between successive discharges at least 1 sec) (Tolerance if the output voltage indication : ±5%)	
6	Vibration Test (Packaged)	1. Sine wave 10 55 Hz frequency (1 min/sweep) 2. The amplitude of vibration :1.5 mm 3. Each direction (X、 Y、 Z) duration for 2 Hrs	
7	Drop Test (Packaged)		
		Packing Weight (Kg)	Drop Height (cm)
		0 ~ 45.4	122
		45.4 ~ 90.8	76
		90.8 ~ 454	61
Over 454	46		
		Drop Direction :※1 corner / 3 edges / 6 sides each 1time	

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

- 5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

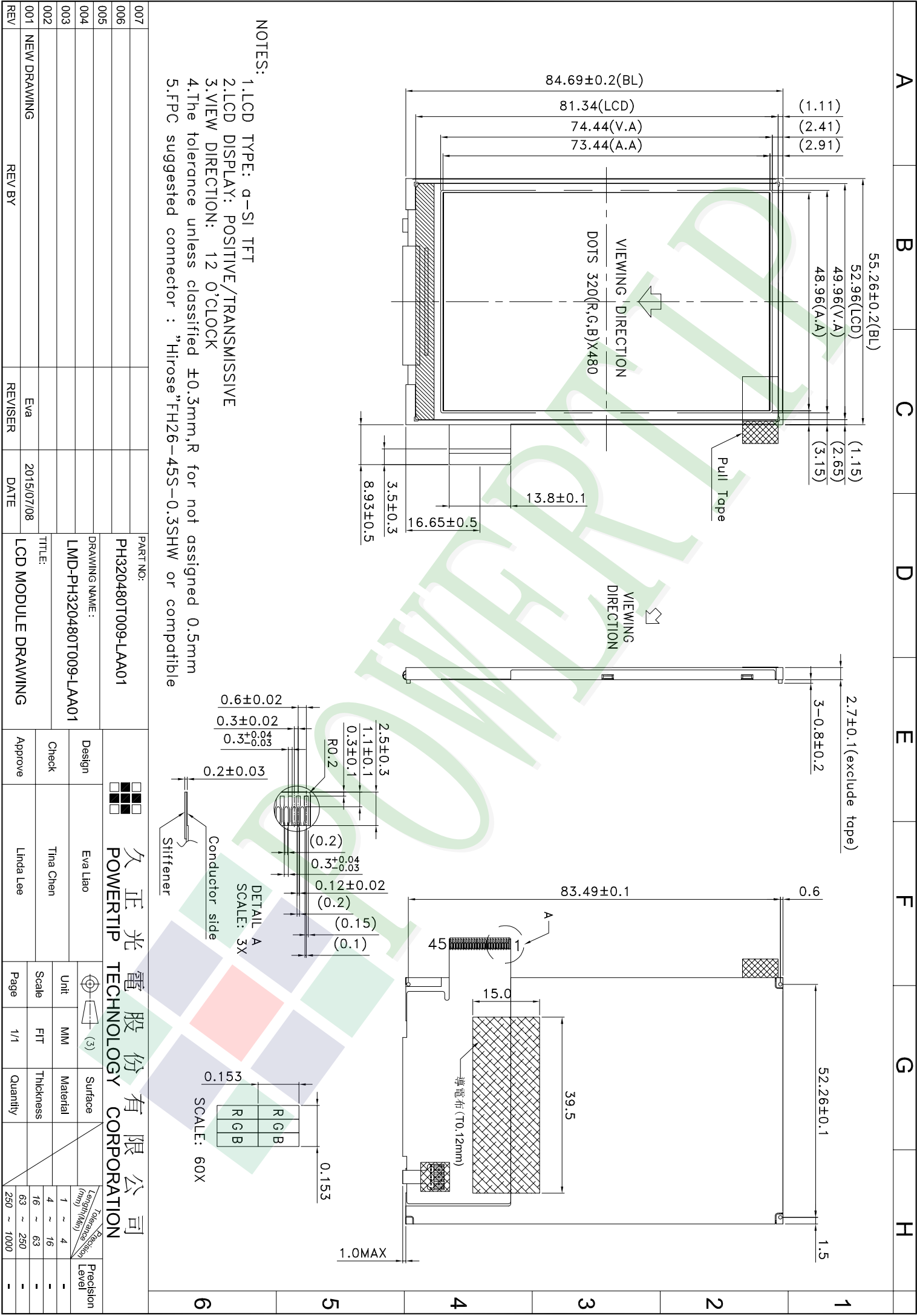
- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands , this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is $320 \pm 10^{\circ}\text{C}$ and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM .

5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush , shake , or jolt the module.

5.4 TERMS OF WARRANTY

- 5.4.1 Applicable warrant period
The period is within thirteen months since the date of shipping out under normal using and storage conditions.
- 5.4.2 Unaccepted responsibility
This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment , we cannot take responsibility if the product is used in nuclear power control equipment , aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.



Ver.001

Documents NO. PKG-PH320480T009-LAA01

LCM包裝規格書

LCM Packaging Specifications

Approve	Check	Contact
Linda	Tina	Eva

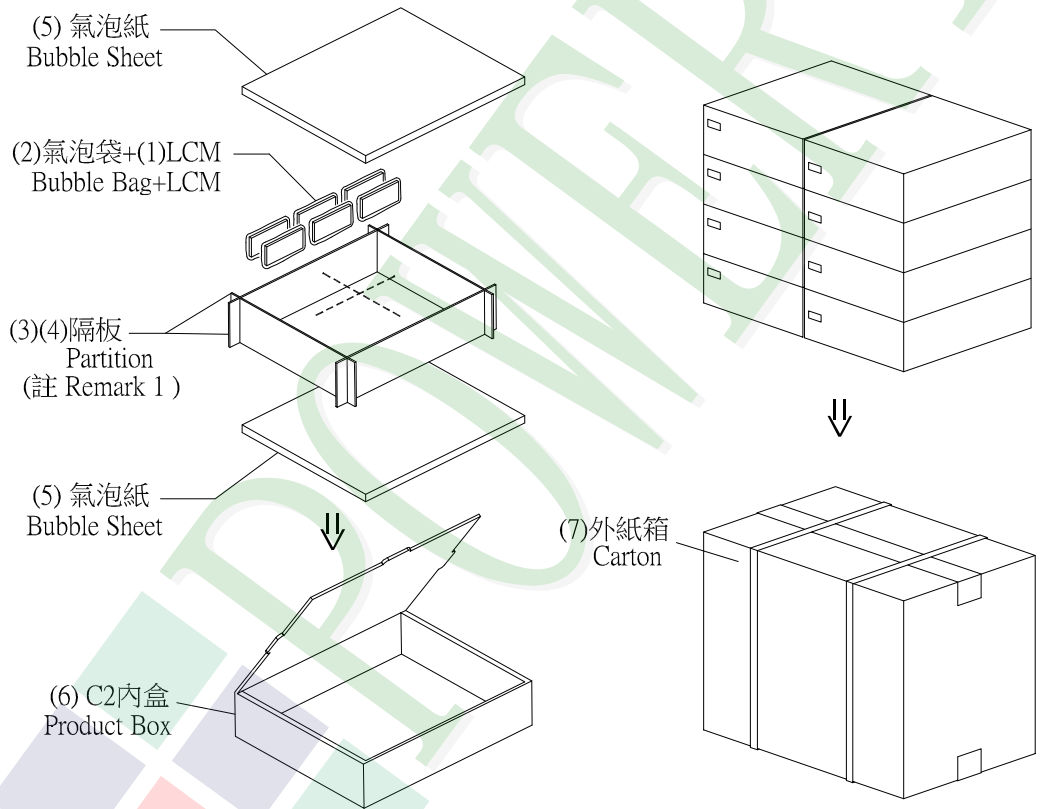
1.包裝材料規格表 (Packaging Material) : (per carton)

No.	Item	Model	Dimensions (mm)	1Pcs Weight	Quantity	Total Weight
1	成品 (1)LCM	PH320480T009-LAA01	55.26 X 84.69	0.0203	288	5.8464
2	氣泡袋(2)Bubble Bag	BAG100080BWABA	100 X 80	0.0012	288	0.3456
3	A2-1隔板(3)A2-1 Partition	BX29500072BZBA	295 X 72 X 3.0	0.0109	104	1.1336
4	B2-1隔板(4)B2-1 Partition	BX24500072BZBA	245 X 72 X 3.0	0.0094	32	0.3008
5	氣泡紙(5)Bubble Sheet	BAG280240BWABA	280 X 240	0.006	16	0.096
6	C2內盒(6)Product Box	BX31025580AABA	310 X 255 X 86	0.16	8	1.28
7	外紙箱(7)Carton	BX52732536CCBA	527 X 325 X 360	0.83	1	0.83
8						
9						

2.一 整箱總重量 (Total LCD Weight in carton) : 9.83 Kg±10%

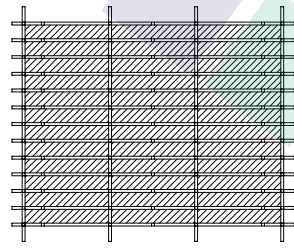
3.單箱數量規格表 (Packaging Specifications and Quantity) :

(1)Quantity Of Spacer : A2-1隔板 X 13 , B2-1隔板 X 4
(2)Total LCM quantity in carton : quantity per box 36 x no of boxes 8 = 288



特 記 事 項 (REMARK)

1. LCM排放示意圖(前後間隔不放置):
1. LCM placed as figure showing:
(First and last slot should be empty)



模組(LCM) X 1pcs.