

PH3330L

N-channel TrenchMOS logic level FET

Rev. 01 — 1 February 2006

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Optimized for use in DC-to-DC converters
- Very low switching and conduction losses
- Logic level compatible
- Lead-free package

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies
- Voltage regulators
- Notebook computers

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 100 \text{ A}$
- $R_{DS(on)} \leq 3.3 \text{ m}\Omega$
- $Q_{GD} = 6.9 \text{ nC (typ)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	 SOT669 (LFPAK)	 mbb076
4	gate (G)		
mb	mounting base; connected to drain (D)		

3. Ordering information

Table 2: Ordering information

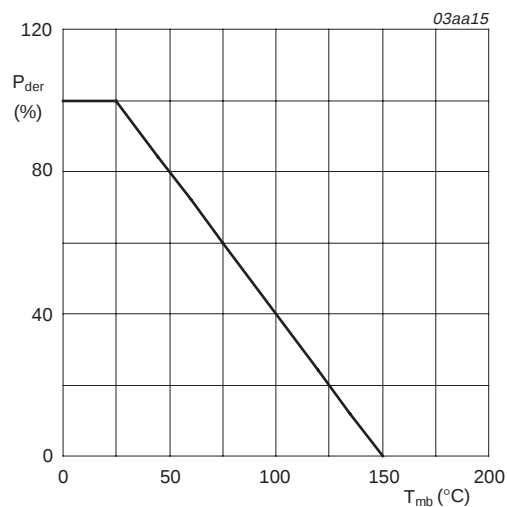
Type number	Package		
	Name	Description	Version
PH3330L	LFPAK	plastic single-ended surface mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

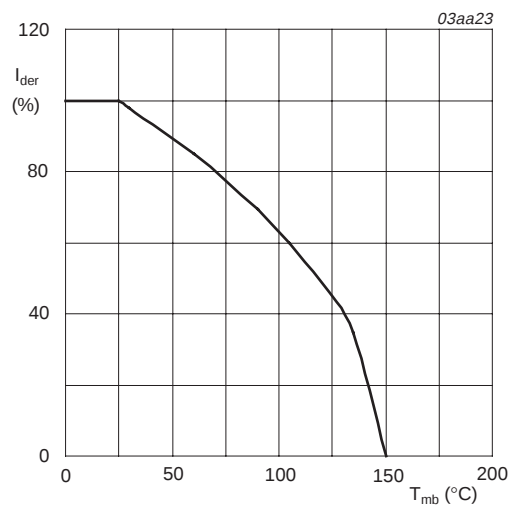
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_J \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	100	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	54.2	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_J	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 70\text{ A}$; $t_p = 0.15\text{ ms}$; $V_{DS} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_J = 25\text{ °C}$	-	245	mJ



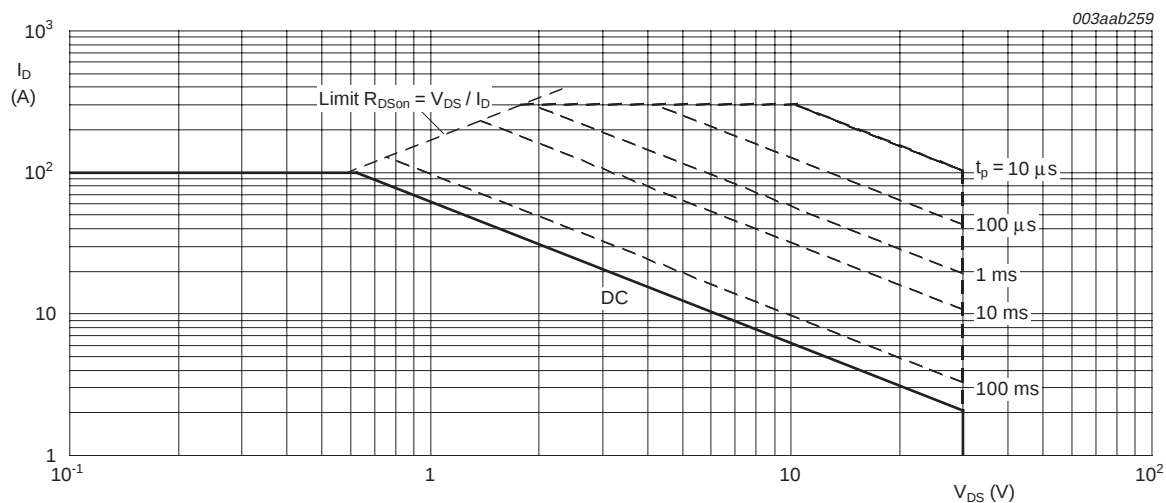
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



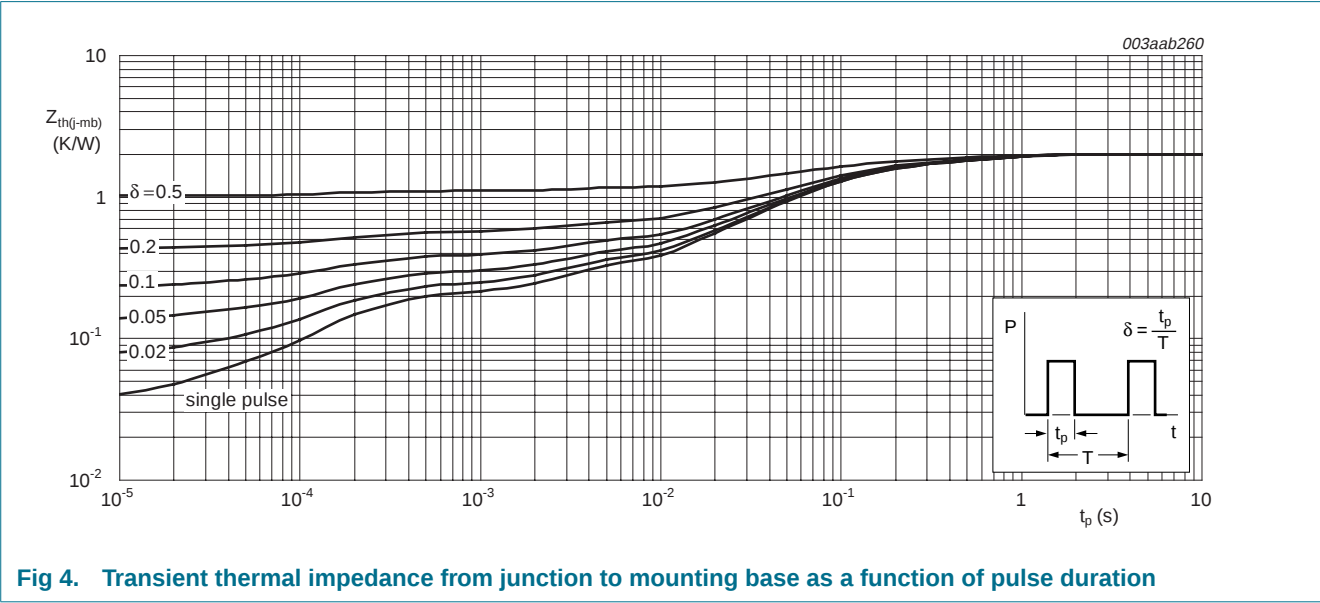
$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W



6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	30	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	1.3	1.7	2.15	V
		$T_j = 150\text{ }^{\circ}\text{C}$	0.8	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^{\circ}\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 16\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
R_G	gate resistance	$f = 1\text{ MHz}$	-	0.7	-	Ω
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	2.3	3.3	m Ω
		$T_j = 150\text{ }^{\circ}\text{C}$	-	4.1	6	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; see Figure 6 and 8	-	3.4	4.5	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; $V_{GS} = 4.5\text{ V}$; see Figure 11 and 12	-	30.5	-	nC
Q_{GS}	gate-source charge		-	15.4	-	nC
Q_{GS1}	pre- $V_{GS(th)}$ gate-source charge		-	7.7	-	nC
Q_{GS2}	post- $V_{GS(th)}$ gate-source charge		-	7.7	-	nC
Q_{GD}	gate-drain charge		-	6.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	3.4	-	V
$Q_{G(tot)}$	total gate charge	$I_D = 0\text{ A}$; $V_{DS} = 0\text{ V}$; $V_{GS} = 4.5\text{ V}$	-	28.5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $f = 1\text{ MHz}$; see Figure 14	-	4840	-	pF
C_{oss}	output capacitance		-	960	-	pF
C_{rss}	reverse transfer capacitance		-	410	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$	-	5380	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}$; $R_L = 0.5\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 5.6\text{ }\Omega$	-	41	-	ns
t_r	rise time		-	75	-	ns
$t_{d(off)}$	turn-off delay time		-	52	-	ns
t_f	fall time		-	27	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 13	-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	52	-	ns
Q_r	recovered charge		-	23	-	nC

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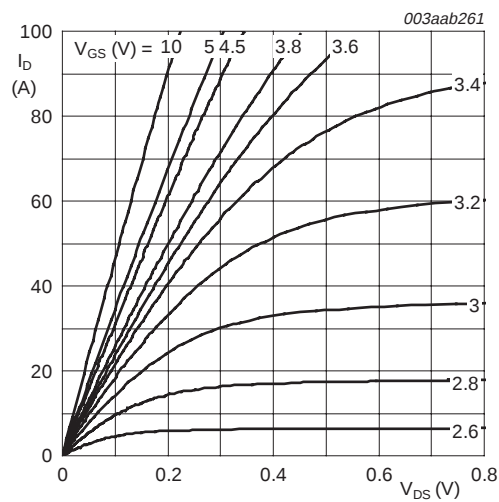


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

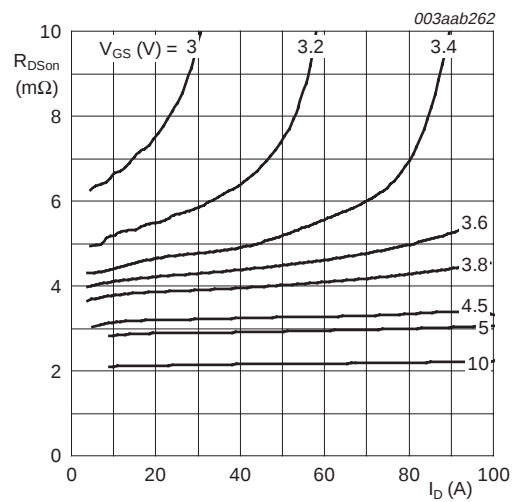


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

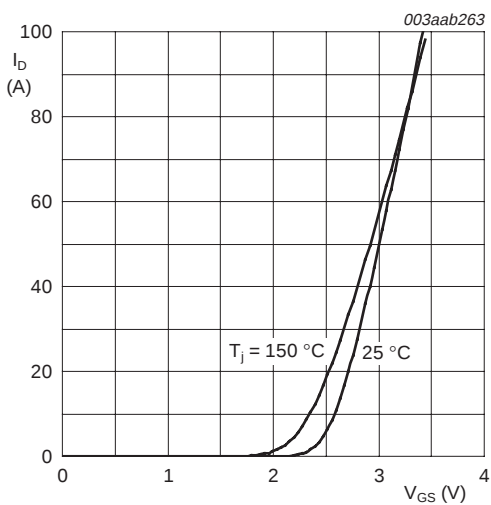


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

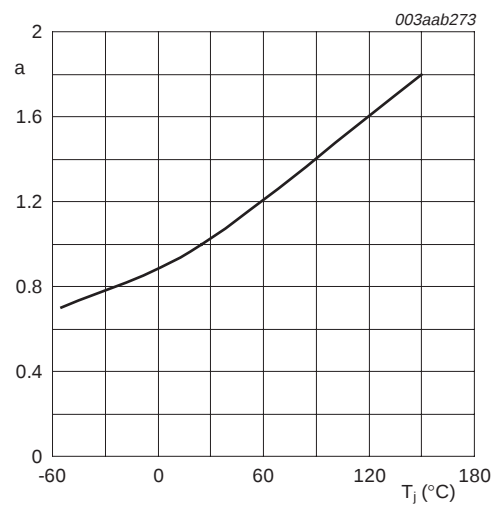
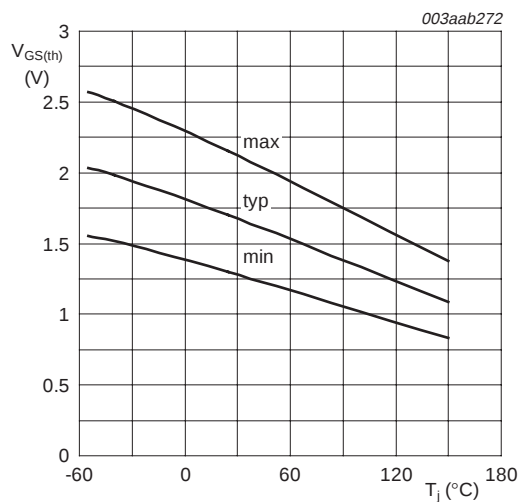
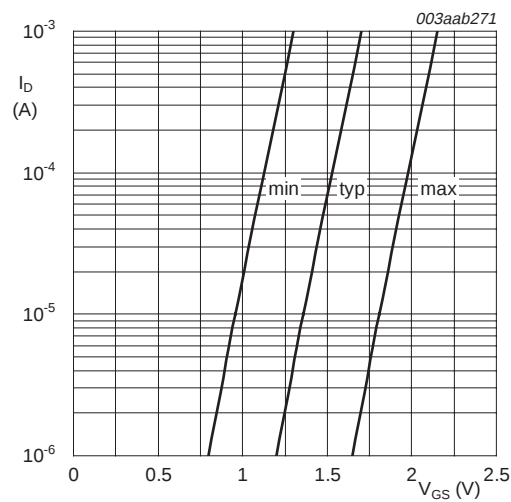


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



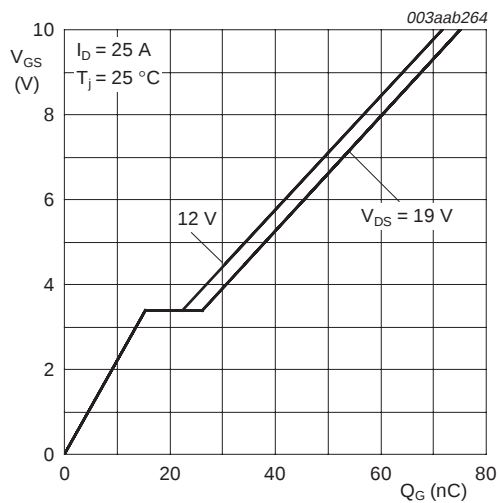
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



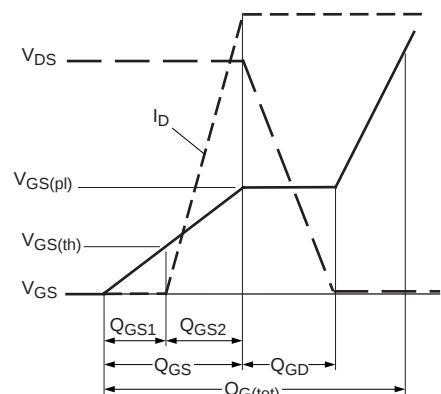
$T_j = 25\text{ °C}$; $V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



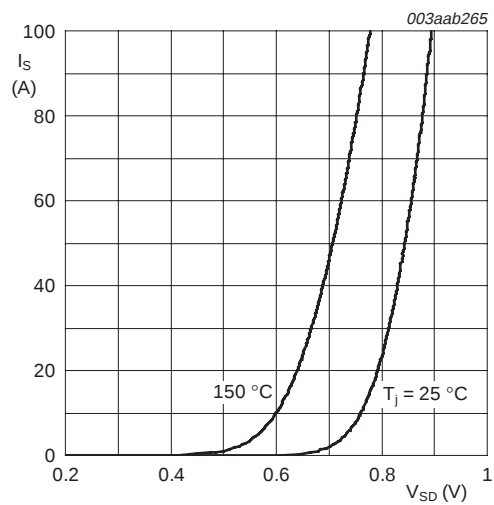
$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$ and 19 V

Fig 11. Gate-source voltage as a function of gate charge; typical values



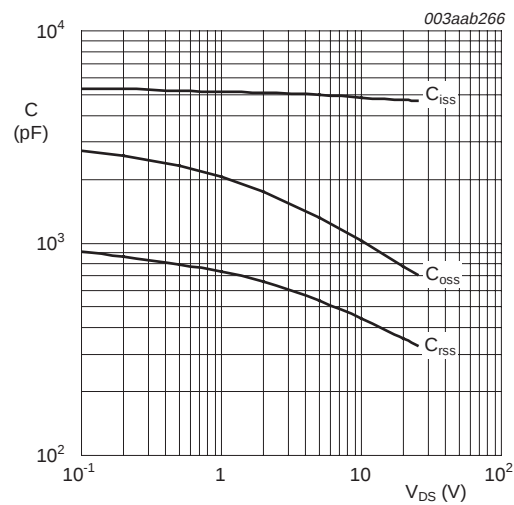
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Fig 12. Gate charge waveform definitions



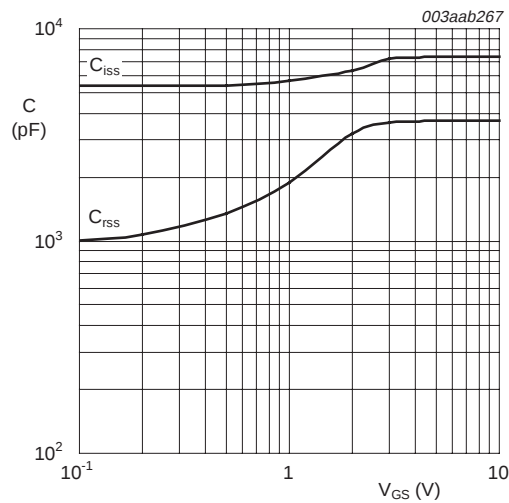
$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

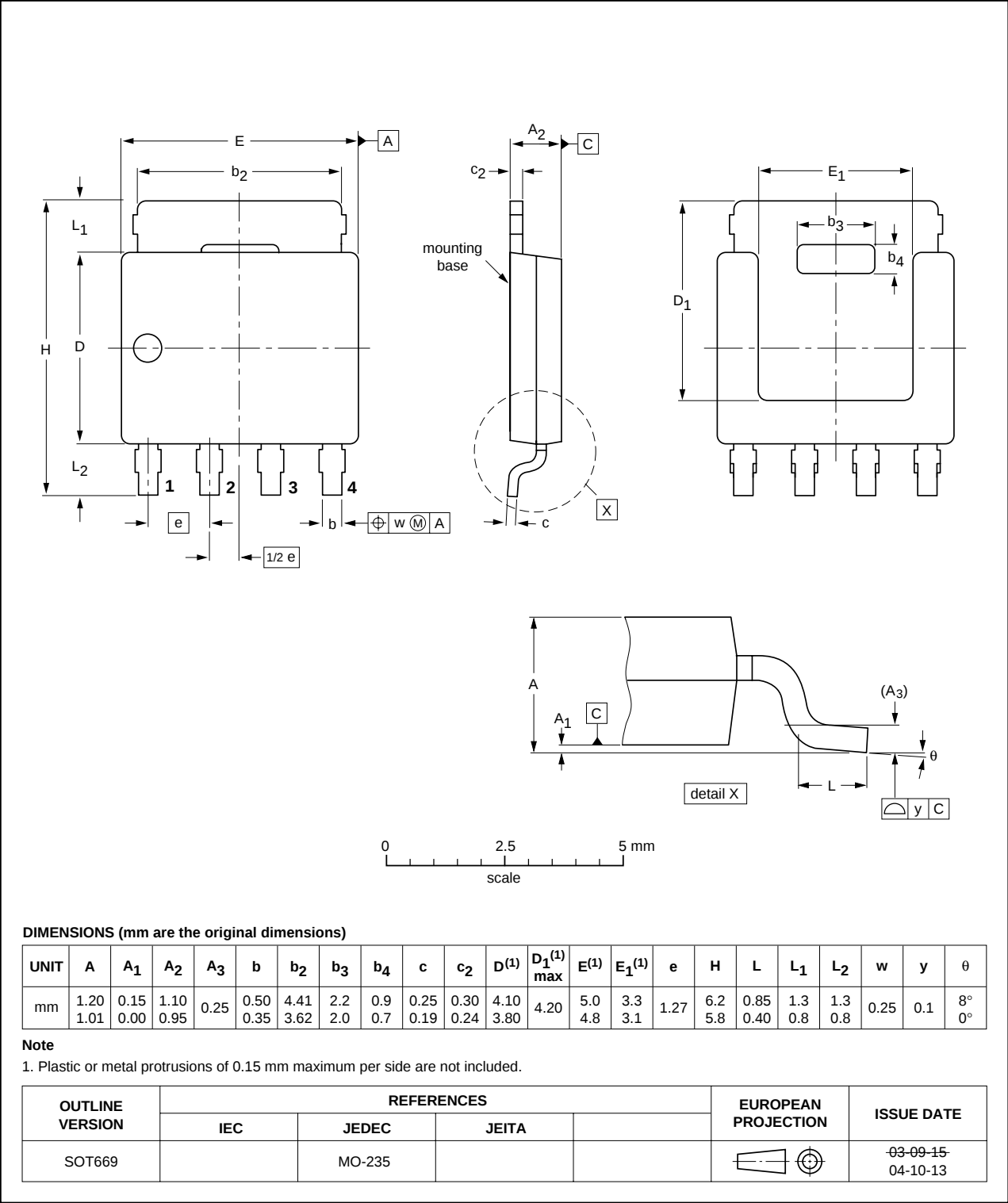


Fig 16. Package outline SOT669 (LPAK)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH3330L_1	20060201	Product data sheet	-	-	-

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Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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