

PH3830L

N-channel TrenchMOS™ logic level FET

Rev. 03 — 2 March 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Logic level gate drive
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

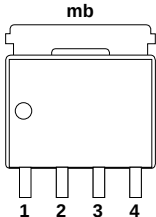
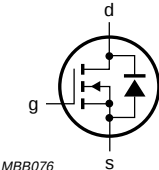
- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 98 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DS(on)} \leq 3.8 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	 Top view <i>MBL286</i>	 <i>MBB076</i>
4	gate (g)		
mb	mounting base; connected to drain (d)		
SOT669 (LFAK)			

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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PH3830L	LFPAK	Plastic single-ended surface mounted package; 4 leads	SOT669

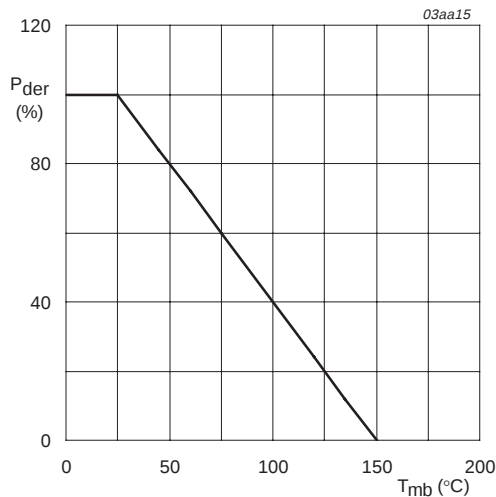
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

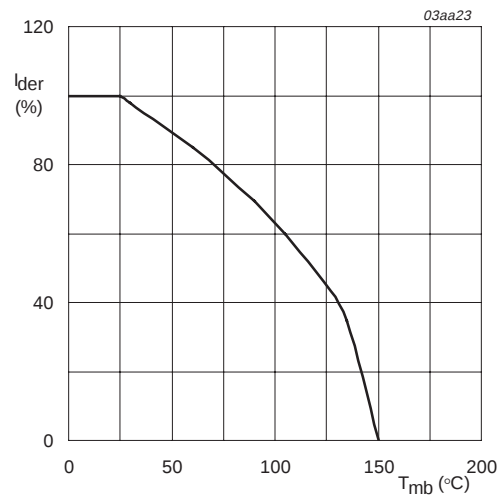
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	98	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	62	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	290	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 70.7\text{ A}$; $t_p = 0.1\text{ ms}$; $V_{DD} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	250	mJ

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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

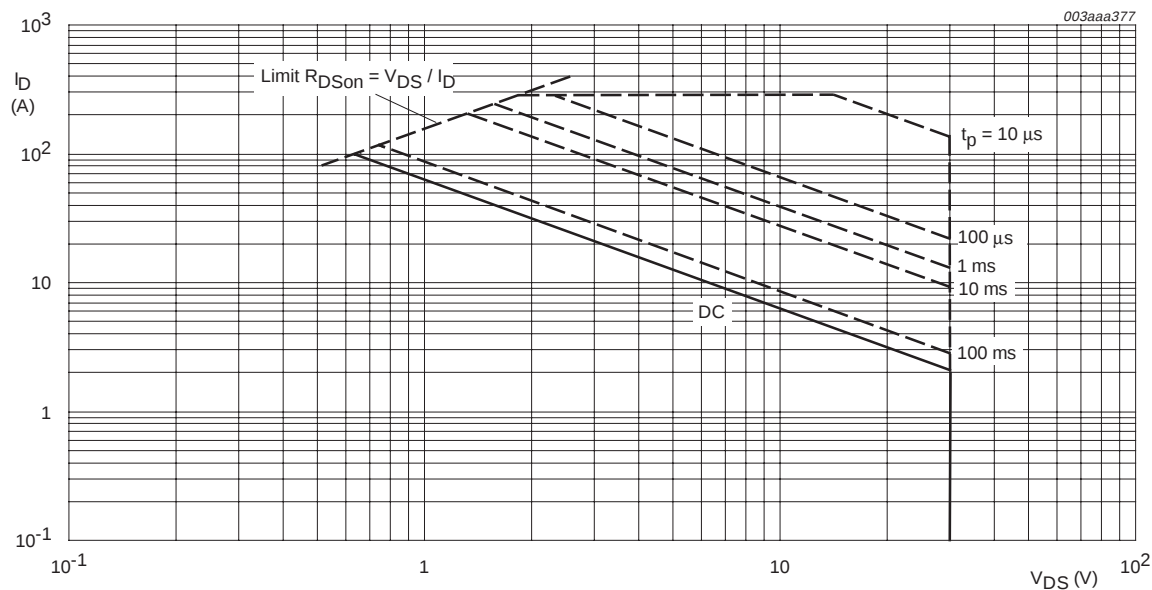
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 10 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is single pulse; $V_{GS} = 10 \text{ V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

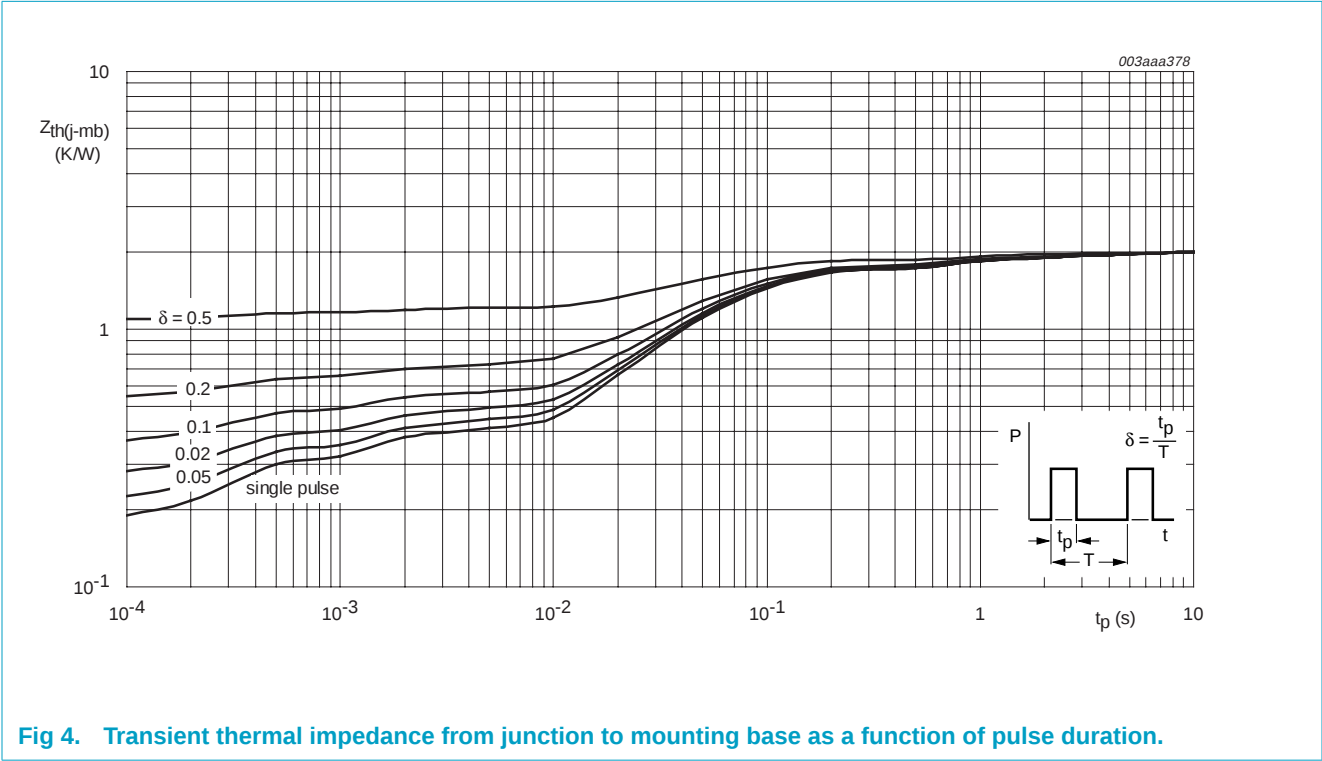
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5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance



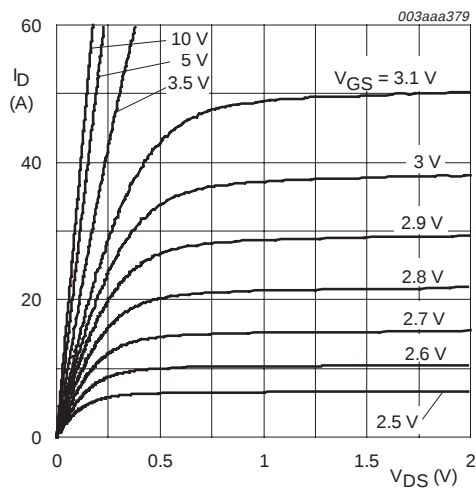
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6. Characteristics

Table 5: Characteristics

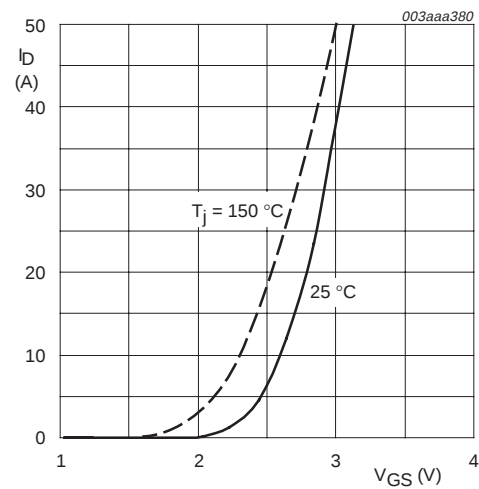
 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	1	1.5	2	V
		T _j = 150 °C	0.65	-	-	V
I _{DSS}	drain-source leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C	-	0.06	1	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	20	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; Figure 7 and 8				
		T _j = 25 °C	-	3.2	3.8	mΩ
		T _j = 150 °C	-	5.4	6.5	mΩ
		V _{GS} = 5 V; I _D = 25 A; Figure 7	-	4	4.9	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 20 A; V _{DD} = 10 V; V _{GS} = 5 V; Figure 13	-	33	-	nC
Q _{gs}	gate-source charge		-	11	-	nC
Q _{gd}	gate-drain (Miller) charge		-	11	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; Figure 11	-	3190	-	pF
C _{oss}	output capacitance		-	1050	-	pF
C _{rss}	reverse transfer capacitance		-	457	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 15 V; I _D = 20 A; V _{GS} = 4.5 V; R _G = 4.7 Ω	-	30	-	ns
t _r	rise time		-	88	-	ns
t _{d(off)}	turn-off delay time		-	58	-	ns
t _f	fall time		-	57	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 12	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = −100 A/μs; V _{GS} = 0 V	-	42	-	ns



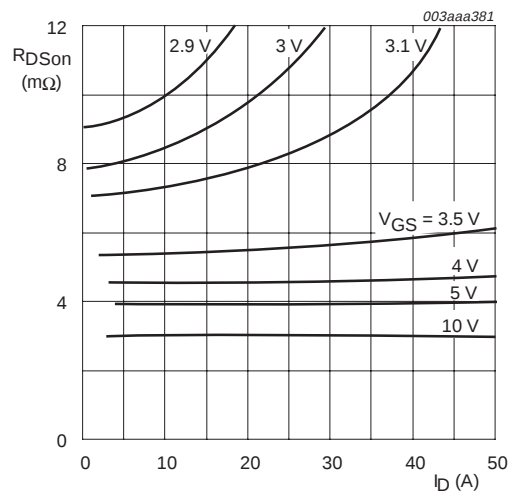
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



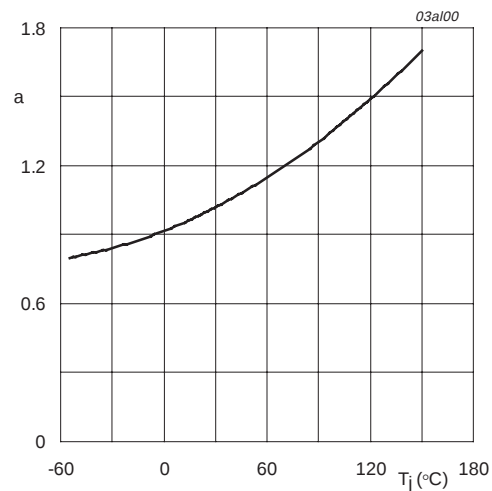
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25^\circ\text{C}$

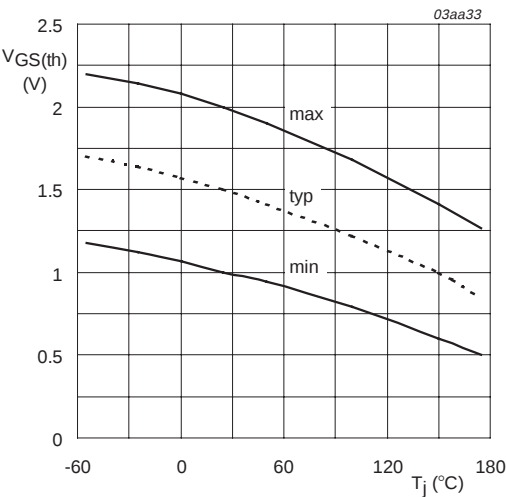
Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

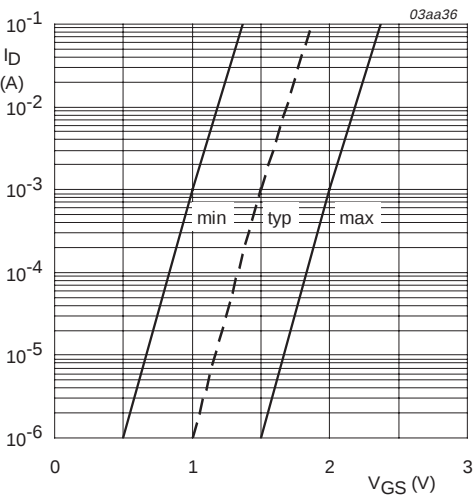
Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.

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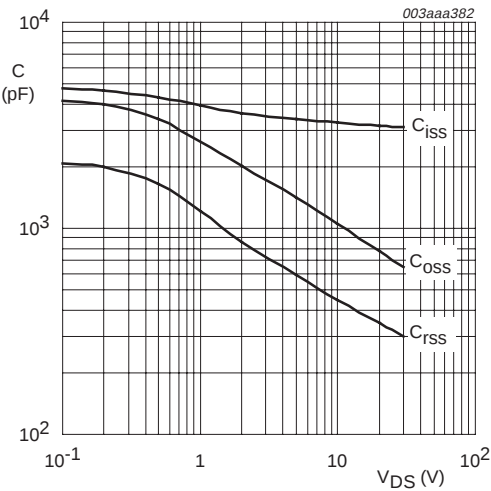
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25\text{ }^{\circ}C$; $V_{DS} = 5\text{ V}$

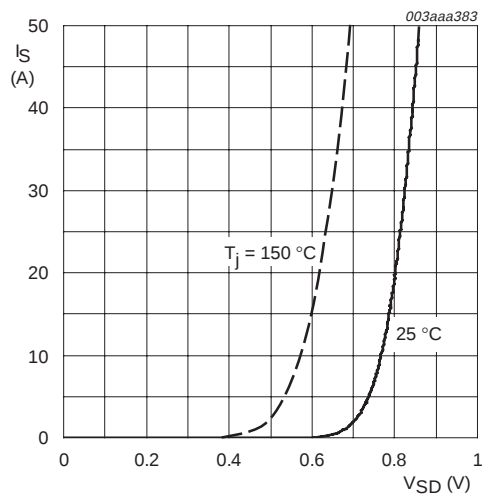
Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

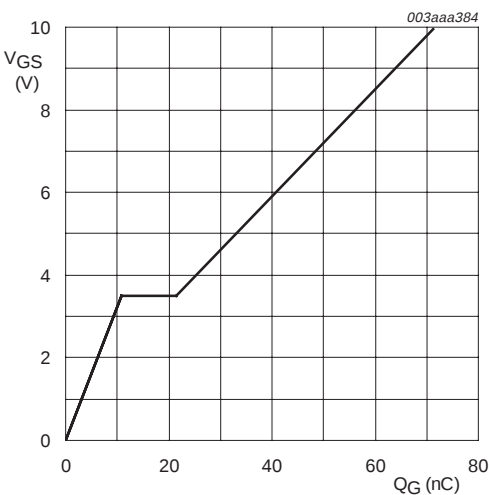
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

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T_J = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



I_D = 20 A; V_{DD} = 10 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version LFAK); 4 leads

SOT669

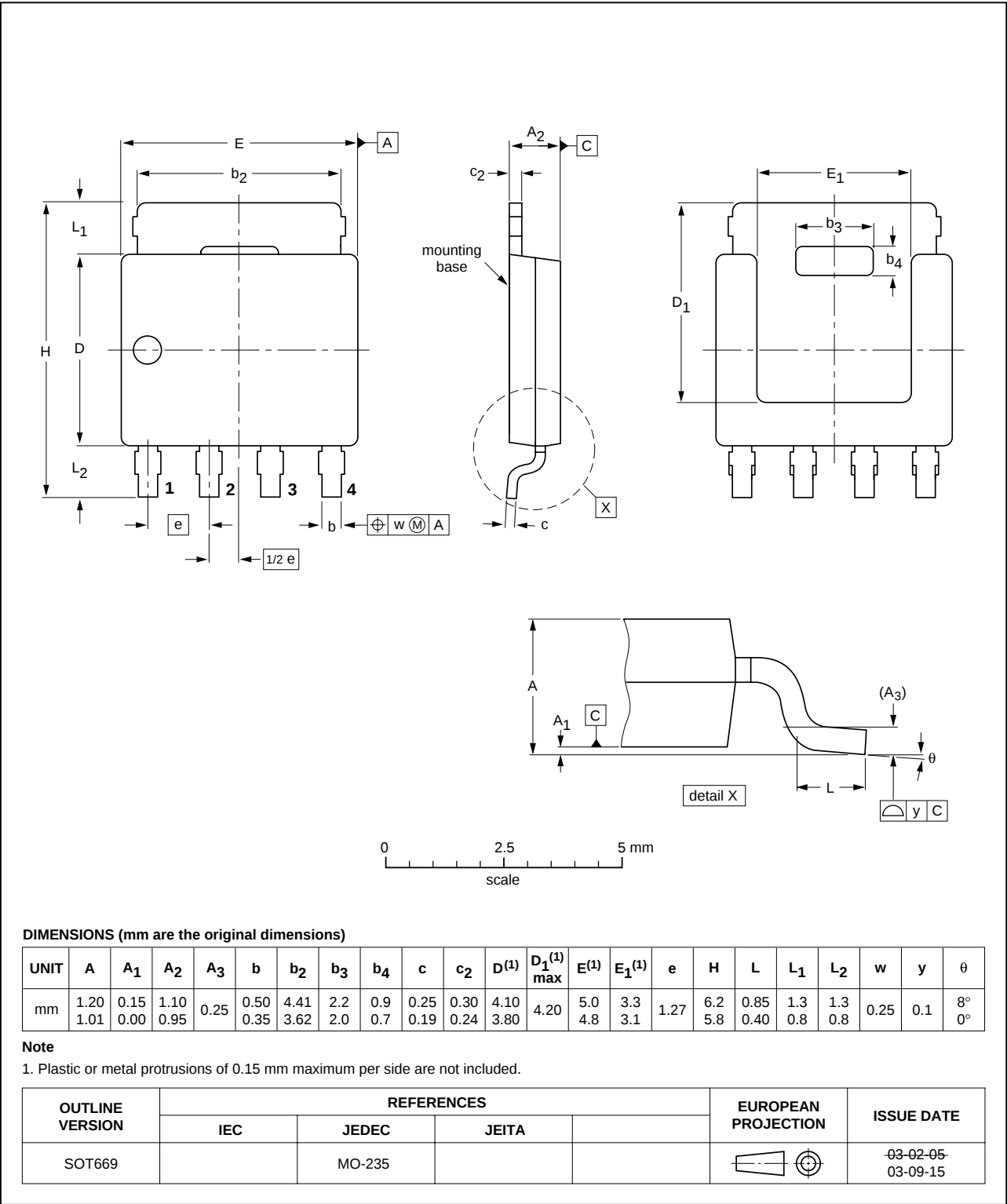


Fig 14. SOT669 (LFAK).

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8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20040302	-	Product data (9397 750 12945) Modifications: • Table 5 “Characteristics” t_r data revised.
02	20030918	-	Product data (9397 750 11776) Modifications: • Section 3 “Ordering information” added. • Table 5 “Characteristics” $Q_{g(tot)}$ data revised. • Table 3 “Limiting values” V_{GS} data revised. • Figure 7 revised.
01	20030502	-	Product data (9397 750 11403).

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9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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