



# PH6325L

N-channel 25 V 6.3 m $\Omega$  logic level MOSFET in LPAK

Rev. 2 — 22 December 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology

### 1.2 Features and benefits

- Low thermal resistance
- Low threshold voltage
- Optimized for use in DC-to-DC converters
- Very low switching and conduction losses

### 1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

### 1.4 Quick reference data

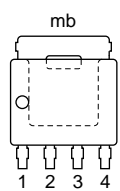
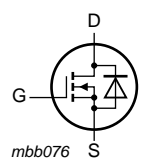
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	78.7	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	62.5	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	7.4	9.5	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	4.7	6.3	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	3.3	-	nC
$Q_{G(tot)}$	total gate charge		-	13.3	-	nC



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LPAK; Power-SO8)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PH6325L	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 4. Limiting values

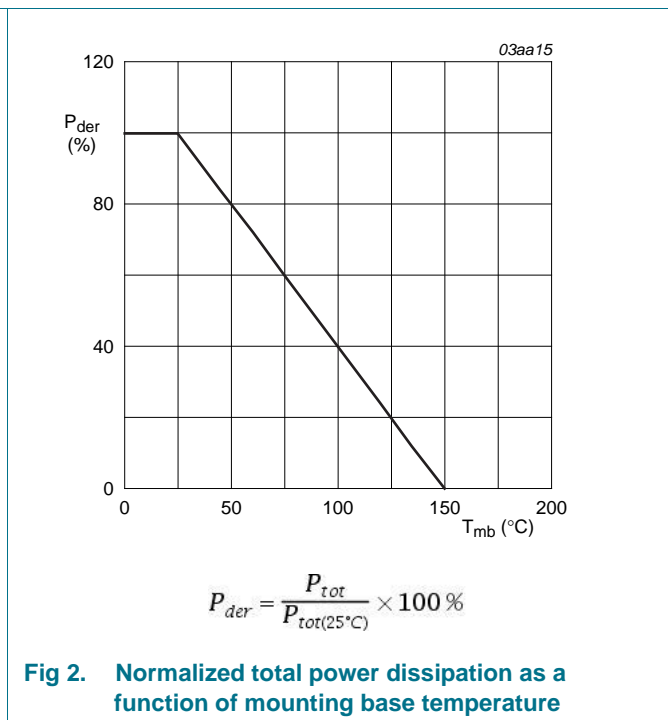
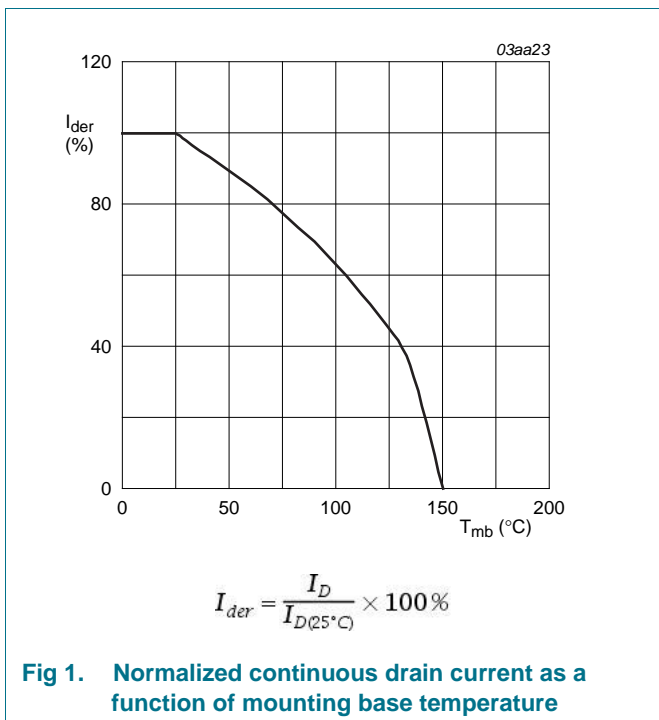
**Table 4. Limiting values**

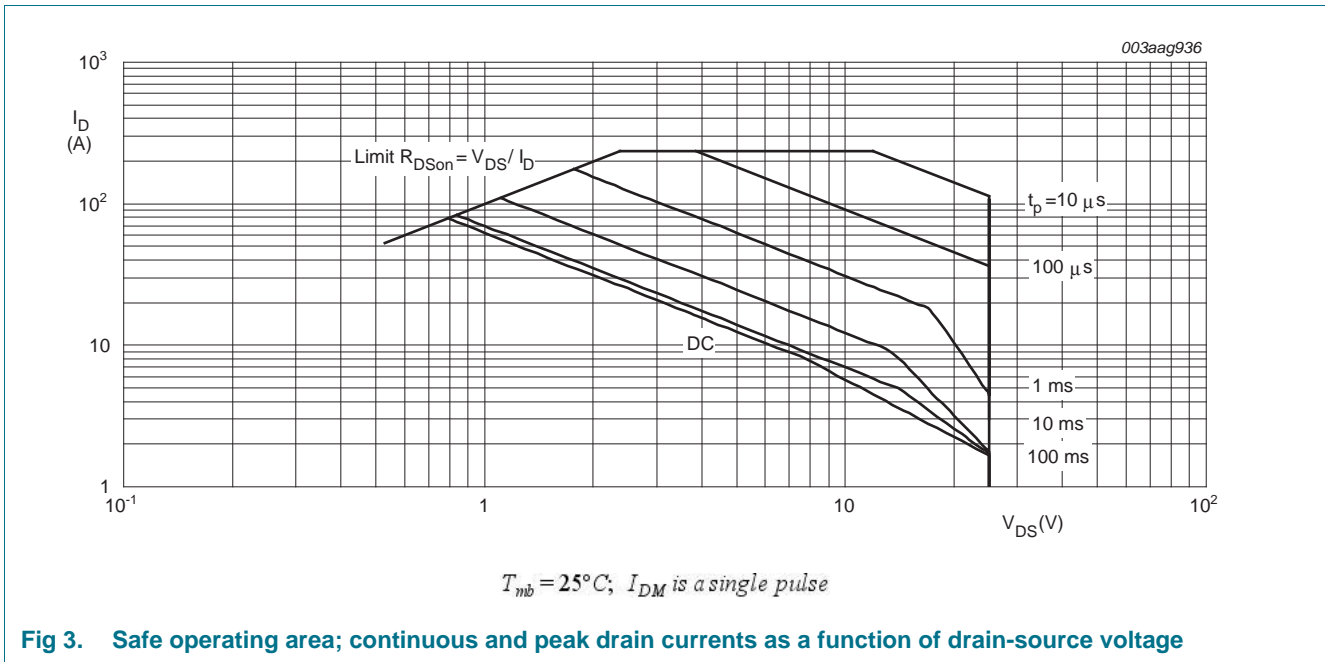
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	25	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	-	49.6	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	78.7	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	236	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	62.5	W
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	52	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	208	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)R</sub>	repetitive drain-source avalanche energy	t <sub>p</sub> = 0.015 ms; unclamped; R <sub>GS</sub> = 50 Ω; I <sub>D</sub> = 3.4 A; <a href="#">[1][2]</a>	-	1.2	mJ
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 34 A; V <sub>DD</sub> = 25 V; t <sub>p</sub> = 0.15 ms; unclamped; R <sub>GS</sub> = 50 Ω	-	115	mJ

[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.





### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

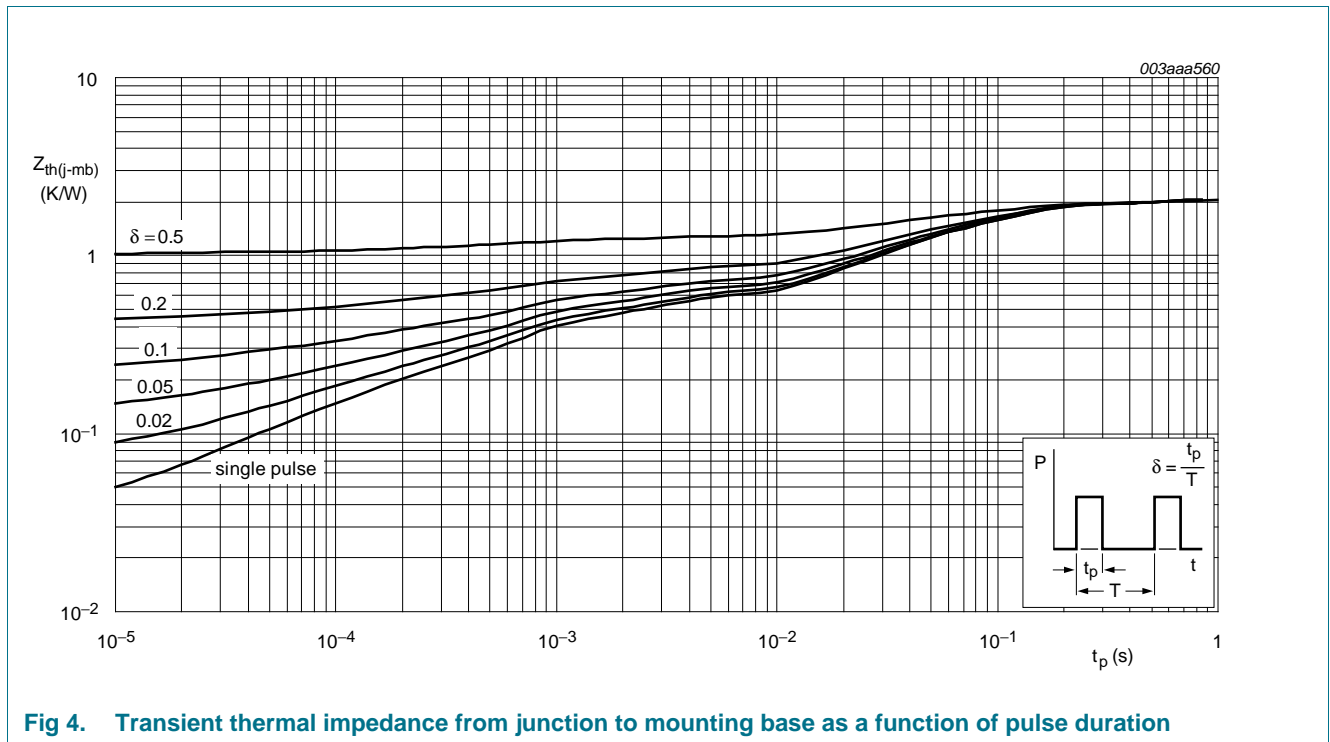


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	2.2	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.06	1	$\mu\text{A}$
		$V_{DS} = 25 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -16 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	7.5	10.1	mΩ
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	11.8	15.2	mΩ
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	7.4	9.5	mΩ
		$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	4.7	6.3	mΩ
$R_G$	internal gate resistance	$f = 1 \text{ MHz}$	-	1.8	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$ ; $V_{DS} = 12 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	13.3	-	nC
		$I_D = 0 \text{ A}$ ; $V_{DS} = 0 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$	-	11.1	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}$ ; $V_{DS} = 12 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	4.9	-	nC
$Q_{GS1}$	pre-threshold gate-source charge		-	2.6	-	nC
$Q_{GS2}$	post-threshold gate-source charge		-	2.3	-	nC
$Q_{GD}$	gate-drain charge		-	3.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$ ; $V_{DS} = 12 \text{ V}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	2.4	-	V
$C_{iss}$	input capacitance	$V_{DS} = 0 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2420	-	pF
		$V_{DS} = 12 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	1871	-	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	517	-	pF
$C_{rss}$	reverse transfer capacitance		-	179	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 \text{ V}$ ; $V_{GS} = 4.5 \text{ V}$ ; $R_{G(ext)} = 4.7 \text{ } \Omega$ ; $I_D = 25 \text{ A}$	-	25	-	ns
$t_r$	rise time		-	25	-	ns
$t_{d(off)}$	turn-off delay time		-	32	-	ns
$t_f$	fall time		-	12	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	33	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$	-	13	-	nC

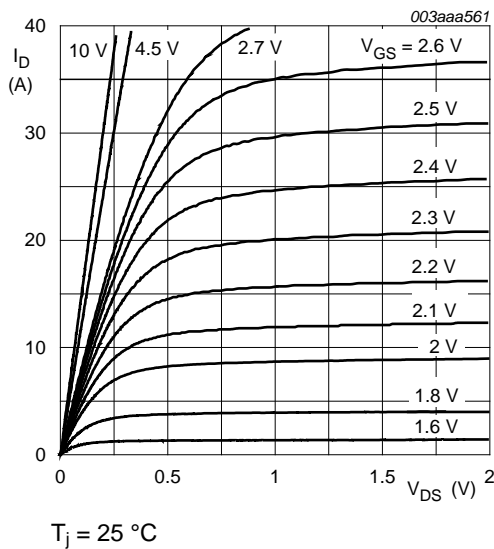


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

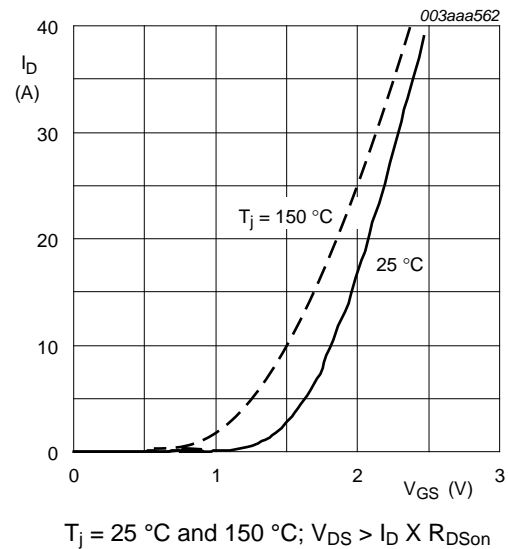


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

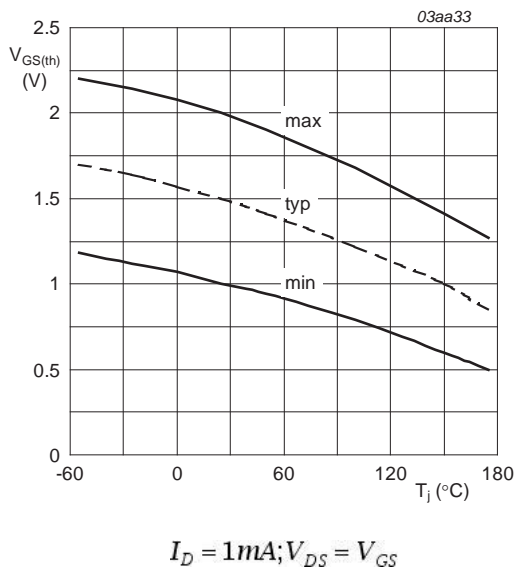


Fig 7. Gate-source threshold voltage as a function of junction temperature

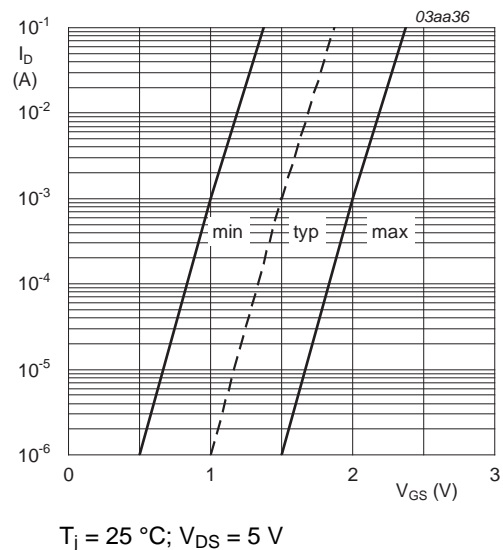
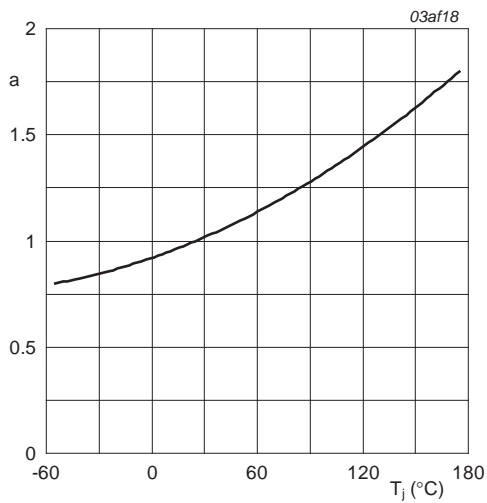
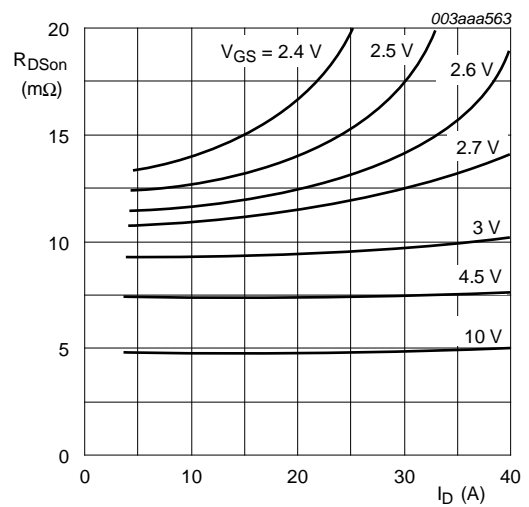


Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



T<sub>j</sub> = 25 °C

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

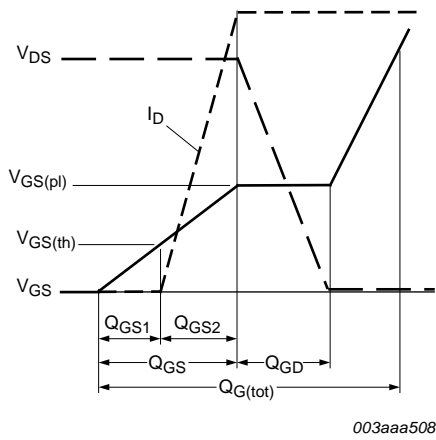
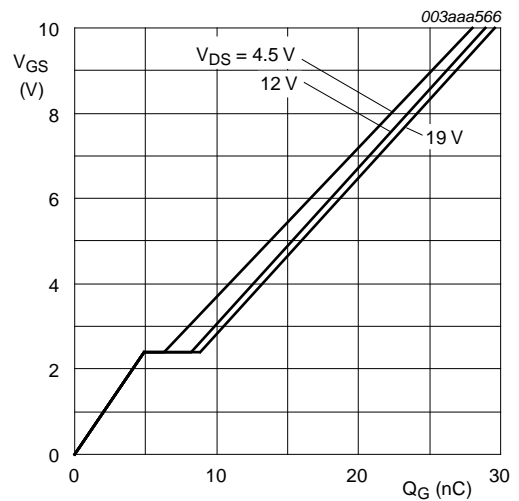


Fig 11. Gate charge waveform definitions



I<sub>D</sub> = 25 A; V<sub>DS</sub> = 4.5 V, 12 V and 19 V

Fig 12. Gate-source voltage as a function of gate charge; typical values



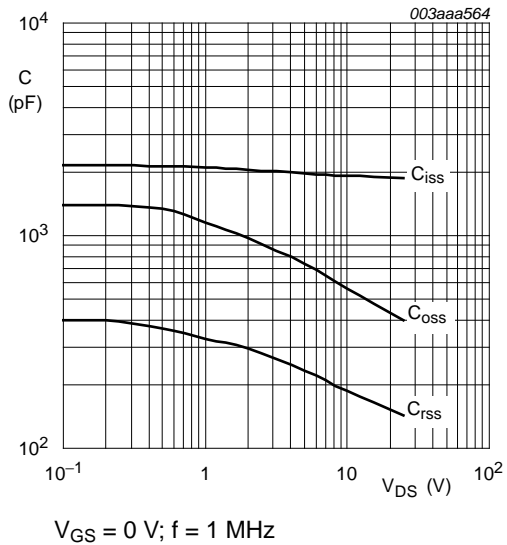


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

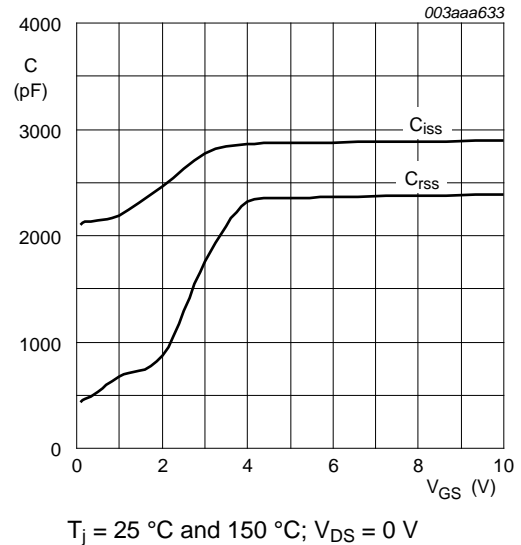
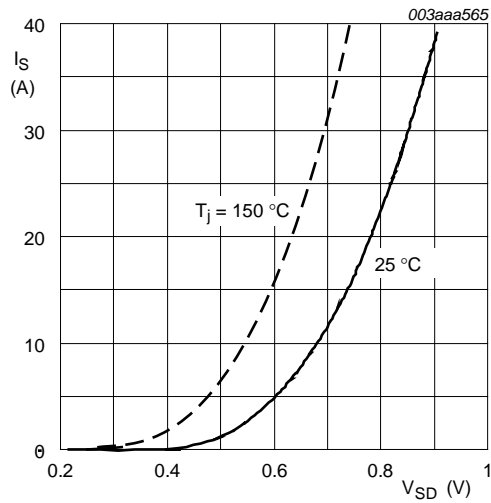


Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



$T_j = 25 \text{ }^\circ\text{C}$  and  $150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669

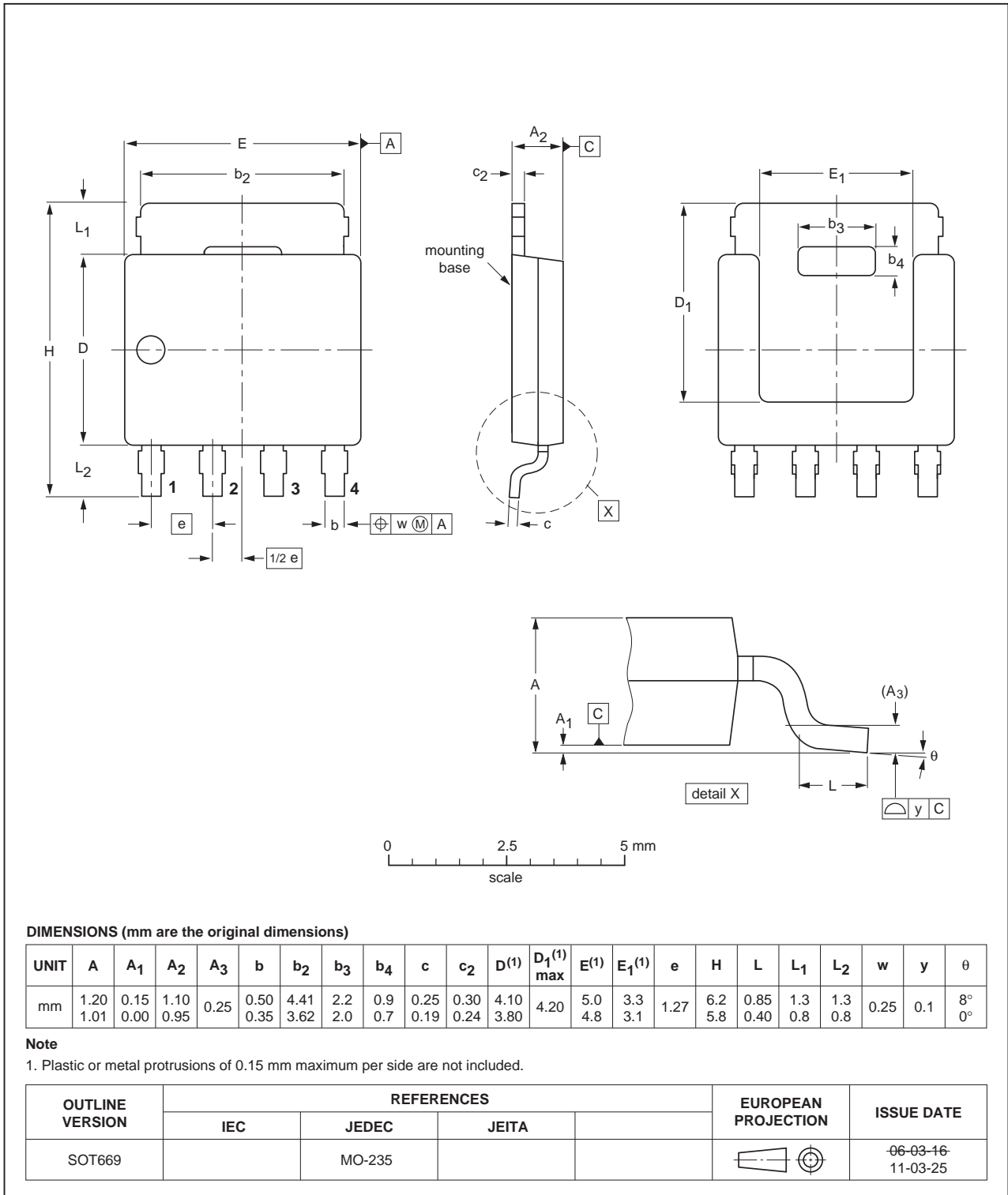


Fig 16. Package outline SOT669 (LPAK; Power-SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH6325L v.2	20111222	Product data sheet	-	PH6325L v.1
Modifications:	<ul style="list-style-type: none"><li>• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Status changed from preliminary to product.</li></ul>			
PH6325L v.1	20040428	Preliminary data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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