

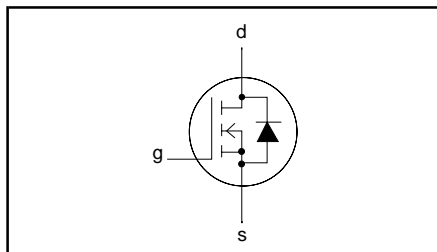
TrenchMOS™ transistor Logic level FET

PHB42N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Surface mounting package

SYMBOL



QUICK REFERENCE DATA

| |
|--|
| $V_{DSS} = 30\text{ V}$ |
| $I_D = 42\text{ A}$ |
| $R_{DS(ON)} \leq 26\text{ m}\Omega$ ($V_{GS} = 5\text{ V}$) |
| $R_{DS(ON)} \leq 23\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$) |

GENERAL DESCRIPTION

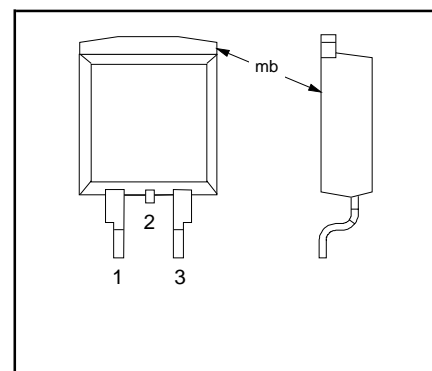
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHB42N03LT is supplied in the SOT404 surface mounting package.

PINNING

| PIN | DESCRIPTION |
|-----|--------------------------------|
| 1 | gate |
| 2 | drain (no connection possible) |
| 3 | source |
| tab | drain |

SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|----------------------------------|--------------------------------------|------|------|------------------|
| V_{DS} | Drain-source voltage | - | - | 30 | V |
| V_{DGR} | Drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 30 | V |
| $\pm V_{GS}$ | Gate-source voltage | - | - | 15 | V |
| I_D | Drain current (DC) | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 42 | A |
| I_D | Drain current (DC) | $T_{mb} = 100\text{ }^\circ\text{C}$ | - | 33 | A |
| I_{DM} | Drain current (pulse peak value) | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 168 | A |
| P_{tot} | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 86 | W |
| T_{stg}, T_j | Storage & operating temperature | - | - 55 | 175 | $^\circ\text{C}$ |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|----------------|--|--------------------------------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | - | - | 1.75 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | pcb mounted, minimum footprint | 50 | - | K/W |

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STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------|----------------------------------|---|-------------|---------------|----------------|----------------|
| V _{(BR)DSS} | Drain-source breakdown voltage | V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55°C | 30 27 | - - | - - | V V |
| V _{GS(TO)} | Gate threshold voltage | V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175°C T _j = -55°C | 1 0.5 | 1.5 - | 2 - | V V |
| I _{DSS} | Zero gate voltage drain current | V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175°C | - - | 0.05 - | 10 500 | μA μA |
| I _{GSS} | Gate source leakage current | V _{GS} = ±5 V; V _{DS} = 0 V | - | 10 | 100 | nA |
| R _{DS(ON)} | Drain-source on-state resistance | V _{GS} = 5 V; I _D = 25 A V _{GS} = 10 V; I _D = 25 A V _{GS} = 5 V; I _D = 25 A; T _j = 175°C | - - - | 20 16 - | 26 23 48 | mΩ mΩ mΩ |

DYNAMIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------|----------------------------|--|------|------|------|------|
| g _{fs} | Forward transconductance | V _{DS} = 25 V; I _D = 25 A | 8 | 16 | - | S |
| Q _{g(tot)} | Total gate charge | I _D = 40 A; V _{DD} = 24 V; V _{GS} = 5 V | - | 23 | - | nC |
| Q _{gs} | Gate-source charge | | - | 3 | - | nC |
| Q _{gd} | Gate-drain (Miller) charge | | - | 9 | - | nC |
| C _{iss} | Input capacitance | V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz | - | 1050 | - | pF |
| C _{oss} | Output capacitance | | - | 270 | - | pF |
| C _{rss} | Feedback capacitance | | - | 140 | - | pF |
| t _{d on} | Turn-on delay time | V _{DD} = 15 V; I _D = 25 A; | - | 30 | 45 | ns |
| t _r | Turn-on rise time | V _{GS} = 5 V; R _G = 5 Ω | - | 80 | 130 | ns |
| t _{d off} | Turn-off delay time | Resistive load | - | 95 | 135 | ns |
| t _f | Turn-off fall time | | - | 40 | 55 | ns |
| L _d | Internal drain inductance | Measured from tab to centre of die | - | 3.5 | - | nH |
| L _d | Internal drain inductance | Measured from drain lead solder point to centre of die | - | 4.5 | - | nH |
| L _s | Internal source inductance | Measured from source lead solder point to source bond pad | - | 7.5 | - | nH |

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|----------------------------------|--|--------|-------------|----------|------|
| I _{DR} | Continuous reverse drain current | | - | - | 42 | A |
| I _{DRM} | Pulsed reverse drain current | | - | - | 168 | A |
| V _{SD} | Diode forward voltage | I _F = 25 A; V _{GS} = 0 V I _F = 40 A; V _{GS} = 0 V | - - | 0.95 1.0 | 1.2 - | V |
| t _{rr} | Reverse recovery time | I _F = 40 A; -di _F /dt = 100 A/μs; | - | 52 | - | ns |
| Q _{rr} | Reverse recovery charge | V _{GS} = -10 V; V _R = 25 V | - | 0.08 | - | μC |

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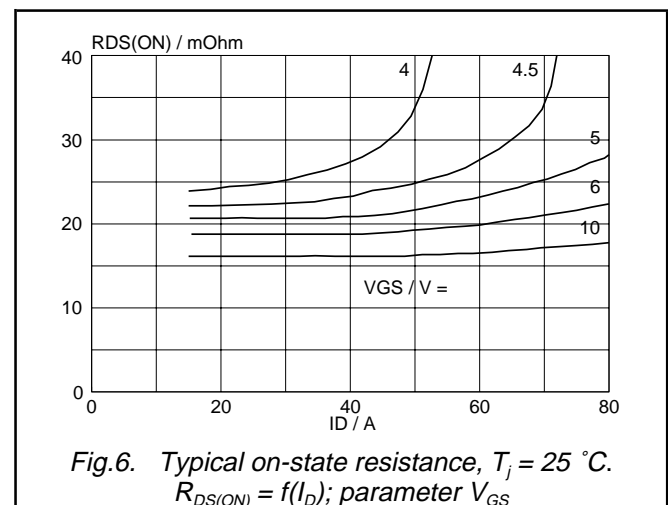
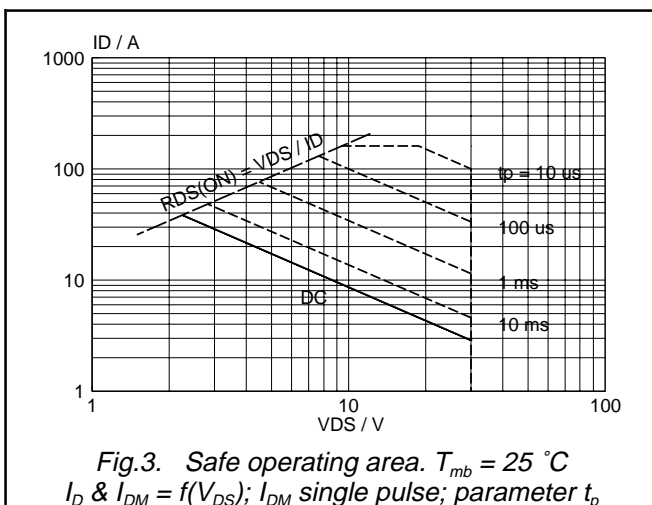
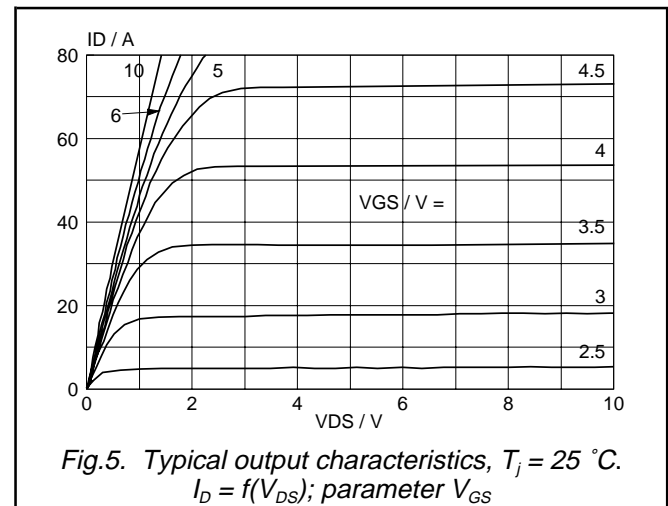
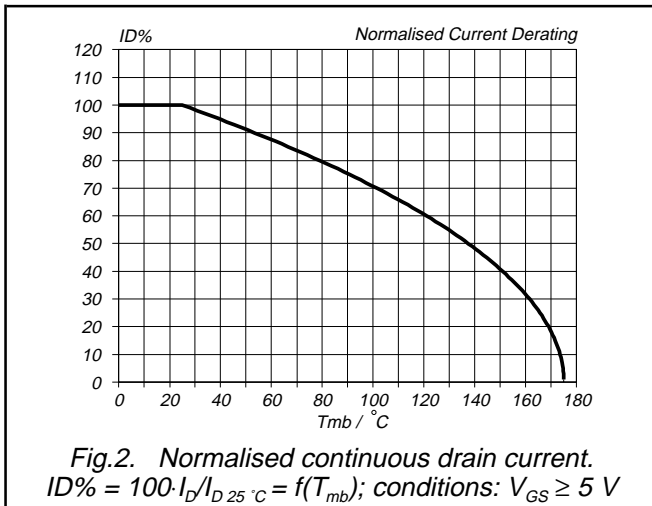
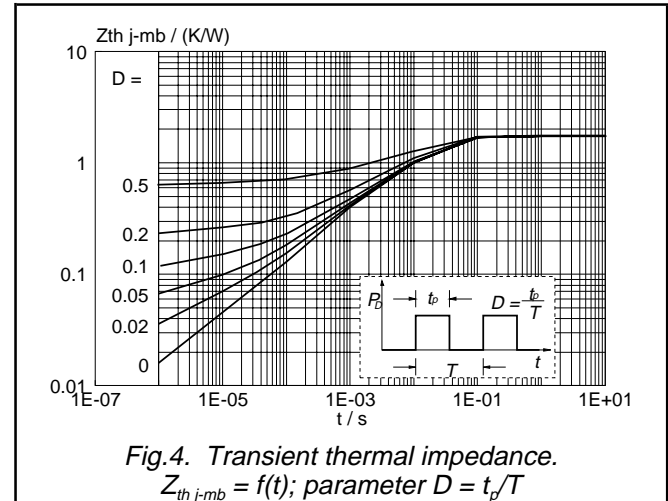
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AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|---|--|------|------|------|------|
| W_{DSS} | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D = 25 \text{ A}$; $V_{DD} \leq 25 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \text{ } \Omega$; $T_{mb} = 25 \text{ } ^\circ\text{C}$ | - | - | 60 | mJ |

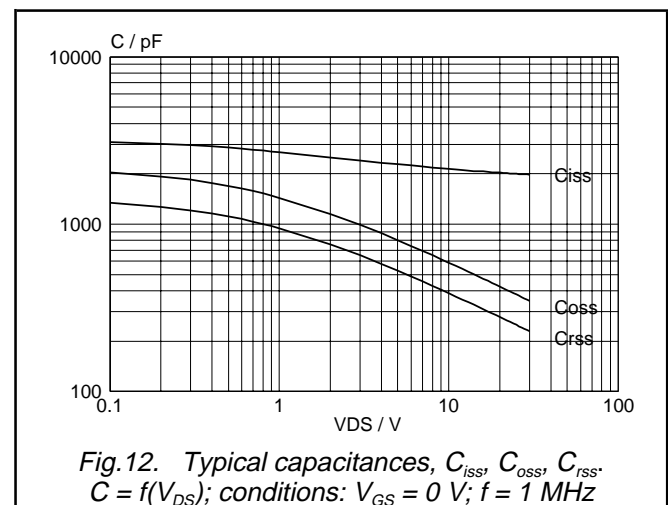
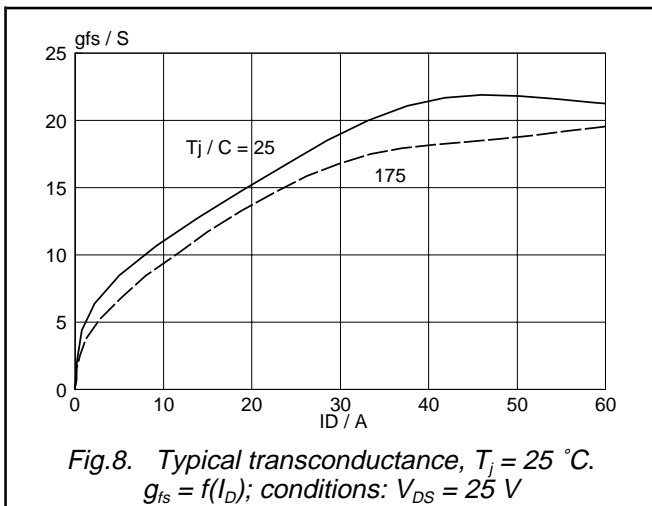
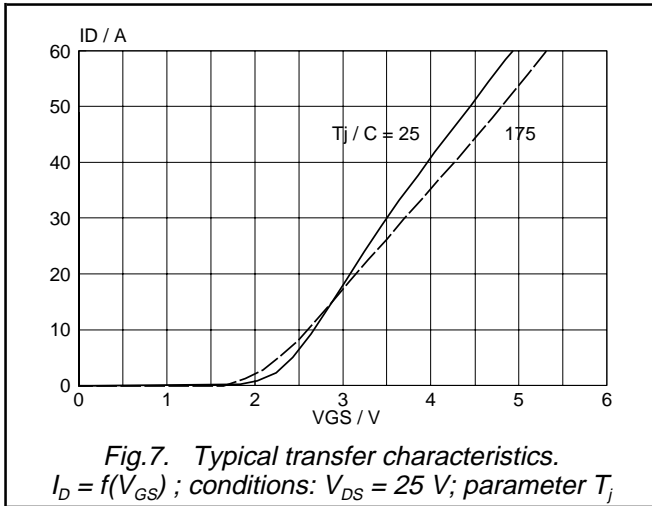
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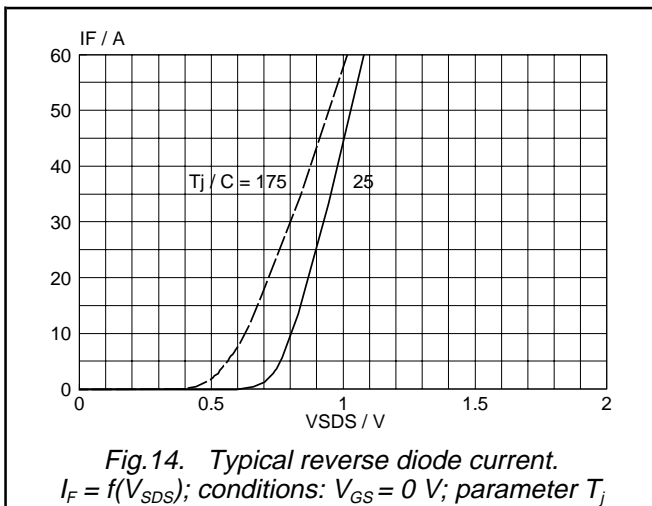
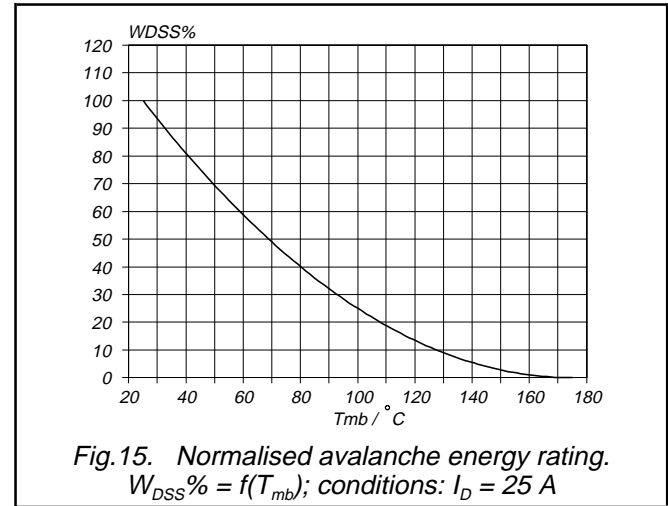
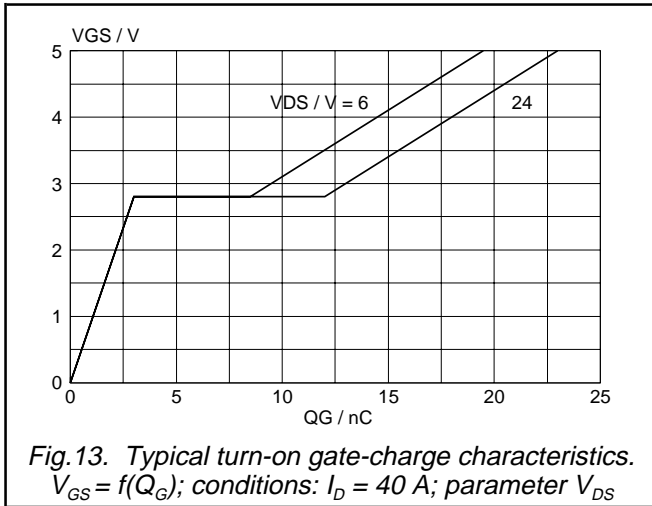
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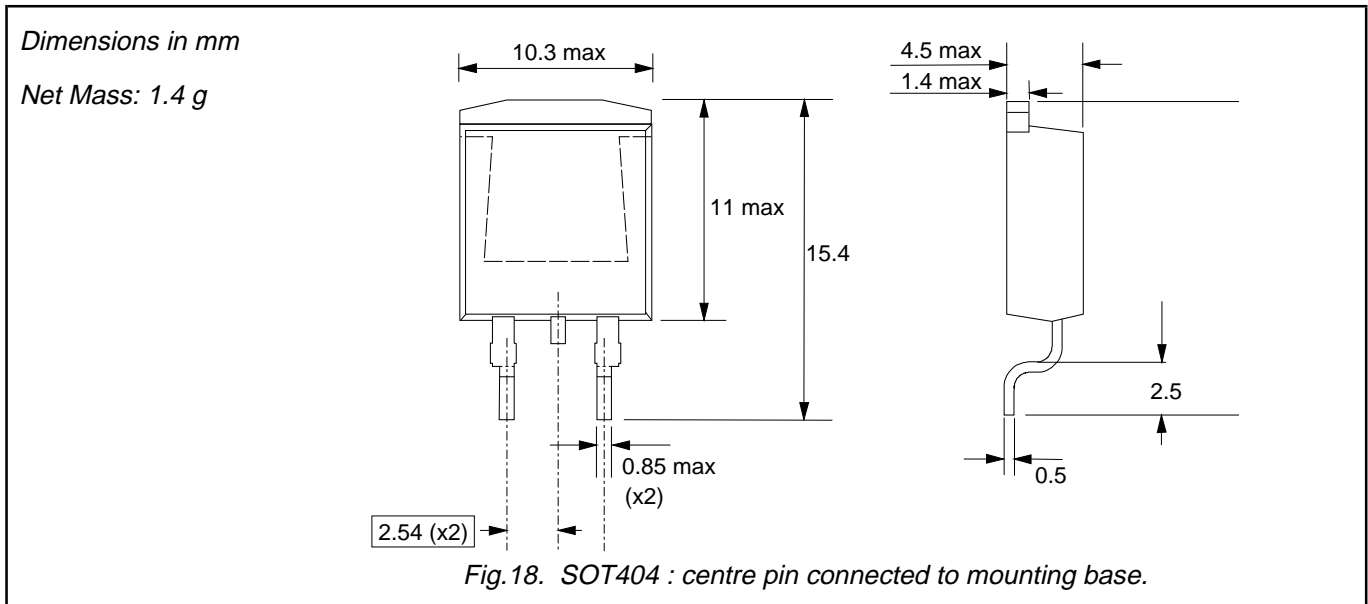
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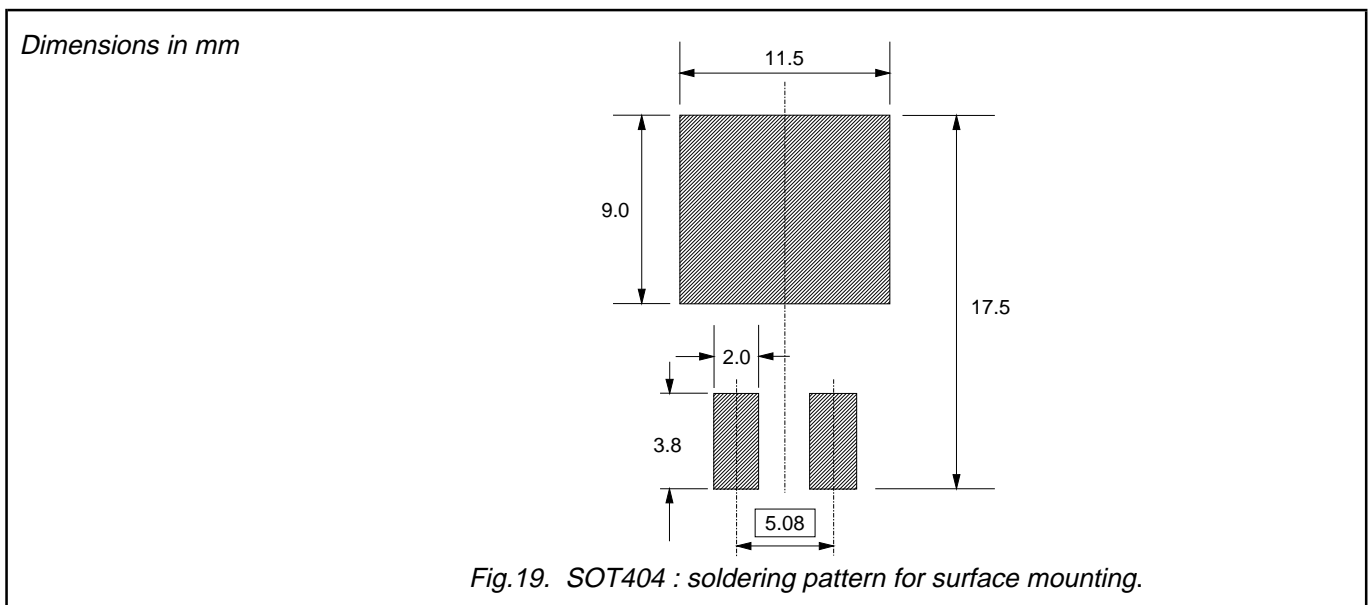
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MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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