

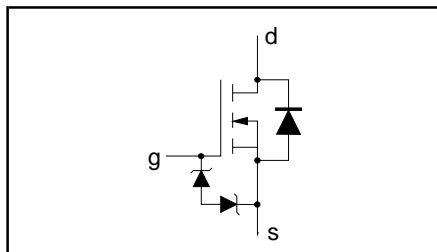
TrenchMOS™ transistor Logic level FET

PHB11N06LT, PHD11N06LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 55 \text{ V}$
$I_D = 11 \text{ A}$
$R_{DS(ON)} \leq 150 \text{ m}\Omega (V_{GS} = 5 \text{ V})$
$R_{DS(ON)} \leq 130 \text{ m}\Omega (V_{GS} = 10 \text{ V})$

GENERAL DESCRIPTION

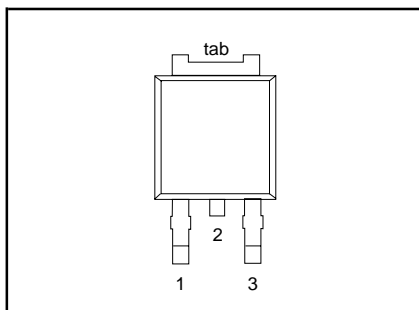
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHB11N06LT is supplied in the SOT404 surface mounting package.
The PHD11N06LT is supplied in the SOT428 surface mounting package.

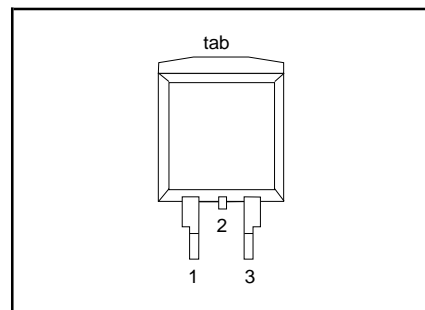
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

SOT428



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $175 \text{ }^\circ\text{C}$	-	55	V
V_{DGR}	Drain-gate voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $175 \text{ }^\circ\text{C}$; $R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	11	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$	-	7.6	A
I_{DM}	Pulsed drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	44	A
P_D	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	36	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

¹ It is not possible to make contact to pin 2 of the SOT404 or SOT428 package

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ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 k Ω)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	4.17	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT428 and SOT404 package, pcb mounted, minimum footprint	60 50	- -	K/W K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA};$ $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1.0 0.5 -	1.5 - -	2.0 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5.5\text{ A}$ $V_{GS} = 5\text{ V}; I_D = 5.5\text{ A}$ $T_j = 175^\circ\text{C}$	- - -	100 120 250	130 150 315	m Ω m Ω m Ω
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5.5\text{ A}$ $T_j = 175^\circ\text{C}$	4	10	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5\text{ V}; V_{DS} = 0\text{ V}$ $T_j = 175^\circ\text{C}$	-	0.02	1	μA μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 175^\circ\text{C}$	-	0.05	10	μA μA
$Q_{g(tot)}$	Total gate charge	$I_D = 11\text{ A}; V_{DD} = 44\text{ V}; V_{GS} = 5\text{ V}$	-	6.1	-	nC
Q_{gs}	Gate-source charge		-	1.3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	3.2	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 5\text{ A};$ $V_{GS} = 5\text{ V}; R_G = 10\ \Omega$	-	6	16	ns
t_r	Turn-on rise time	Resistive load	-	23	35	ns
$t_{d\ off}$	Turn-off delay time		-	18	30	ns
t_f	Turn-off fall time		-	18	30	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	250	330	pF
C_{oss}	Output capacitance		-	34	50	pF
C_{rss}	Feedback capacitance		-	35	50	pF

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

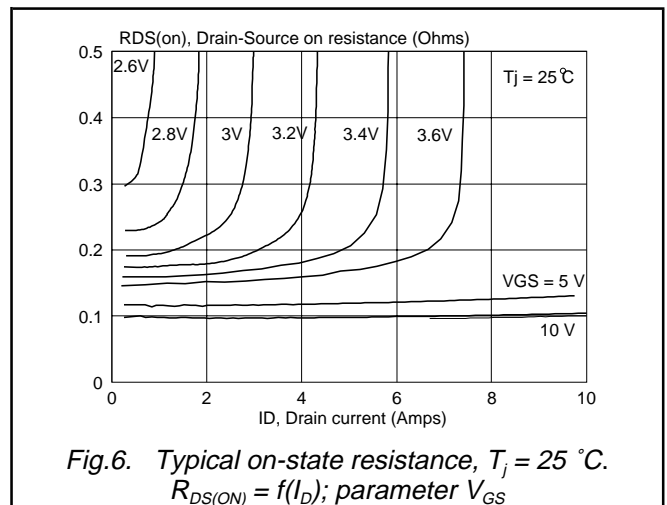
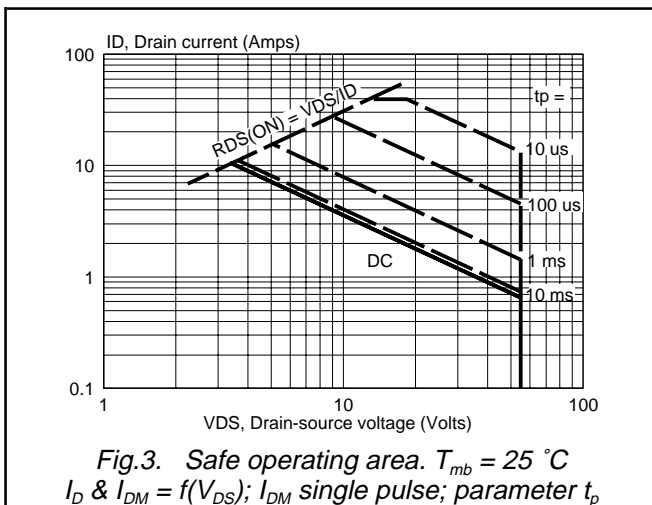
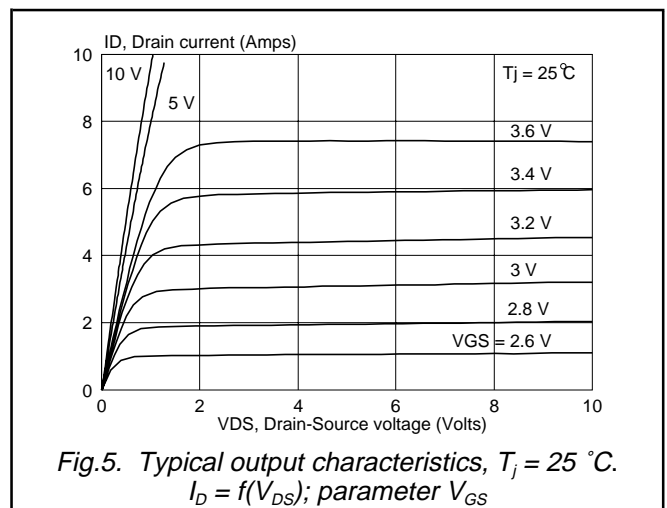
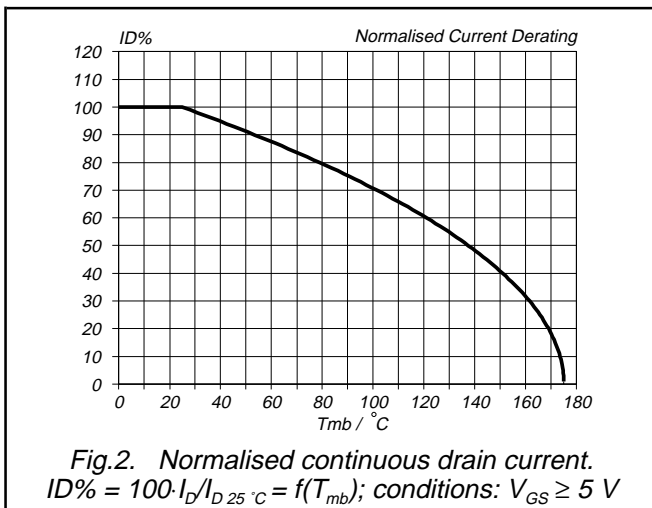
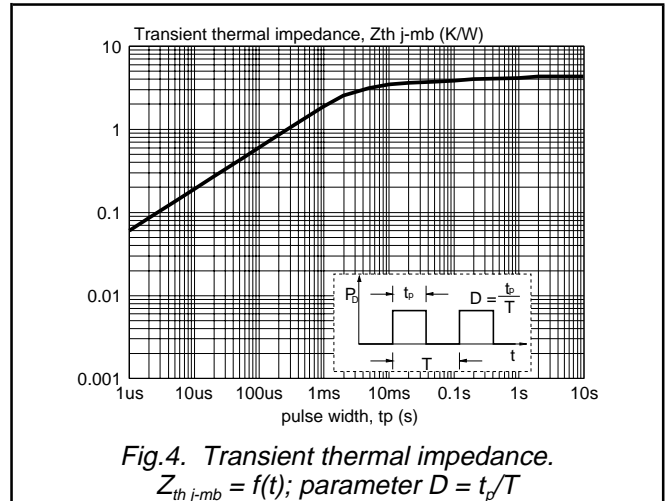
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	11	A
I_{SM}	Pulsed source current (body diode)		-	-	44	A
V_{SD}	Diode forward voltage	$I_F = 11\text{ A}; V_{GS} = 0\text{ V}$	-	0.95	1.2	V
t_{rr}	Reverse recovery time	$I_F = 11\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	34	-	ns
Q_{rr}	Reverse recovery charge		-	57	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D \leq 10\text{ A}; V_{DD} \leq 25\text{ V}; V_{GS} = 5\text{ V};$ $R_{GS} = 50\ \Omega; T_{mb} = 25^\circ\text{C}$	-	10	mJ

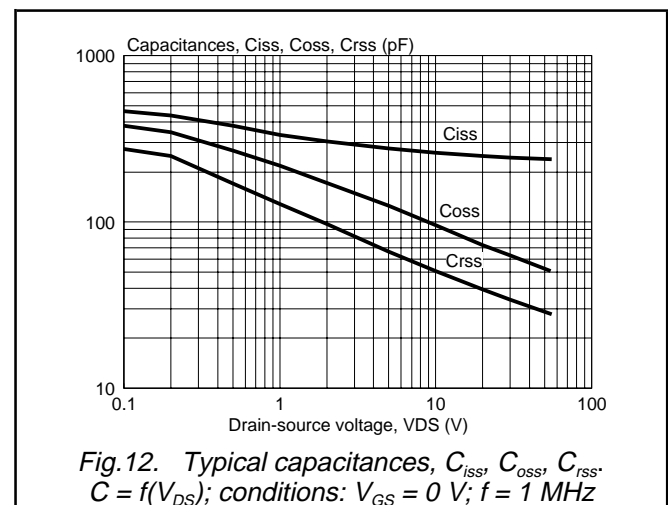
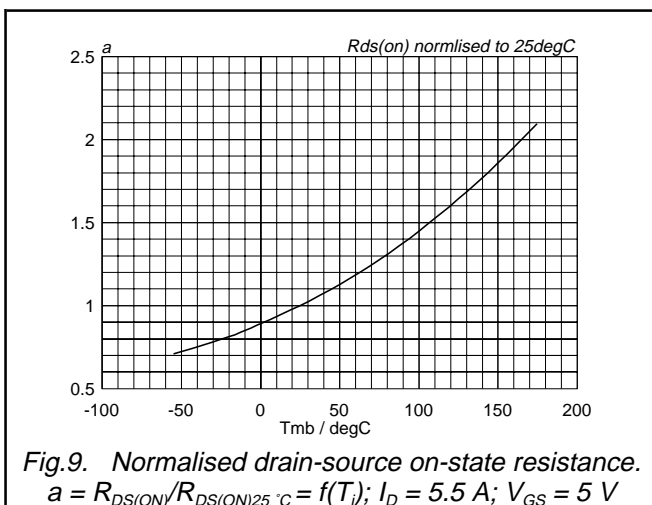
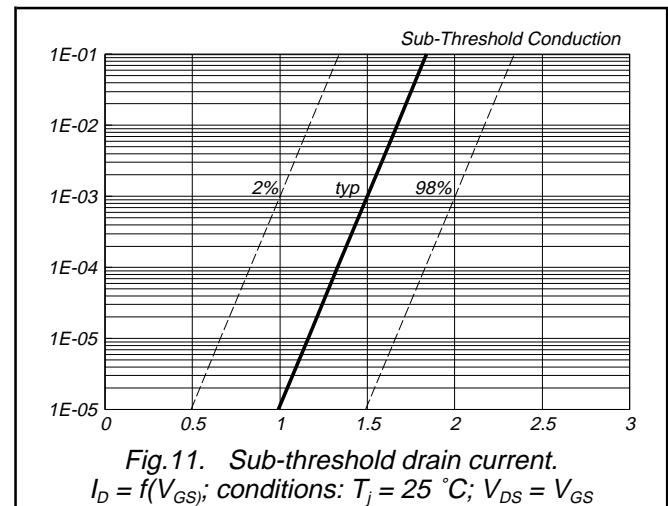
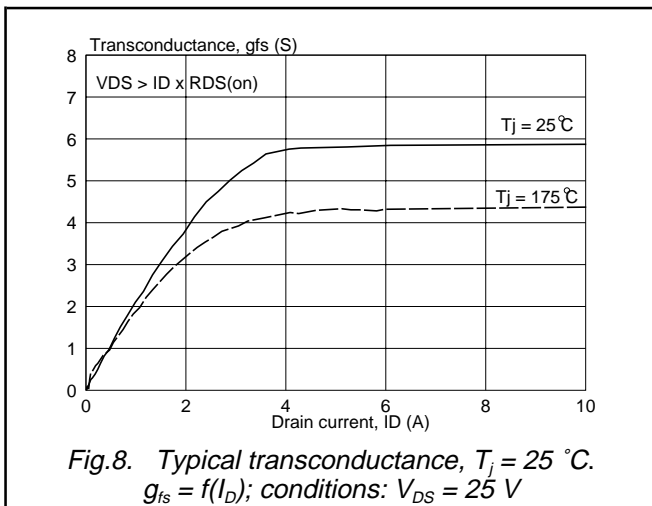
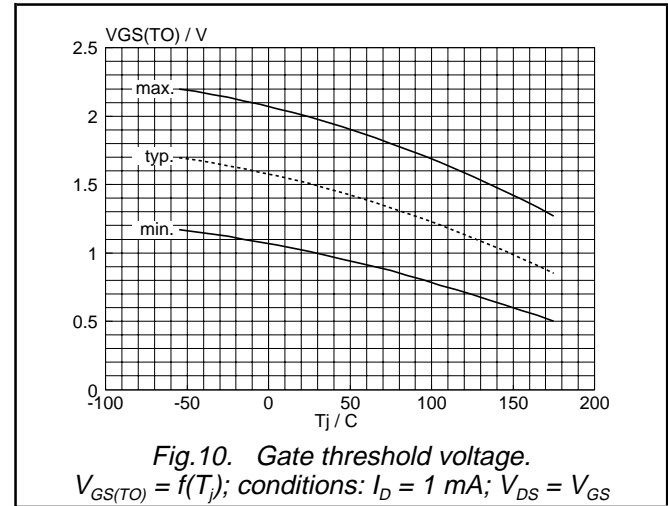
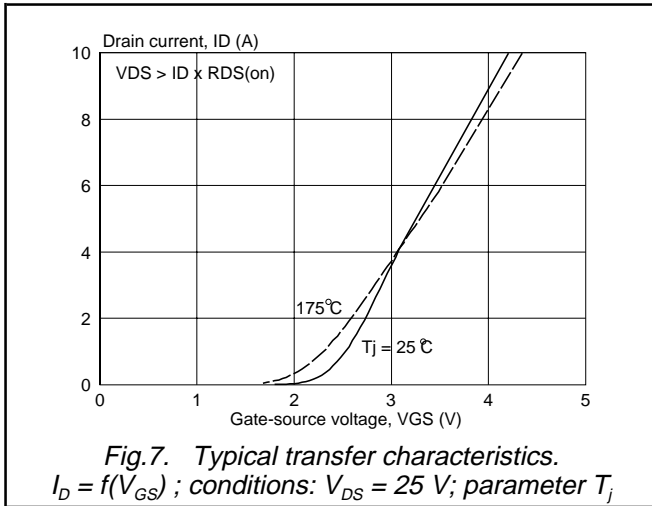
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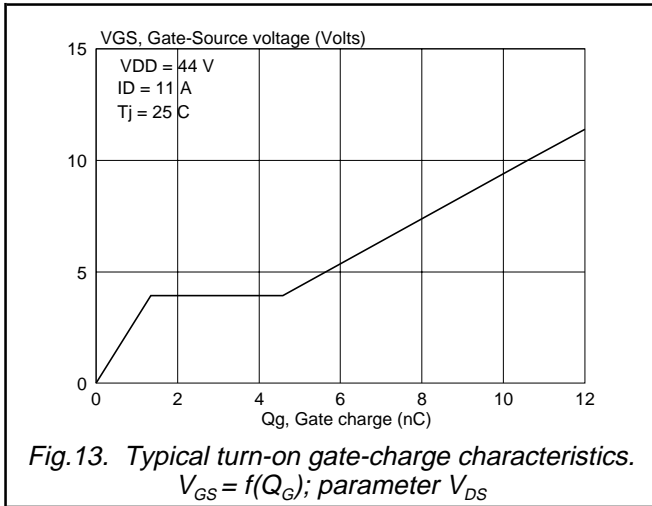


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; parameter V_{DS}

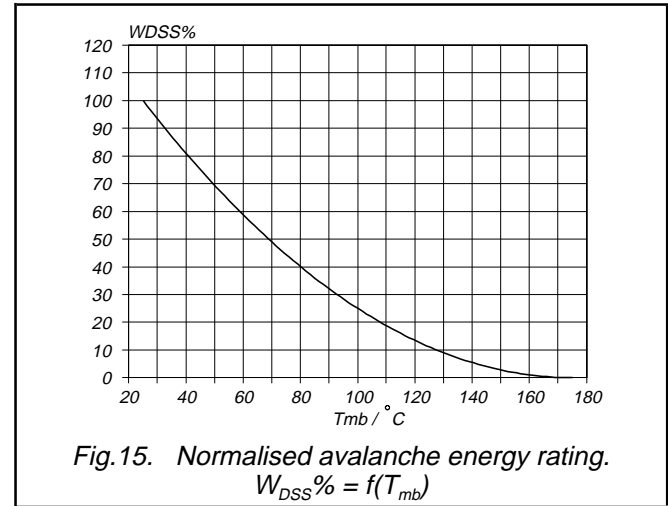


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$

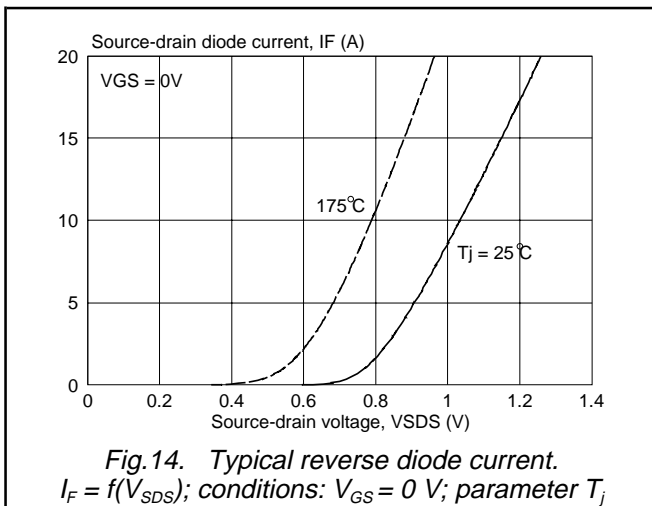


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0 V$; parameter T_j

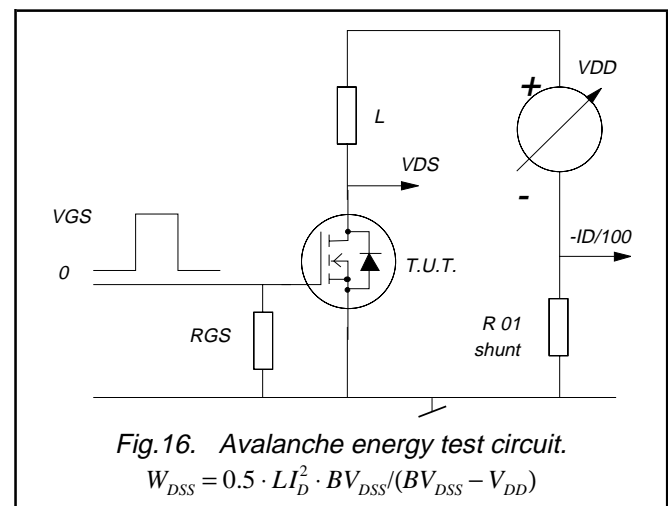
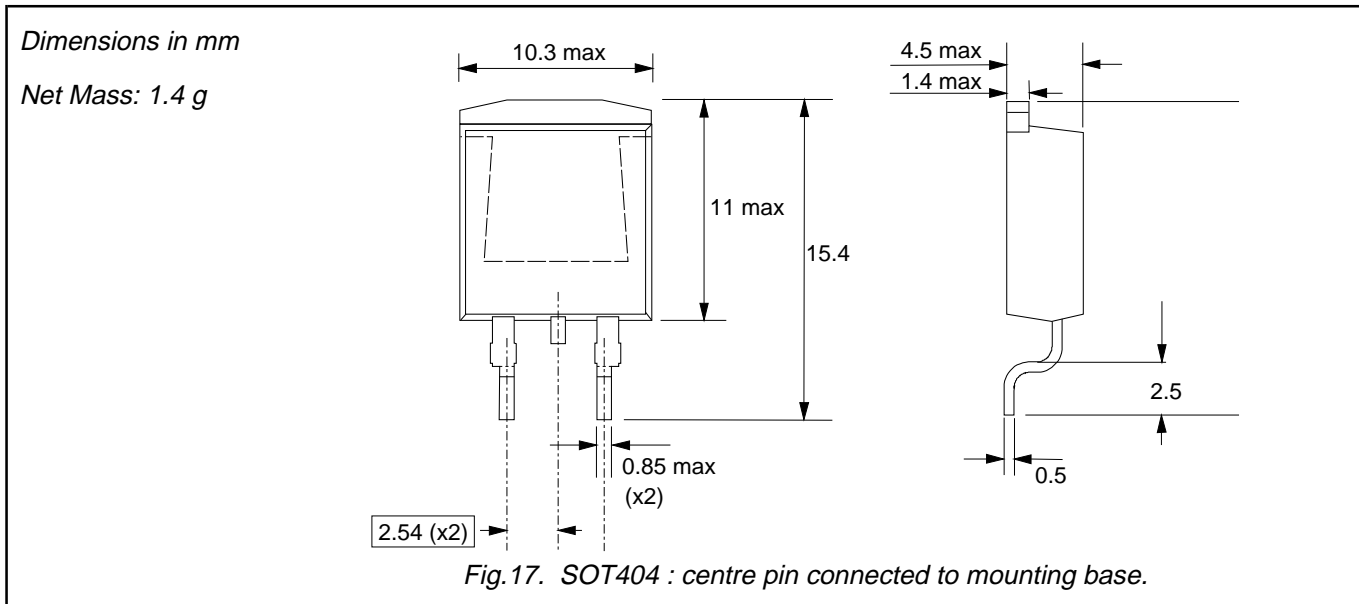


Fig.16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

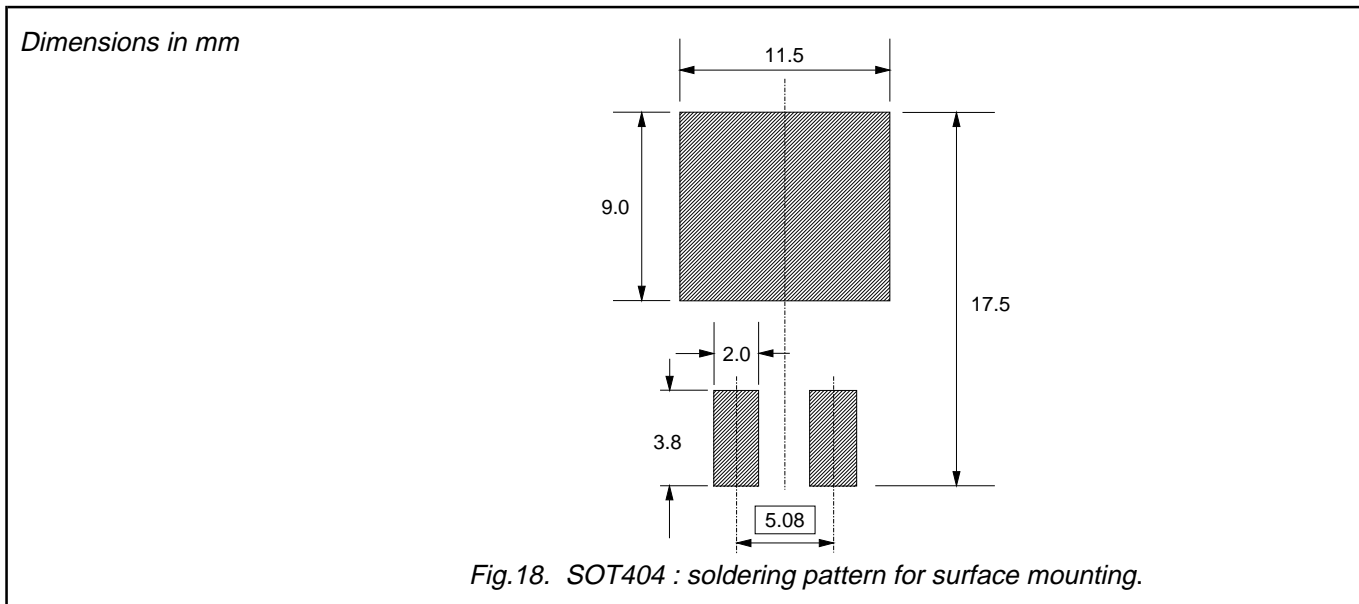
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MECHANICAL DATA



MOUNTING INSTRUCTIONS



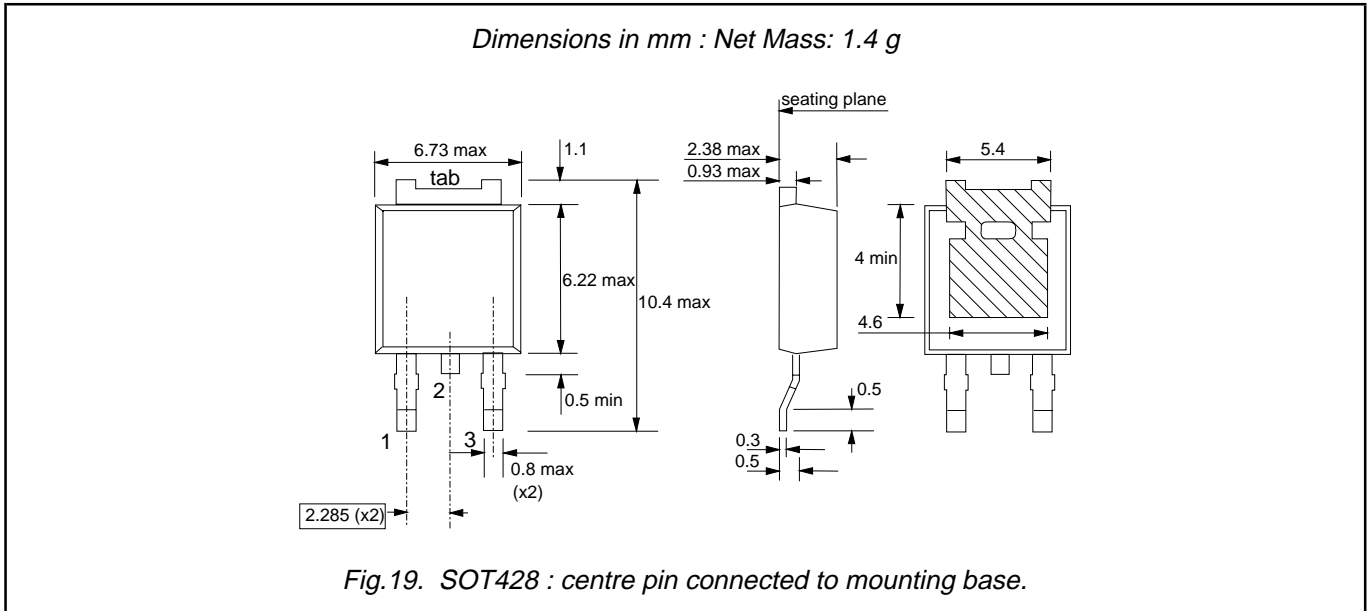
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

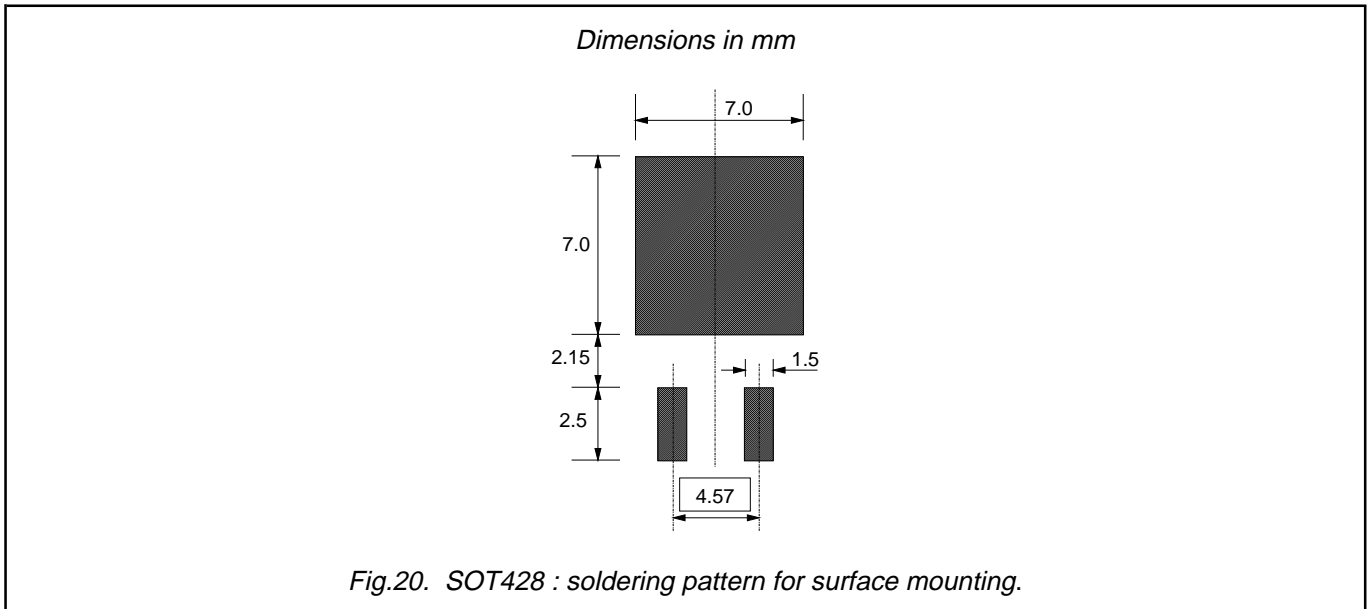
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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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